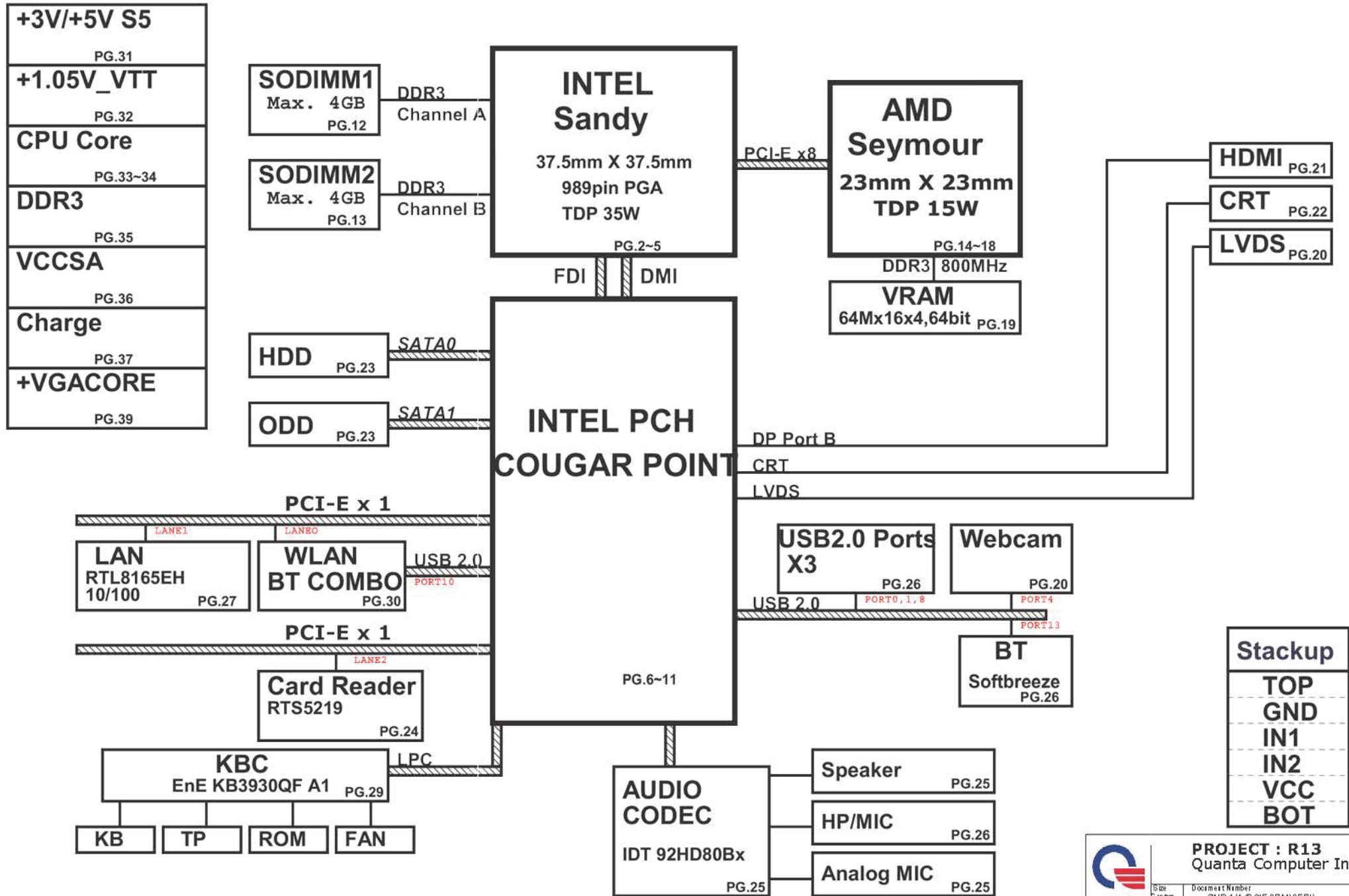
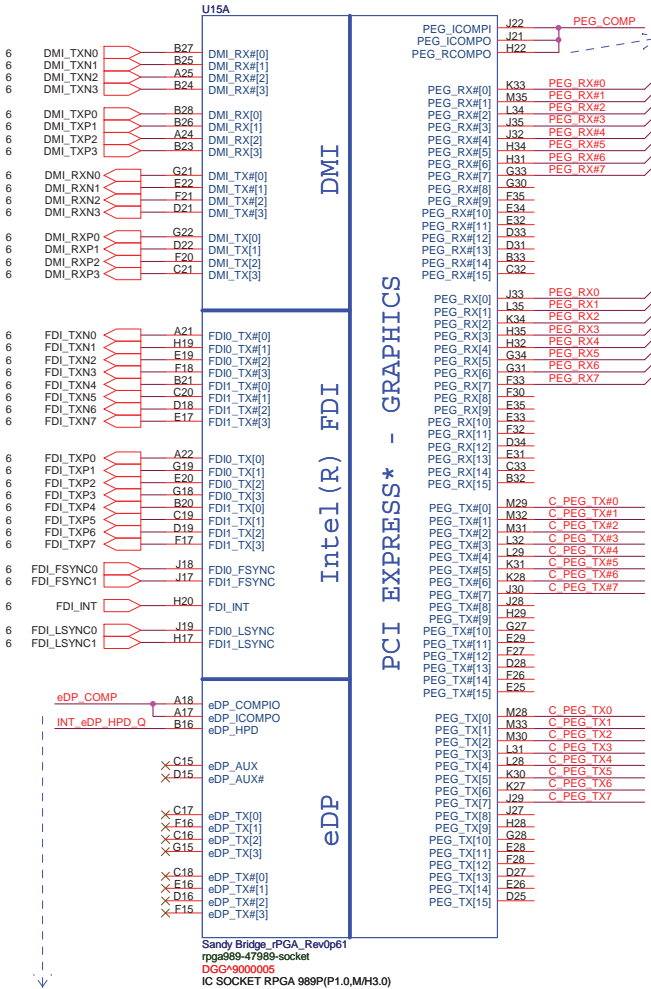


# R13 INTEL UMA/DISCRETE SYSTEM DIAGRAM

01

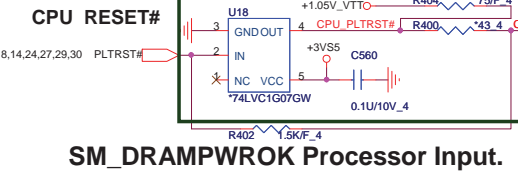
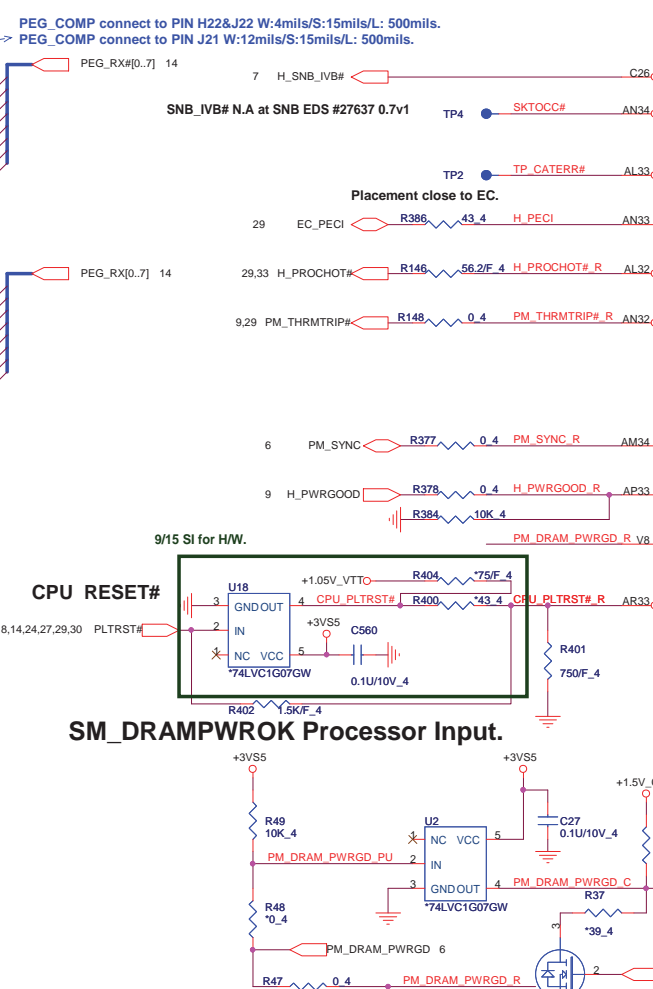


<b>Stackup</b>
TOP
GND
IN1
IN2
VCC
BOT

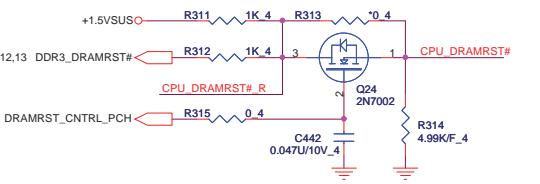
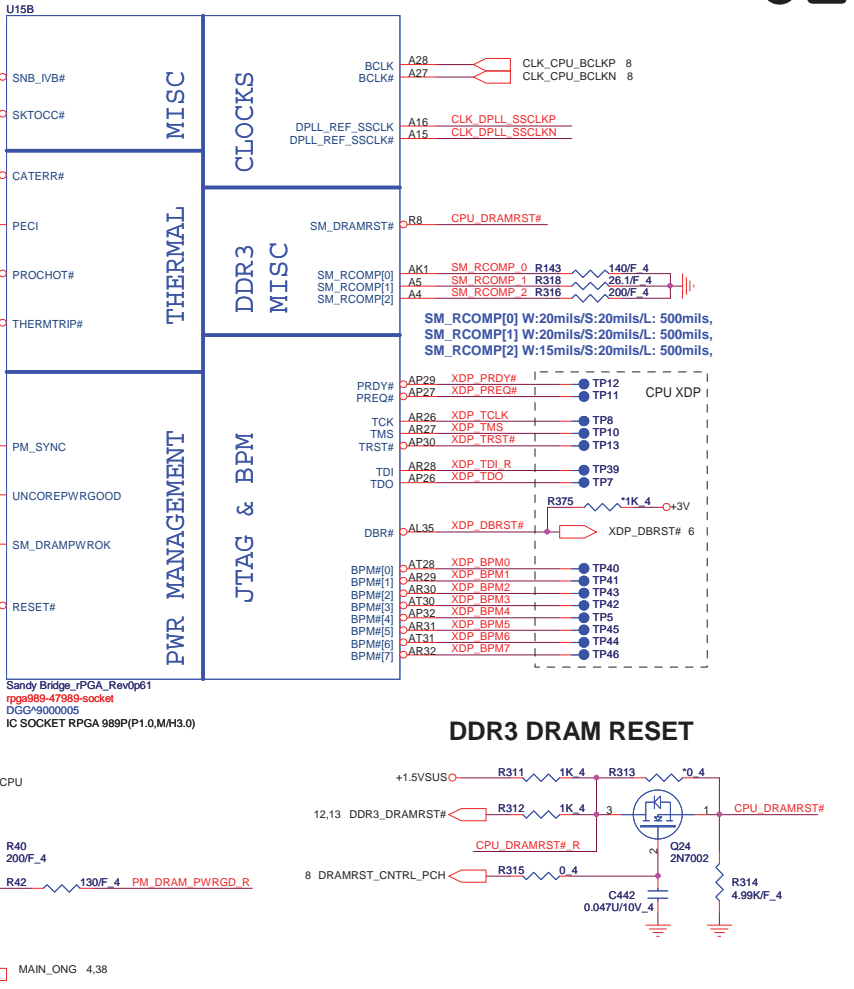


Intel (R) FDI  
PCI EXPRESS\* - GRAPHICS

eDP\_COMP connect to PIN A18 W:4mils/S:15mils/L: 500mils.  
eDP\_COMP connect to PIN A17 W:12mils/S:15mils/L: 500mils.



SM\_DRAMPWROK Processor Input.



- +1.05V\_VTT 4,6,7,8,10,29,32,33
- +1.5V\_CPU 4
- +3V55 6,7,8,9,10,22,26,31,32,38,39
- +3V 6,7,8,9,10,12,13,14,17,20,21,22,23,24,25,27,28,29,30,33,38,39

**FDI disable (DIS only stuff)**

DEL

FDI\_FSYNC can gang all these 4 signals together and tie them with only one 1K resistor to GND (DG V0.5 Ch2.2.9).

**PEG x16 disable (UMA only remove)**

C_PEG_TX0	C483	0.1u/10V_4	PEG_TX0	C_PEG_TX#0	C488	0.1u/10V_4	PEG_TX#0
C_PEG_TX1	C489	0.1u/10V_4	PEG_TX1	C_PEG_TX#1	C490	0.1u/10V_4	PEG_TX#1
C_PEG_TX2	C492	0.1u/10V_4	PEG_TX2	C_PEG_TX#2	C496	0.1u/10V_4	PEG_TX#2
C_PEG_TX3	C498	0.1u/10V_4	PEG_TX3	C_PEG_TX#3	C500	0.1u/10V_4	PEG_TX#3
C_PEG_TX4	C501	0.1u/10V_4	PEG_TX4	C_PEG_TX#4	C503	0.1u/10V_4	PEG_TX#4
C_PEG_TX5	C504	0.1u/10V_4	PEG_TX5	C_PEG_TX#5	C507	0.1u/10V_4	PEG_TX#5
C_PEG_TX6	C508	0.1u/10V_4	PEG_TX6	C_PEG_TX#6	C511	0.1u/10V_4	PEG_TX#6
C_PEG_TX7	C512	0.1u/10V_4	PEG_TX7	C_PEG_TX#7	C517	0.1u/10V_4	PEG_TX#7

0.22uF AC coupling Caps for PCIE GEN1/2/3

**Embedded Display PLL Clock**

DEL

Ra	Rb	Rc
DIS	NC	Stuff
SG/UMA	Stuff	NC

**DP & PEG Compensation**

eDP\_COMP and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

PEG\_ICOMPI and RCOMPO signals should be routed within 500 mils typical impedance = 43 mohms PEG\_ICOMPO signals should be routed within 500 mils typical impedance = 14.5 mohms

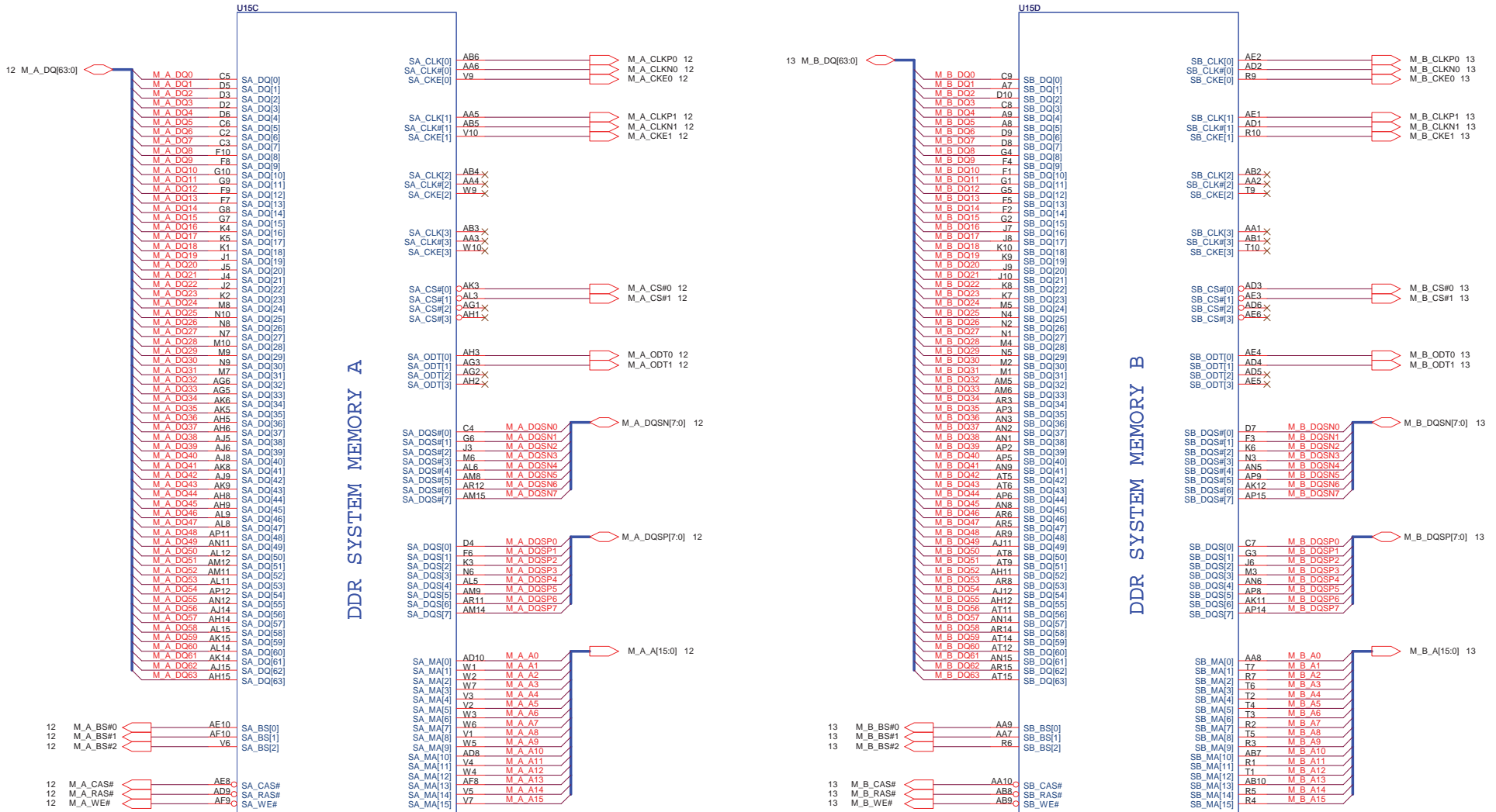
**Processor pull-up (CPU)**

**PROJECT : R13**  
Quanta Computer Inc.

Size Custom Document Number SNB 1/4 (PCIE&DMI&FDI) Rev 3A  
Date: Saturday, September 18, 2010 Sheet 2 of 39



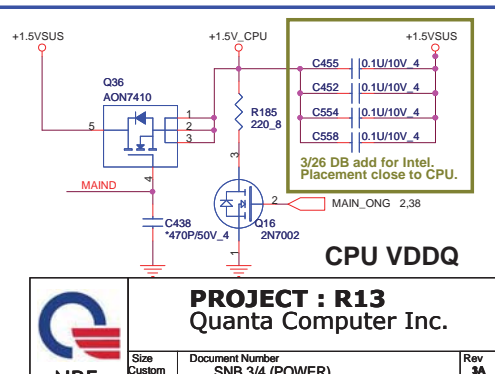
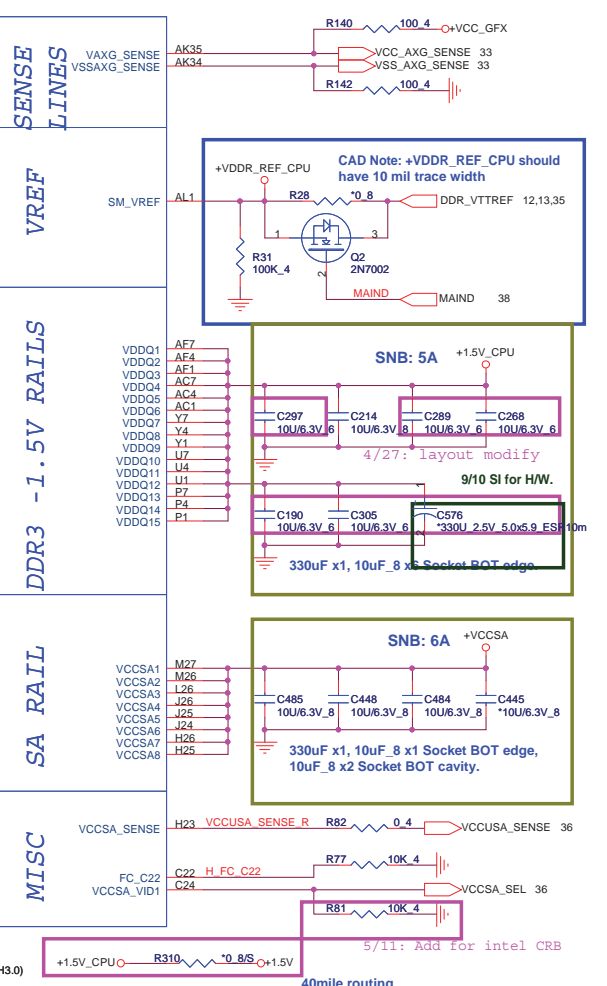
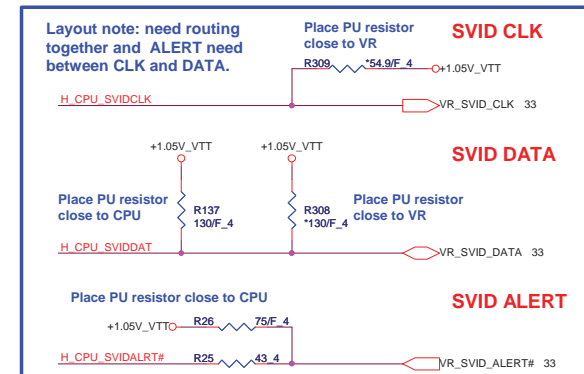
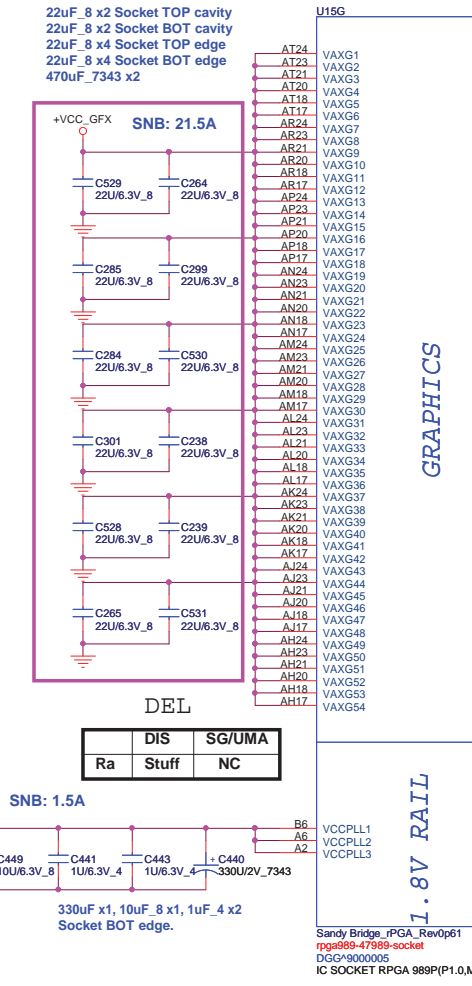
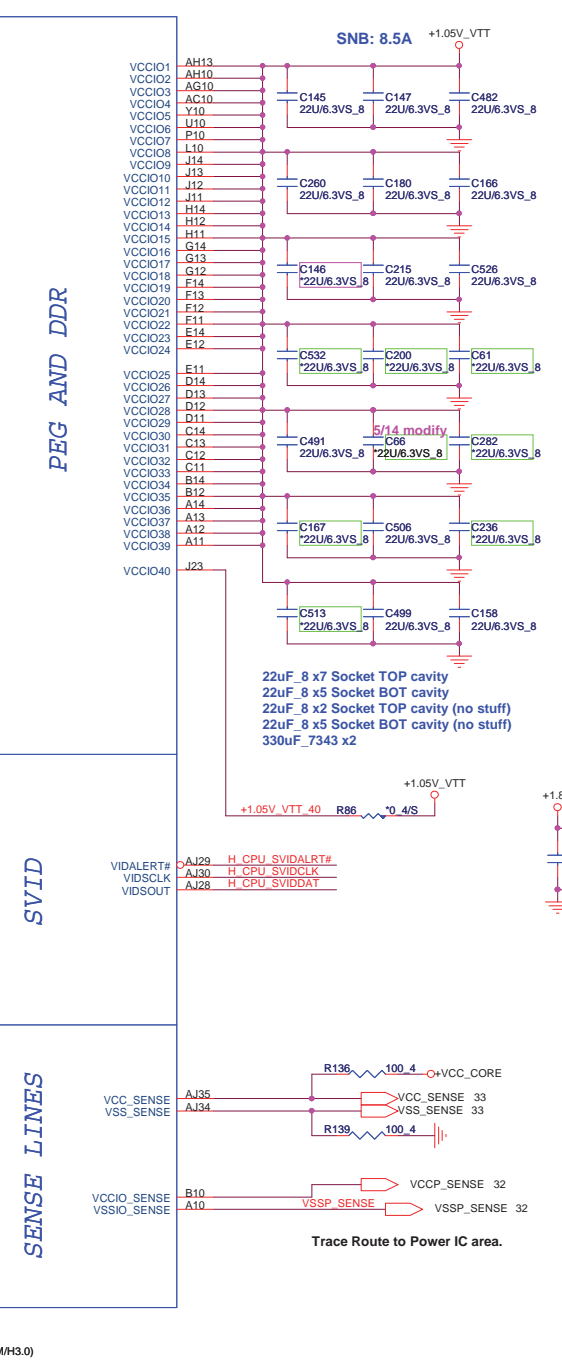
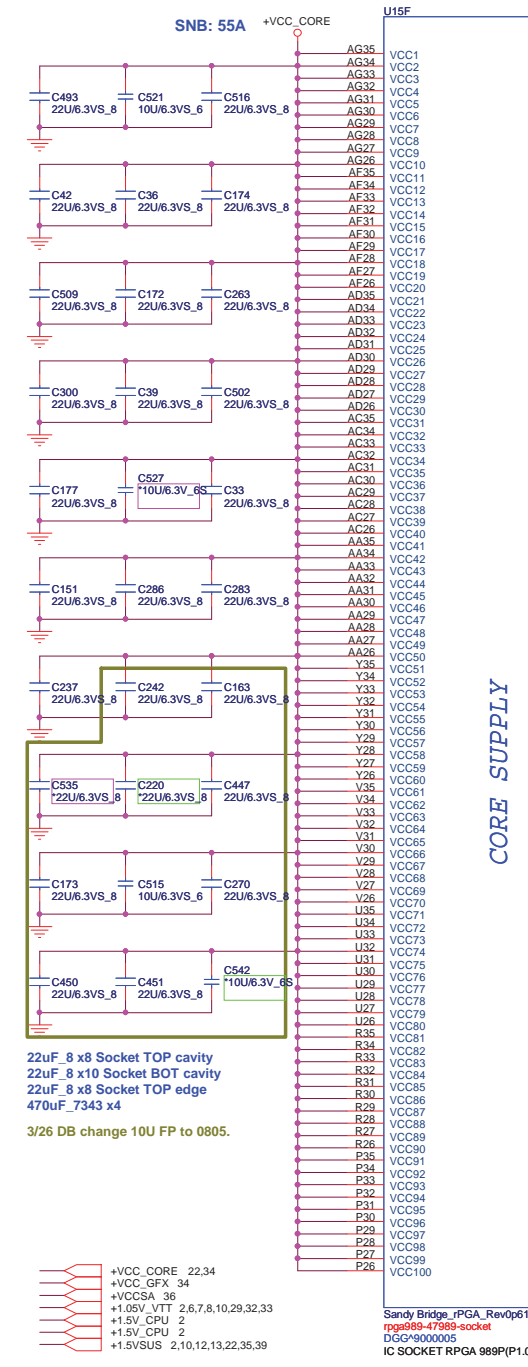
# Sandy Bridge Processor (DDR3)



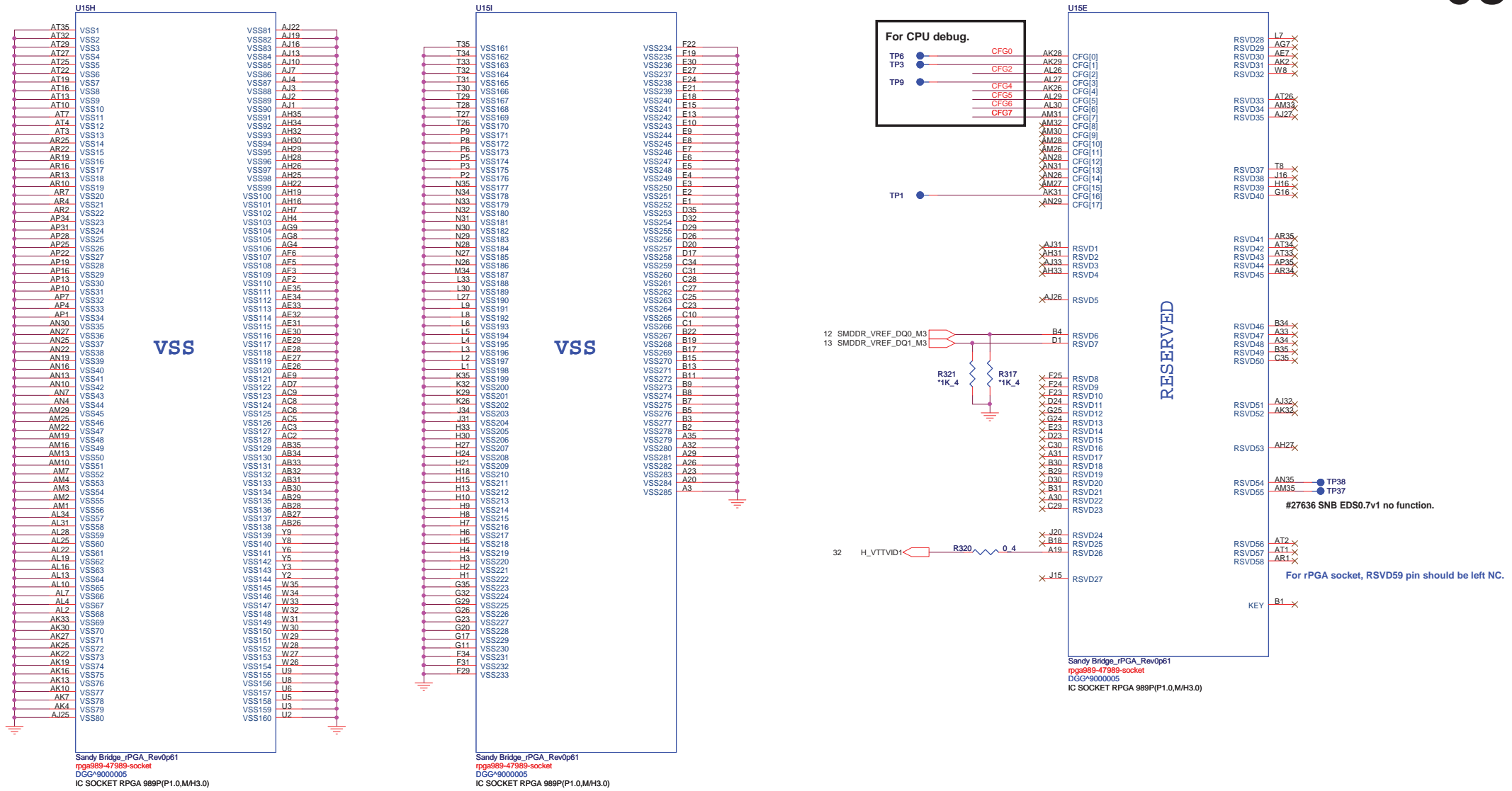
Sandy Bridge\_rPGA\_Rev0p61  
 rpg989-47989-socket  
 DGG-9000005  
 IC SOCKET RPGA 989P(P1.0,M/H3.0)

Sandy Bridge\_rPGA\_Rev0p61  
 rpg989-47989-socket  
 DGG-9000005  
 IC SOCKET RPGA 989P(P1.0,M/H3.0)

	<b>PROJECT : R13</b>		Rev <b>3A</b>
	Quanta Computer Inc.		
	Size Custom	Document Number SNB 2/4 (DDR3 I/F)	
Sheet 3 of 39			



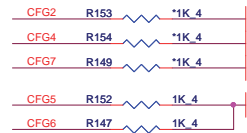




**Processor Strapping**

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training

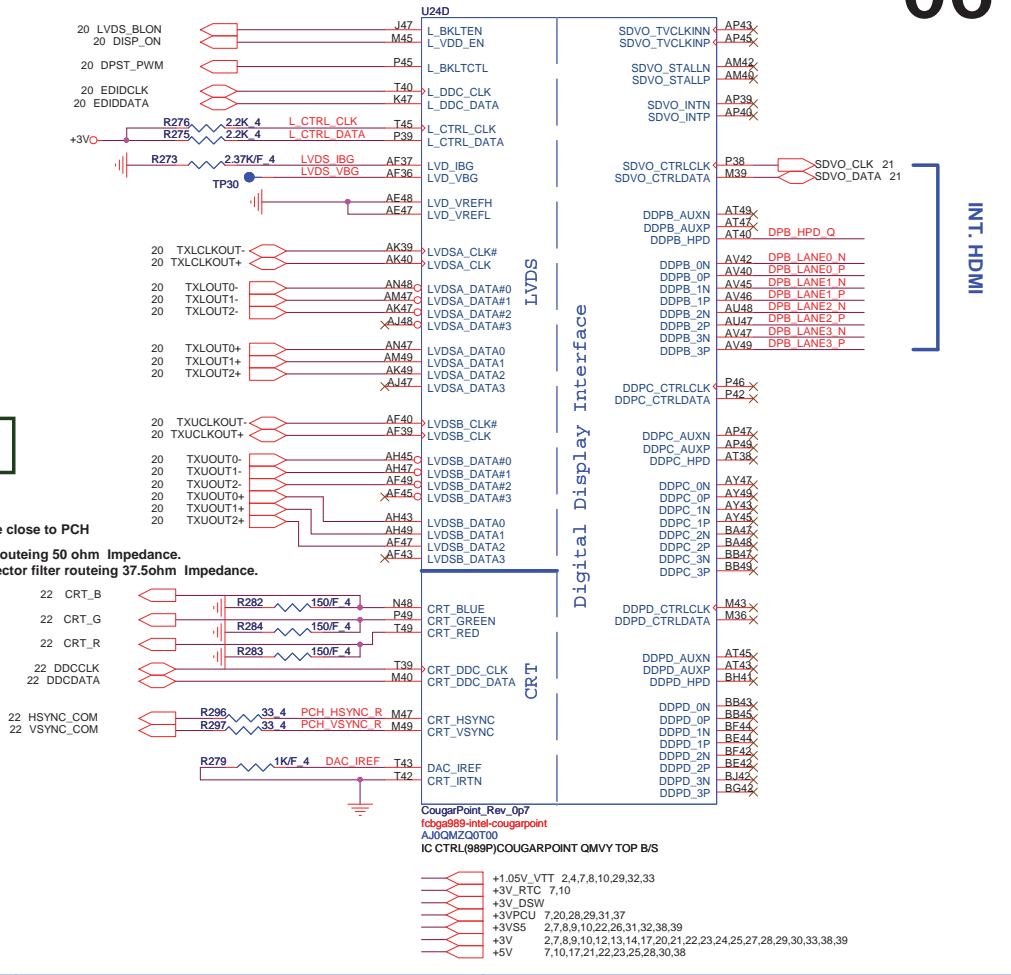
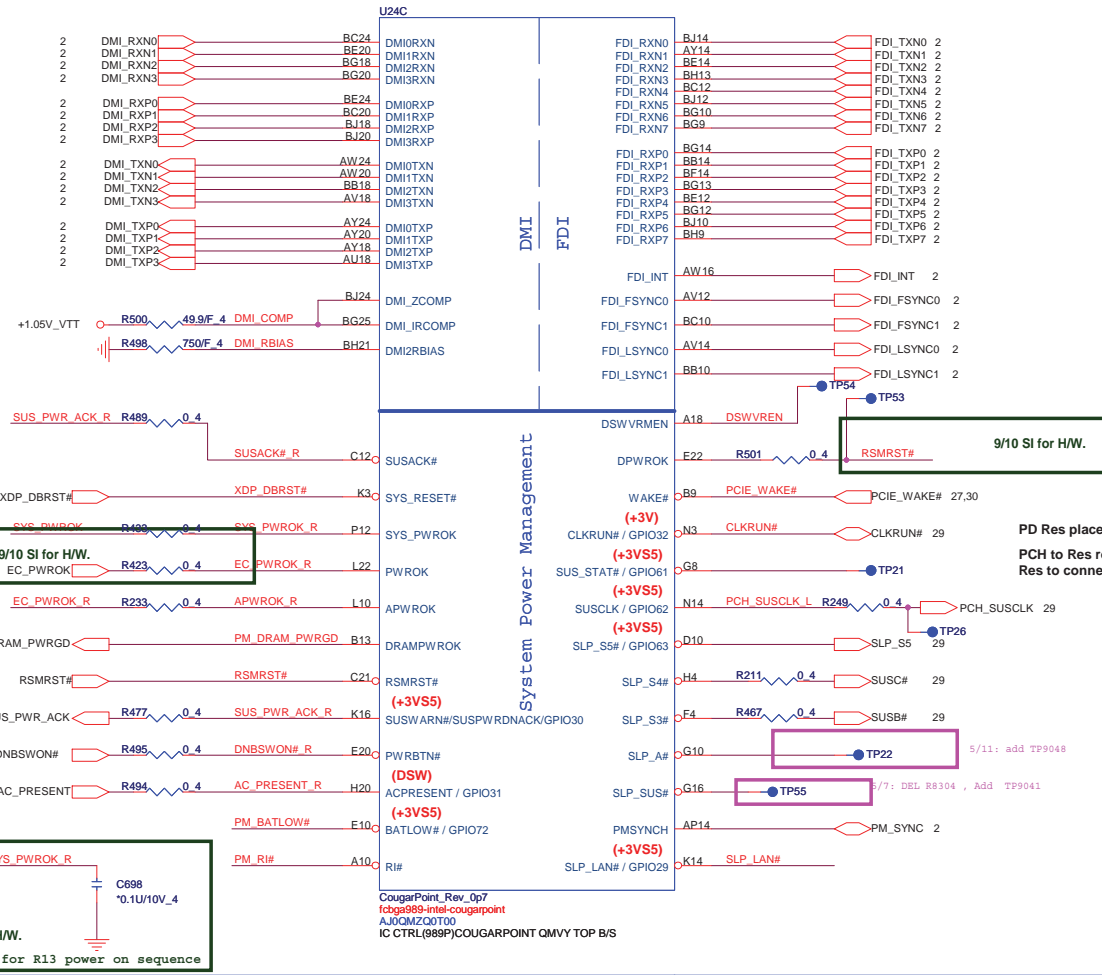


**CFG[6:5] (PCIe Port Bifurcation Straps)**

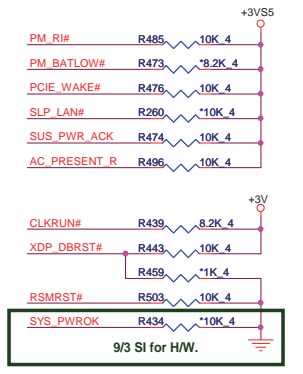
11: (Default) x16 - Device 1 functions 1 and 2 disabled  
 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled  
 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)  
 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

**PROJECT : R13**  
Quanta Computer Inc.

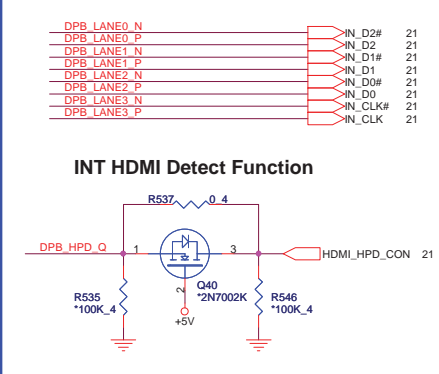
Size Custom	Document Number SNB 4/4 (GND)	Rev 3A
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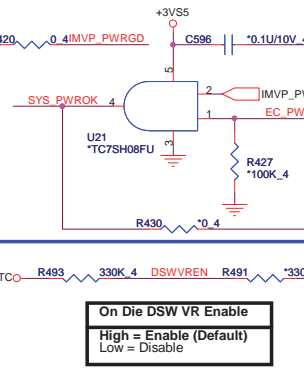
PCH Pull-high/low(CLG)



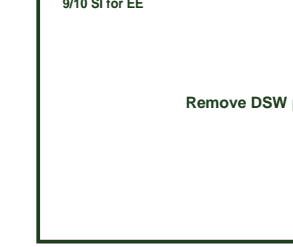
INT HDMI disable (DIS only remove)



System PWR\_OK(CLG)



DPWROK FOR DSW

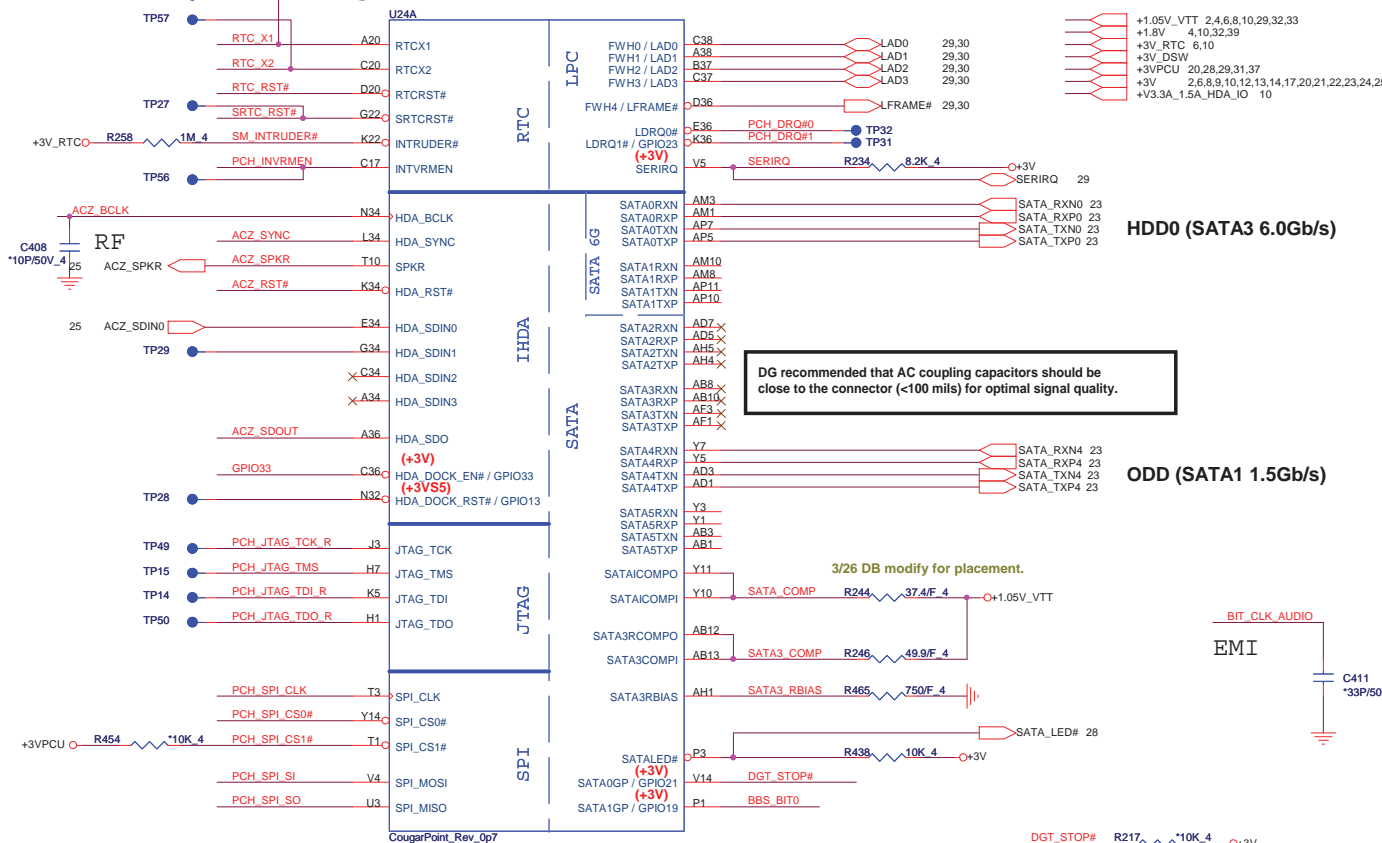


On Die DSW VR Enable  
High = Enable (Default)  
Low = Disable

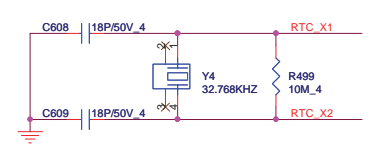
**PROJECT : R13**  
**Quanta Computer Inc.**

Size Custom Document Number PCH 1/6 (DMI/FDI/VIDEO) Rev 3A  
Date: Saturday, September 18, 2010 Sheet 6 of 39

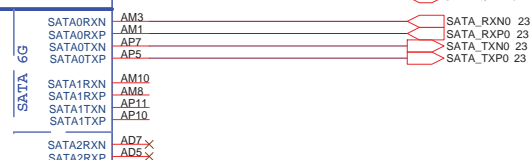
### Cougar Point (HDA, JTAG, SATA)



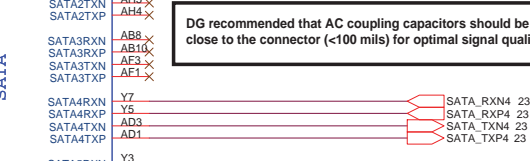
### RTC Clock 32.768KHz



### HDD0 (SATA3 6.0Gb/s)

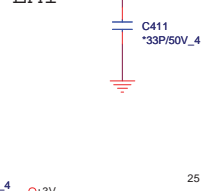


### ODD (SATA1 1.5Gb/s)

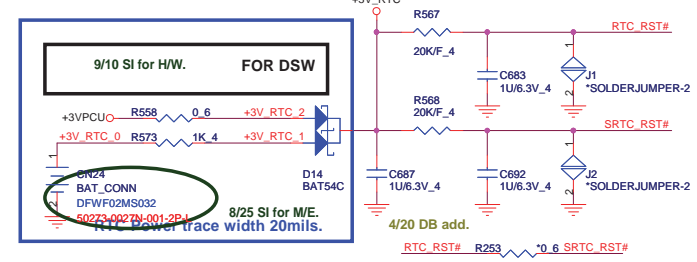


DG recommended that AC coupling capacitors should be close to the connector (<100 mils) for optimal signal quality.

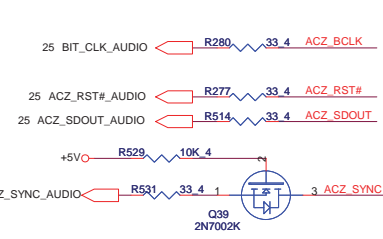
### EMI



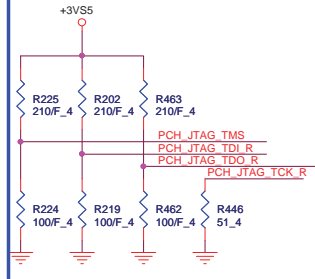
### RTC Circuitry(RTC)



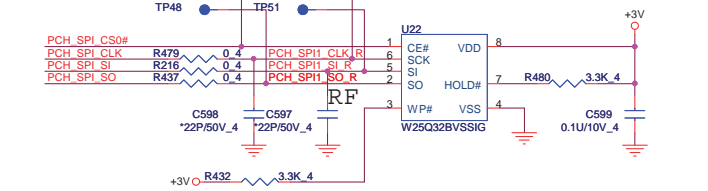
### HDA Bus(CLG)



### PCH JTAG Debug(CLG)



### PCH SPI ROM(CLG)



### PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	Circuit
SPKR	Different from Calpella No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	ACZ_SPKR R435 *1K_4 +3V
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R522 *1K_4 R521 10K_4 +3V
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	PCH_INVRMEN R497 330K_4 +3V_RTC
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security Only for Interposer	PWROK	0 = Override 1 = Default (weak pull-up 20K)	GPIO33 R508 1K_4 GPIO33_E 29
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	[Need external pull-down for LPC BIOS] Default weak pull-up on GNT0/1#	R455 *1K_4 R523 *1K_4 BBS_BIT0
GPIO19	Different from Calpella Boot BIOS Selection 0 [bit-0]	PWROK		BBS_BIT1 8
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN
NV_ALE	Intel Anti-Theft HDD protection Only for Interposer	PWROK	0 = Disable (Internal pull-down 20kohm)	+1.8V R468 *1K_4 NV_ALE 8
NV_CLE	DMI Termination voltage	PWROK	weak pull-down 20kohm	+1.8V R470 2.2K_4 R469 4.7K_4 NV_CLE 8 N.A at CPT EDS 0.7 H_SNB_IVB# 2
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	+3V5 R278 1K_4 ACZ_SYNC
HDA_SDO	Flash Descriptor Security	PWROK	0 = Override 1 = Default (weak pull-up 20K)	ACZ_SDOUD R510 *1K_4 +V3.3A_1.5A_HDA_IO
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)	R483 *1K_4 ICC_EN# 9
GPIO28	Different from Calpella On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	R447 *1K_4 PLL_OVDV_EN 9
SPI_MOSI	iTPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable	PCH_SPI_SI R198 1K_4 +3V

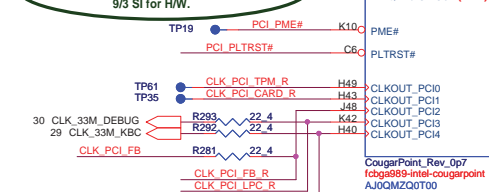
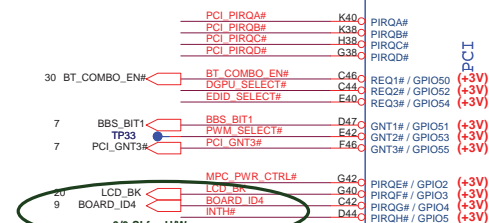
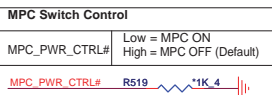
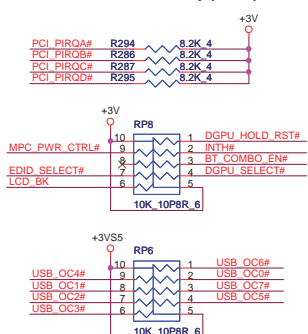
Vender	Size	P/N
EON	4MB	AKE39FN0Q00 (EN25F32-100HIP)
Winbond	4MB	AKE391P0N00 (W25Q32BVSSIG)
Socket		DG008000031



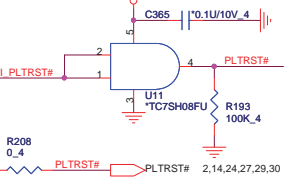
**PROJECT : R13**  
**Quanta Computer Inc.**

Size Custom Document Number PCH 2/6 (SATA/HDA/SPI) Rev 3A  
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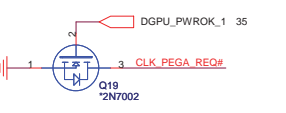
PCI/USB# Pull-up(CLG)



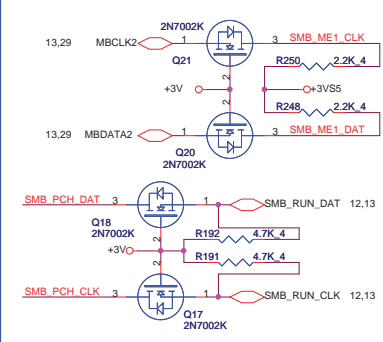
PLTRST#(CLG)



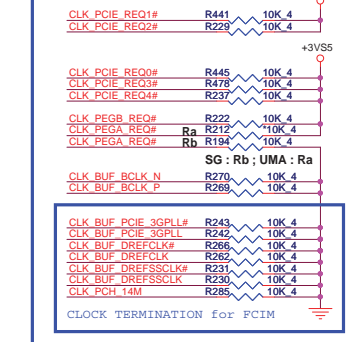
PEG Clock detect (SG only)



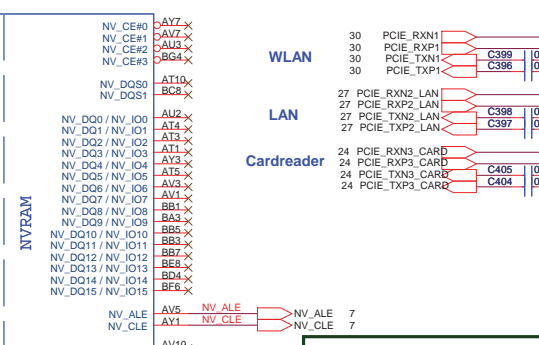
SMBus/Pull-up(CLG)



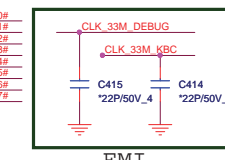
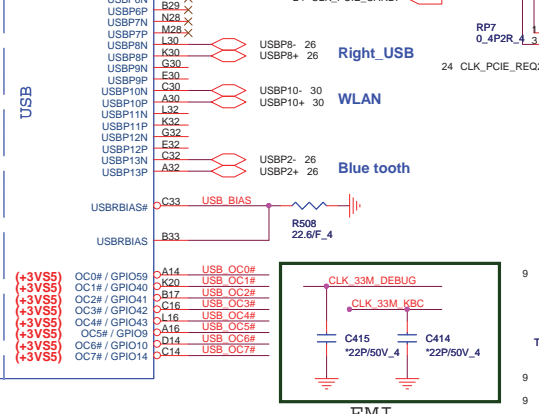
CLK\_REQ/Strap Pin(CLG)



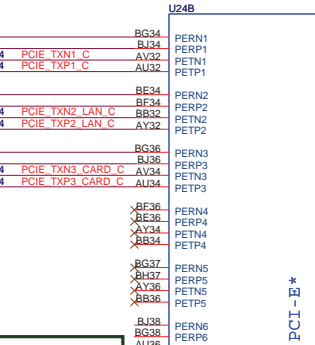
NVRAM



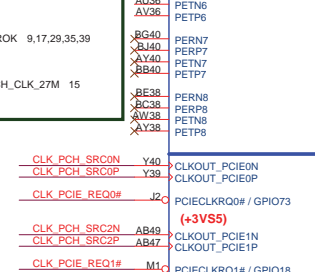
PCI



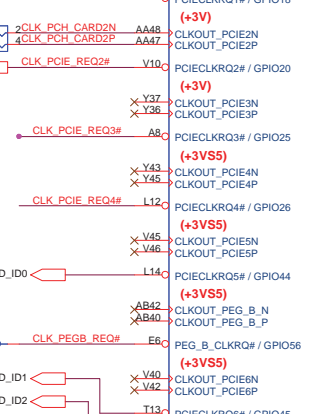
LAN



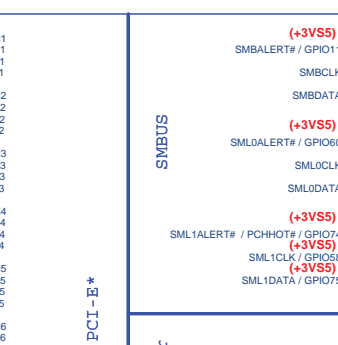
WLAN



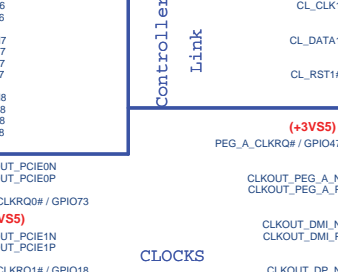
Cardreader



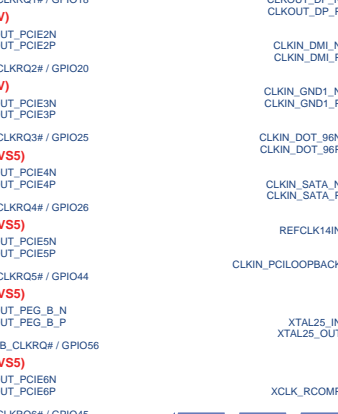
WLAN



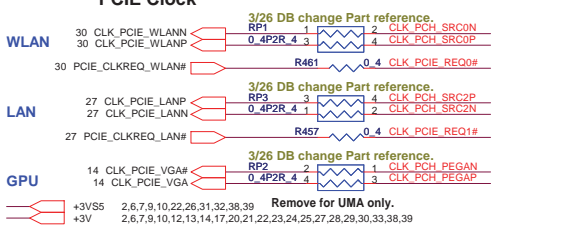
LAN



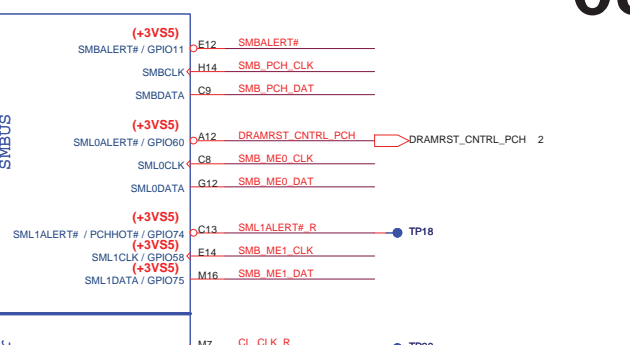
GPU



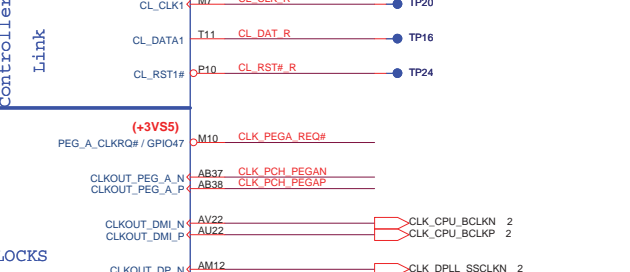
PCI-E Clock



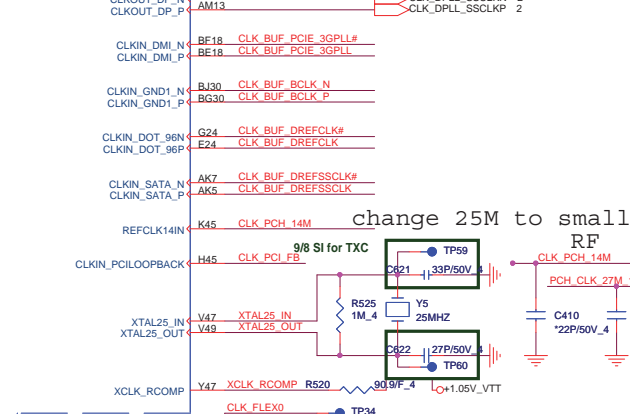
SMBUS



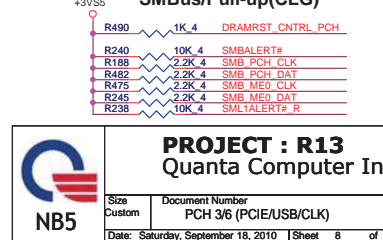
Controller Link



CLOCKS

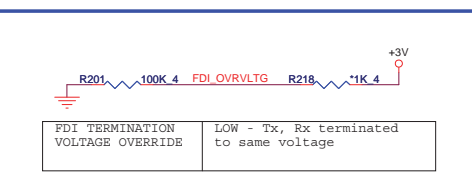
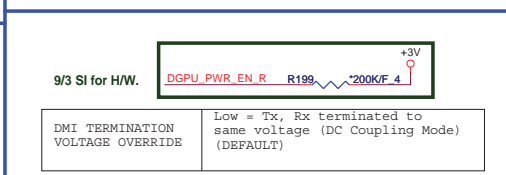
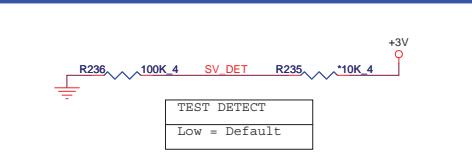
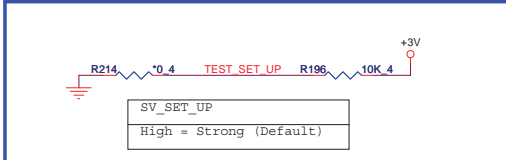
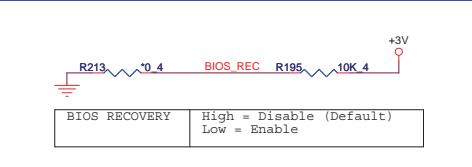
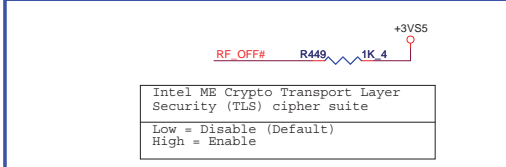
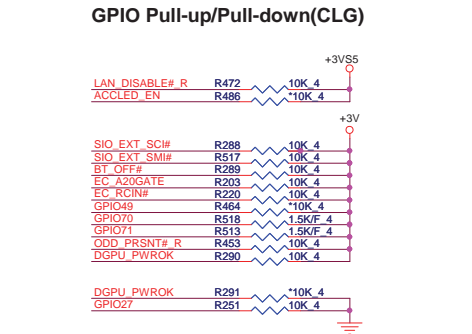
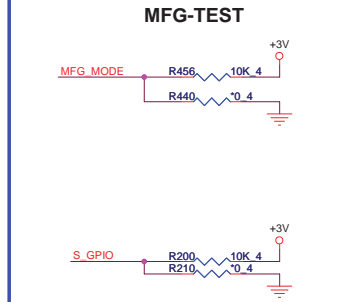
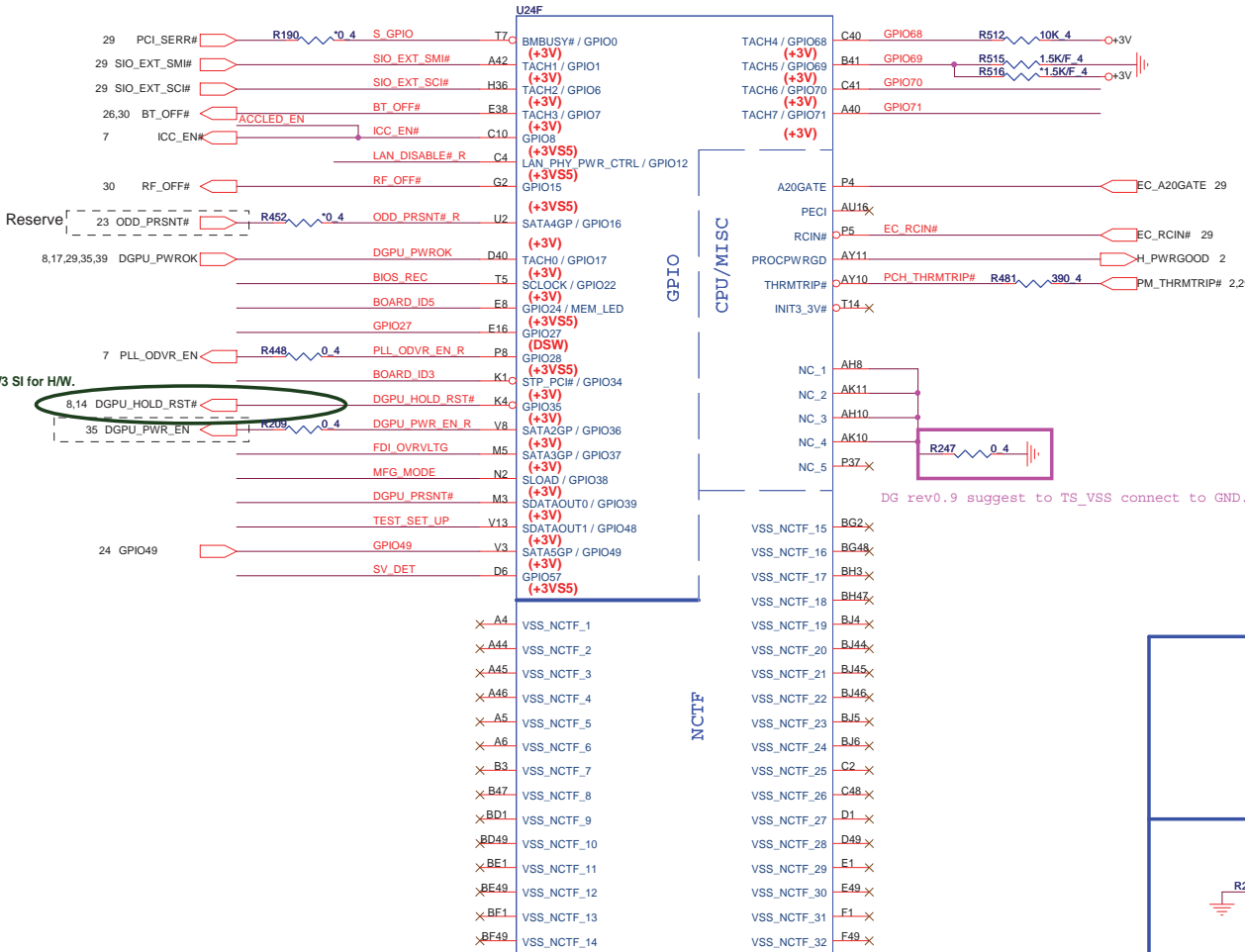


SMBus/Pull-up(CLG)



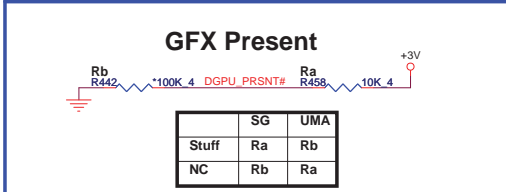
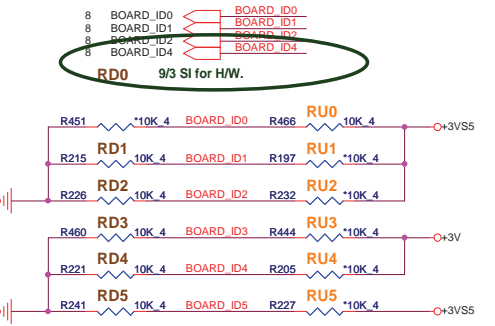
PROJECT : R13 Quanta Computer Inc. Size Custom Document Number PCH 3/6 (PCI/USB/CLK) Rev 3A Date: Saturday, September 18, 2010 Sheet 8 of 39





**BOARD ID SETTING**

Model	BOARD_ID5	BOARD_ID4	BOARD_ID3	BOARD_ID2	BOARD_ID1	BOARD_ID0
R13 UMA	0	0	0	0	0	0
R13 DIS	0	0	0	0	0	1
	0	0	0	0	0	0
	0	0	0	0	0	0
	0	0	0	0	0	0

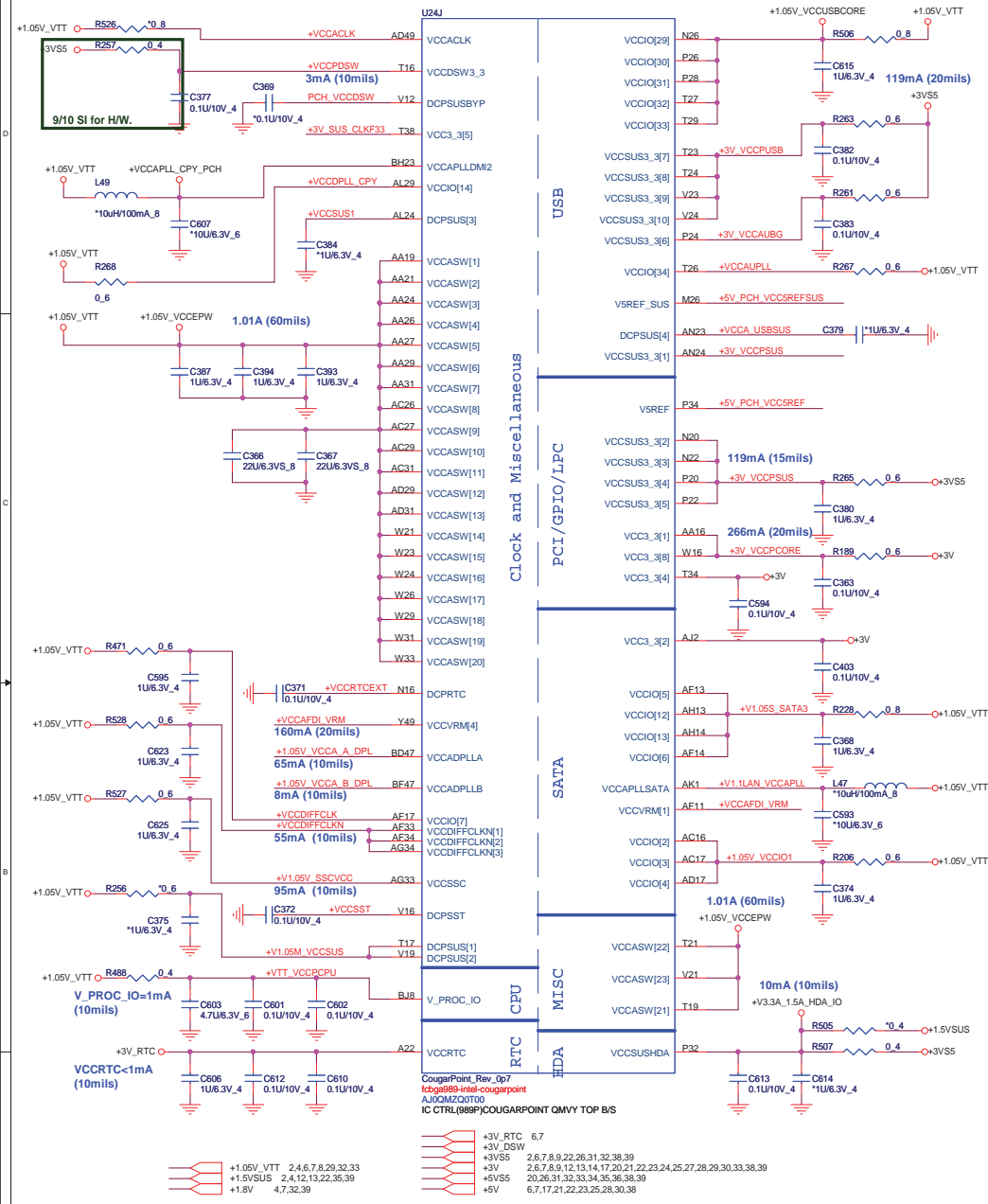


**PROJECT : R13**  
 Quanta Computer Inc.

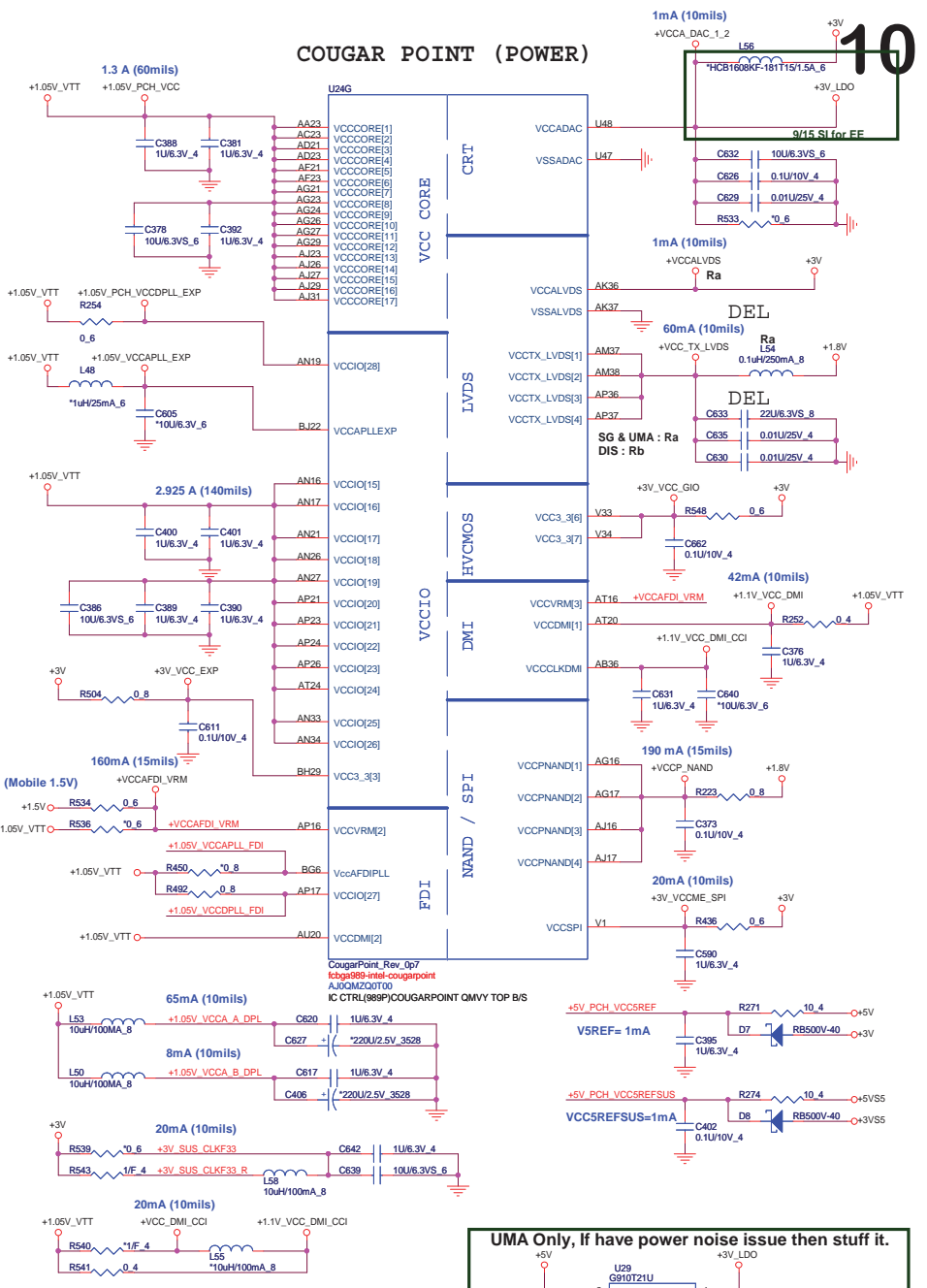
NBS

Size Custom Document Number PCH 4/6 (GPIO/MISC) Rev 3A  
 Date: Saturday, September 18, 2010 Sheet 9 of 39

# Cougar Point-M (POWER)

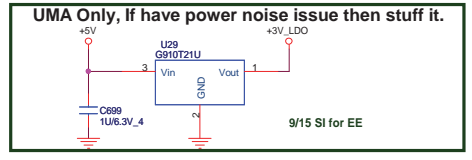


# COUGAR POINT (POWER)



10

+3V_RTC	6,7
+3V_DSWS	2,6,7,8,9,22,26,31,32,38,39
+3V_S5	2,6,7,8,9,12,13,14,17,20,21,22,23,24,25,27,28,29,30,33,38,39
+3V	2,6,7,8,9,12,13,14,17,20,21,22,23,24,25,27,28,29,30,33,38,39
+3V_S5	20,29,31,32,33,34,35,36,38,39
+1.8V	4,7,32,39

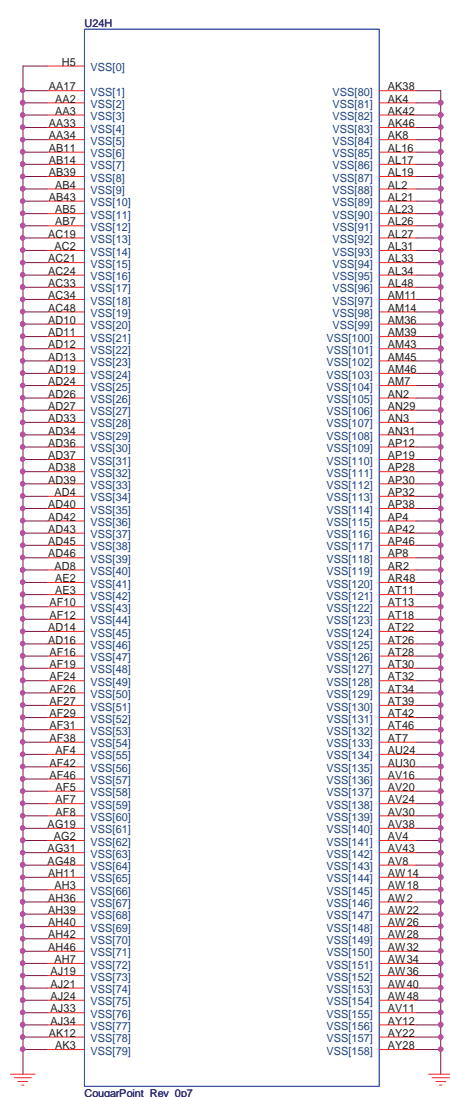
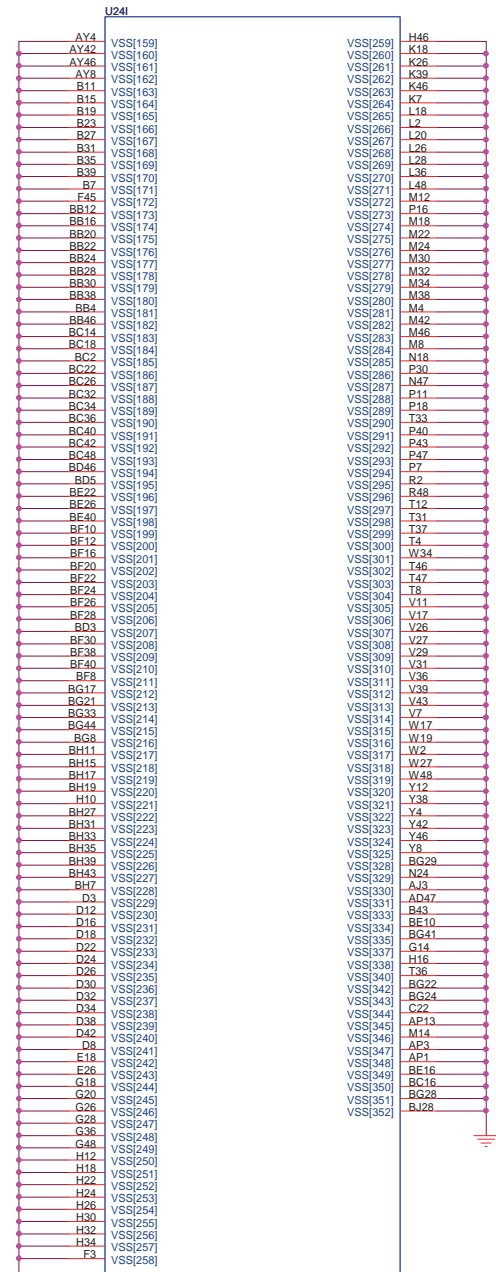



**PROJECT : R13**  
Quanta Computer Inc.

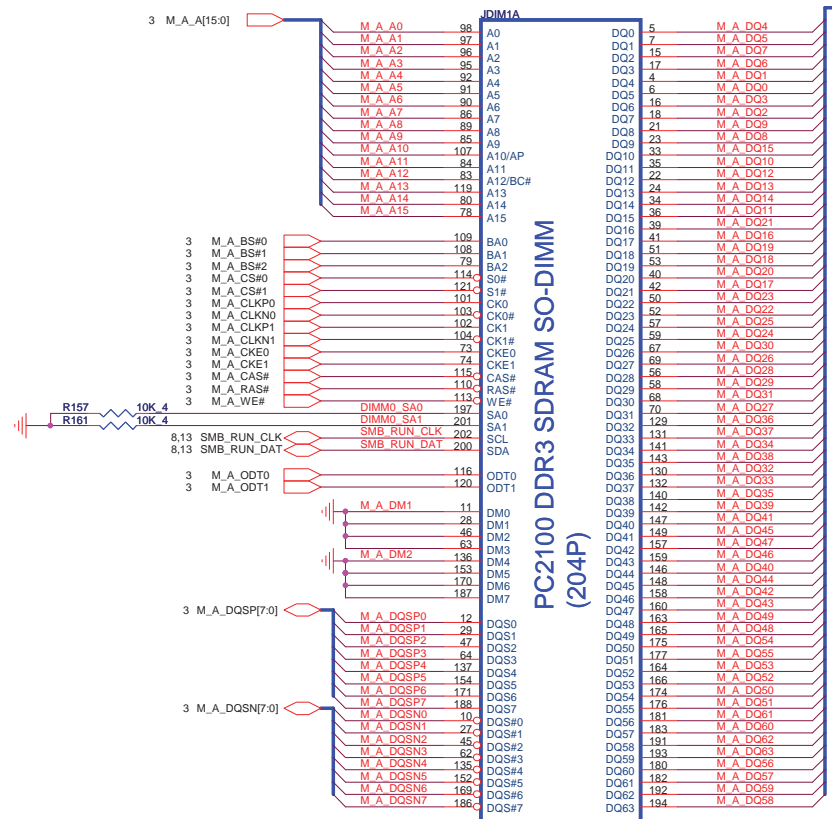
Size Custom	Document Number PCH 5/6 (POWER)	Rev 3A
Date: Saturday, September 18, 2010   Sheet 10 of 39		

IBEX PEAK-M (GND)

IBEX PEAK-M (GND)

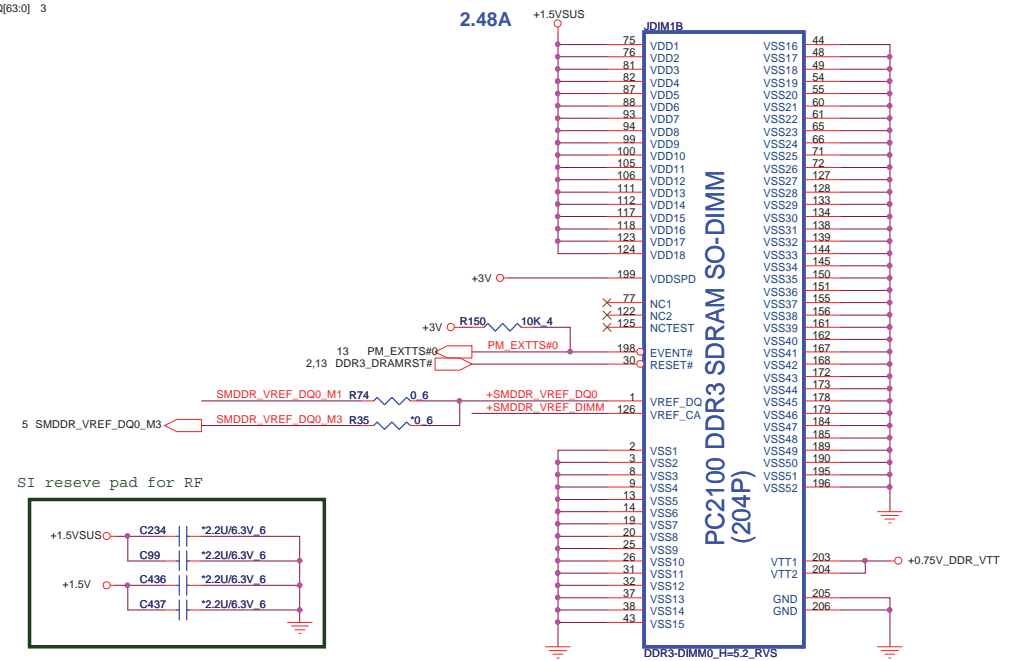


	<b>PROJECT : R13</b>		
	Quanta Computer Inc.		
	Size Custom	Document Number PCH 6/6 (GND)	Rev 3A
Date: Saturday, September 18, 2010   Sheet 11 of 39			



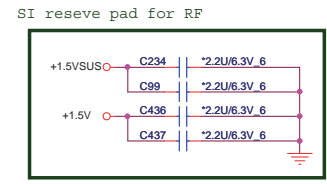
**PC2100 DDR3 SDRAM SO-DIMM (204P)**

DDR3-DIMM0\_H=5.2\_RVS  
 DDR-78279-001-RVS-204P  
 DGMK4000125  
 IC SOCKET DDRIII SO-DIMM(204P,H5.2,RVS)



**PC2100 DDR3 SDRAM SO-DIMM (204P)**

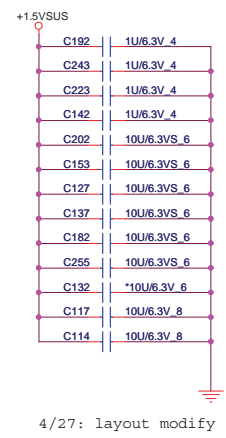
DDR3-DIMM0\_H=5.2\_RVS  
 DDR-78279-001-RVS-204P  
 DGMK4000125  
 IC SOCKET DDRIII SO-DIMM(204P,H5.2,RVS)



- +0.75V\_DDR\_VTT 13,35,38
- +1.5VSUS 2,4,10,13,22,35,39
- +3VPCU 7,20,28,29,31,37
- +3V 2,6,7,8,9,10,13,14,17,20,21,22,23,24,25,27,28,29,30,33,38,39
- +5VPCU 29,31,37

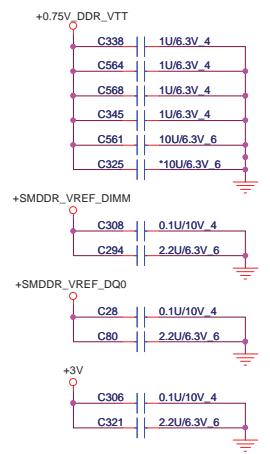
del M2 solution

**VREF DQ0 M2 Solution**

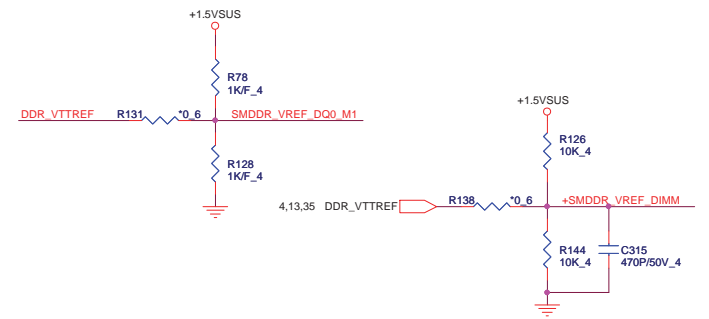


4/27: layout modify

**Place these Caps near So-Dimm0.**



**VREF DQ0 M1 Solution**

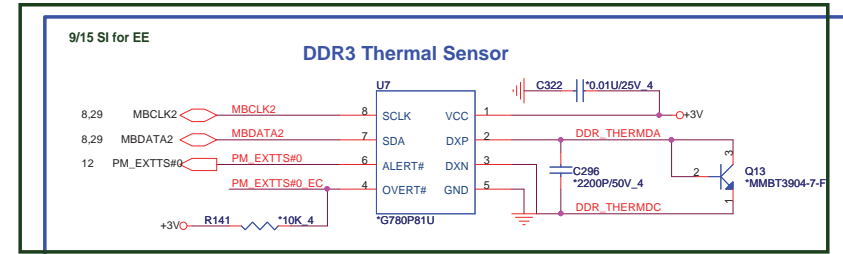
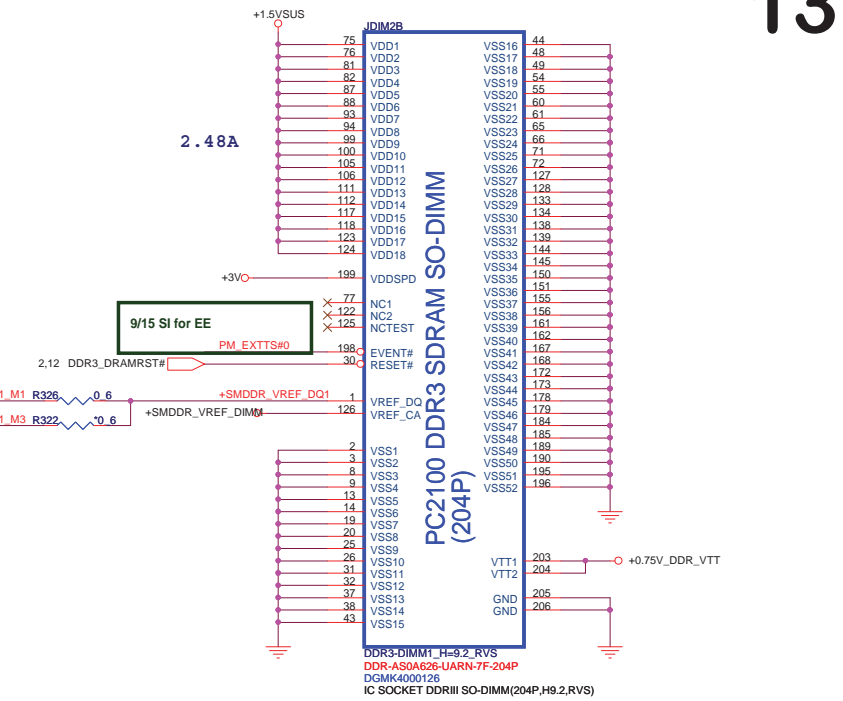
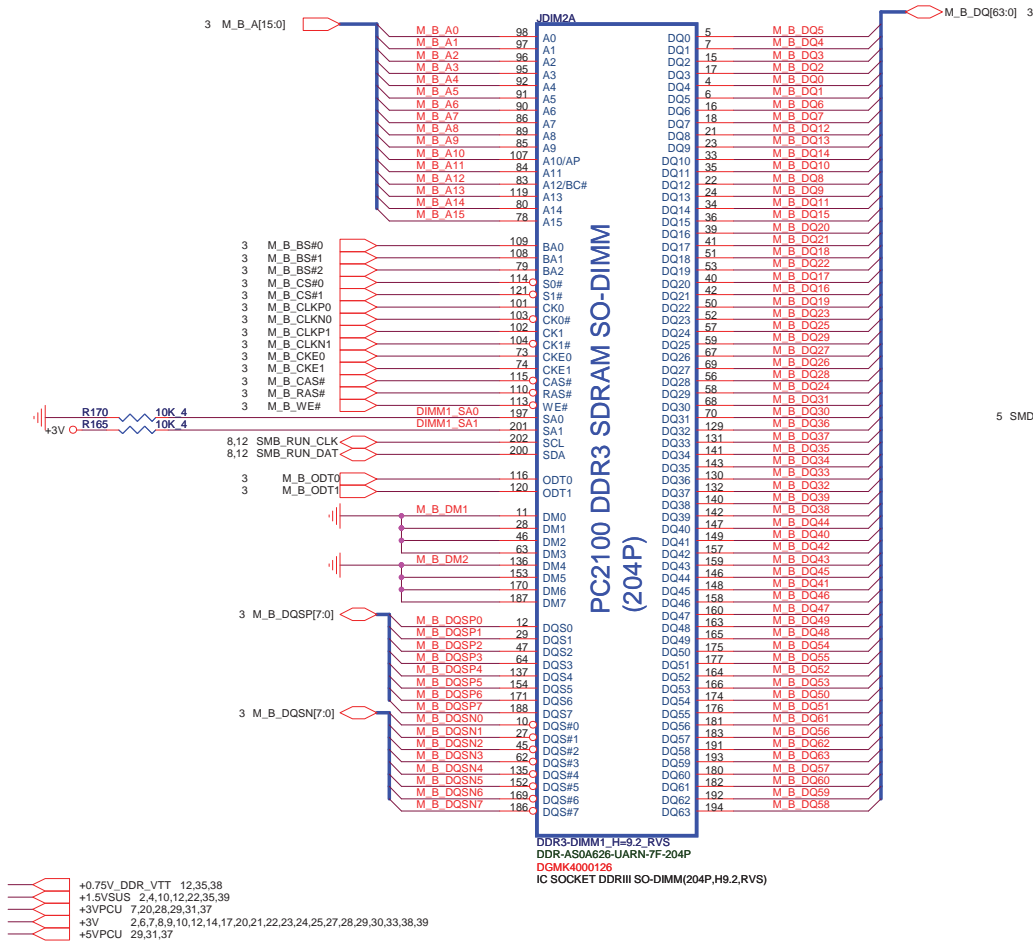


**PROJECT : R13**  
 Quanta Computer Inc.

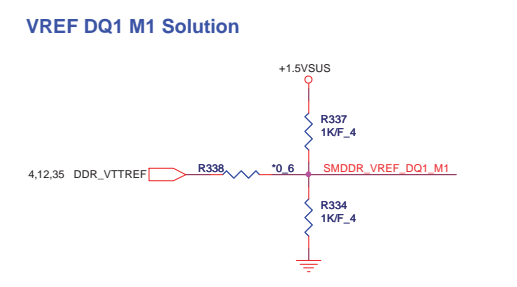
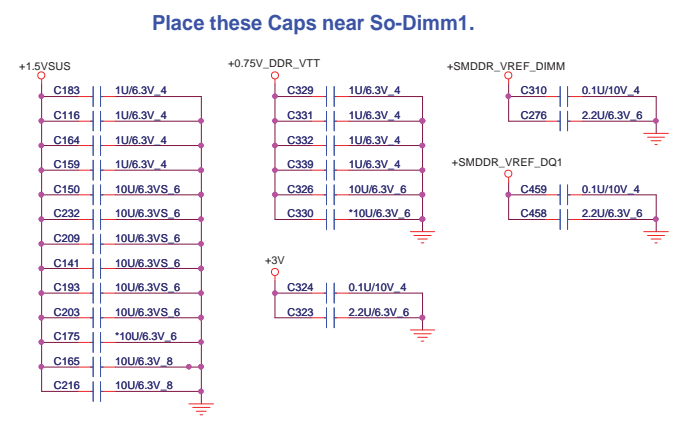
NB5

Size Custom	Document Number	Rev 3A
	DDR3 DIMM0-RVS (5.2H)	
Date: Saturday, September 18, 2010	Sheet 12	of 39





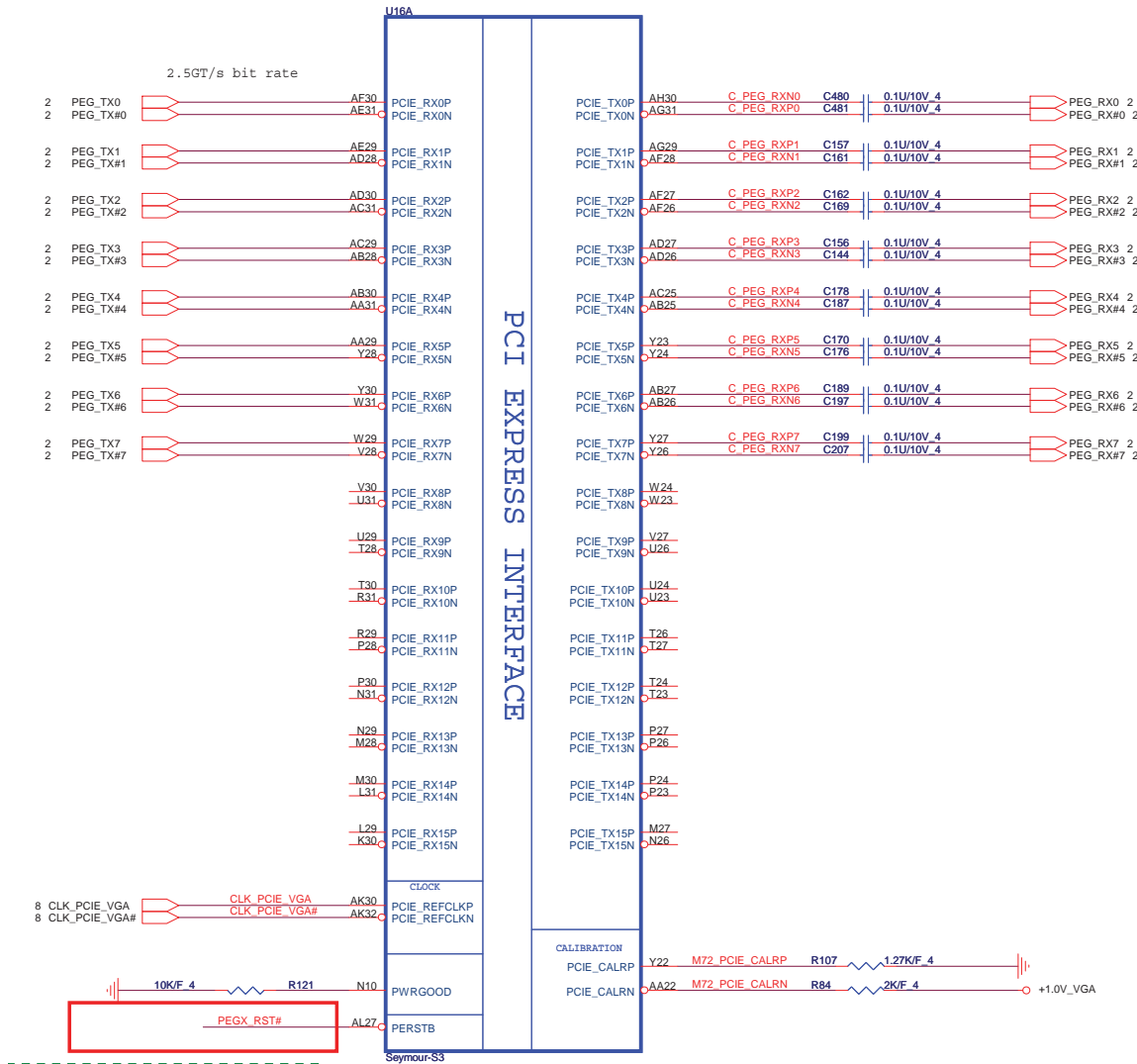
del M2 solution



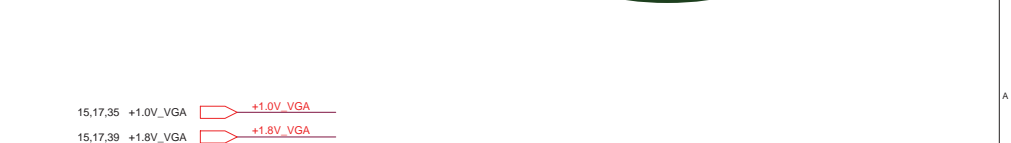
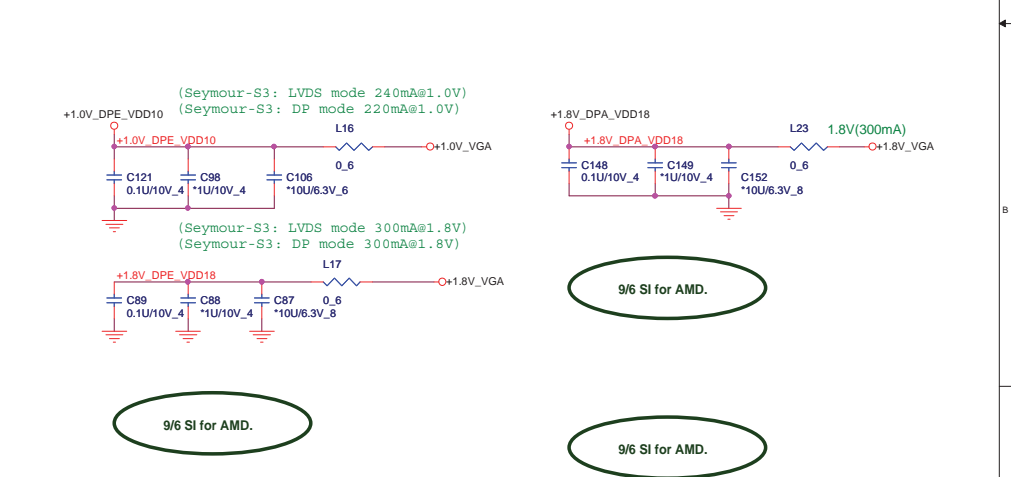
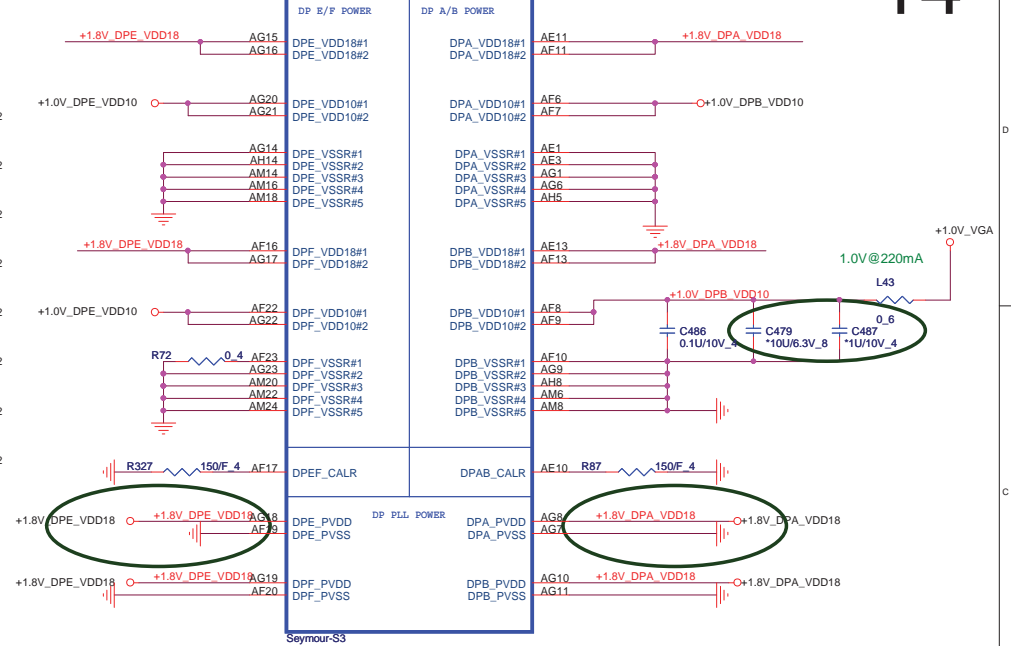
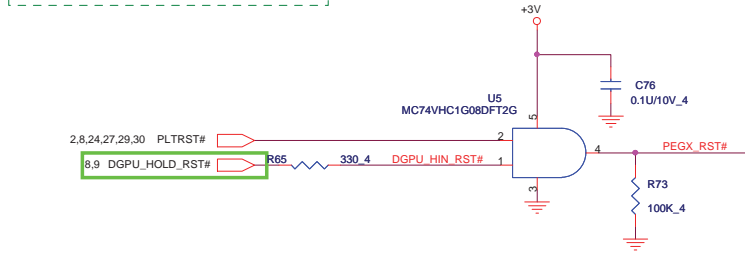
**PROJECT : R13**  
Quanta Computer Inc.

NB5

Size Custom	Document Number DDR3 DIMM1-RVS (9.2H)	Rev 3A
Date: Saturday, September 18, 2010		Sheet 13 of 39



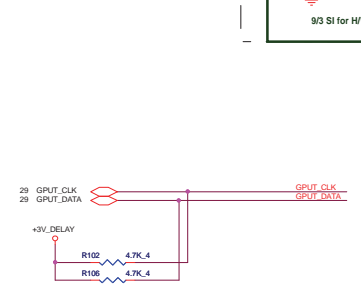
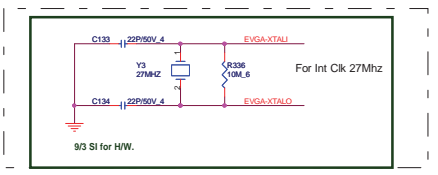
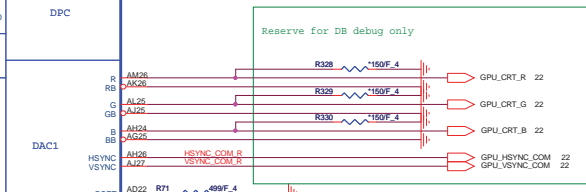
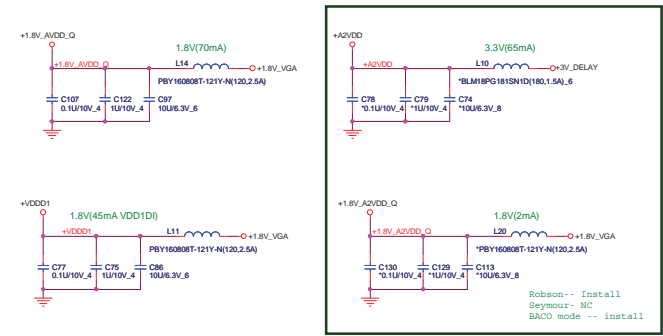
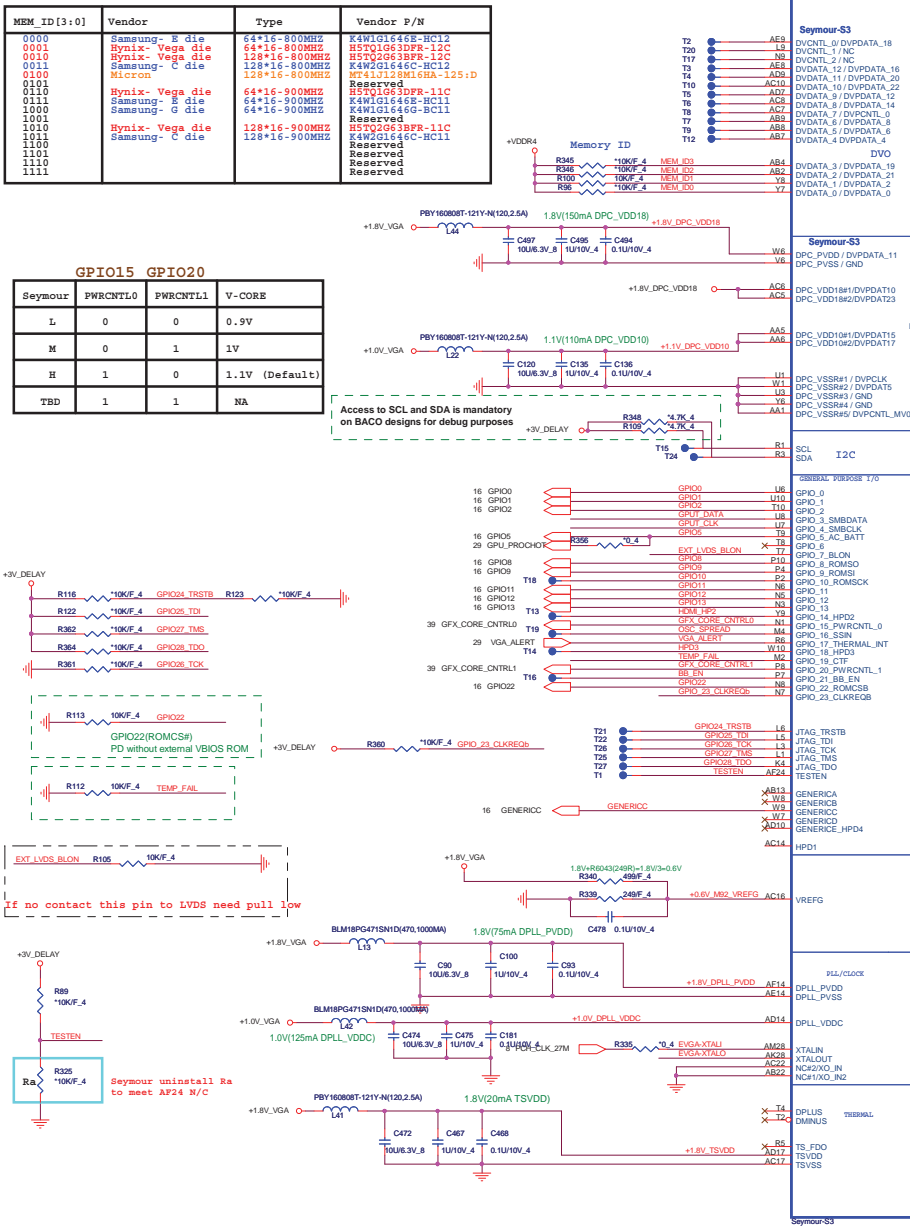
100MHz (+/-300ppm) input frequency,  
0-0.7V single-ended swing

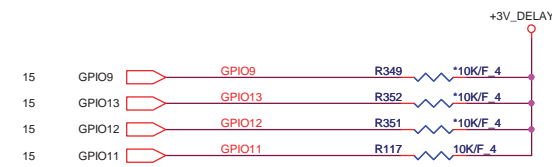
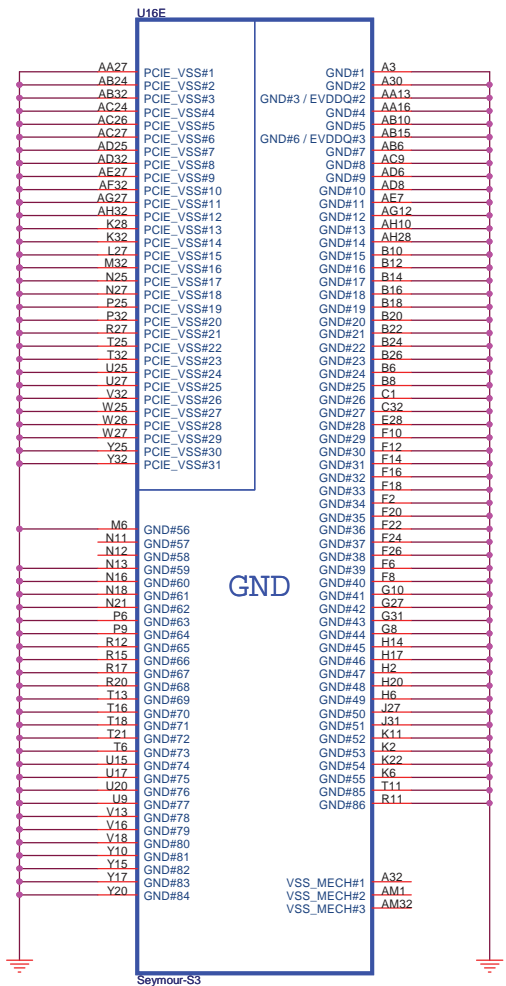


	<b>PROJECT : R13</b> <b>Quanta Computer Inc.</b>	
	Size Custom <b>NB5</b>	Document Number <b>Seymour PCIe Interface</b>
Date: Saturday, September 18, 2010   Sheet 14 of 39		

MEM_ID [3:0]	Vendor	Type	Vendor P/N
0000	Samsung- E die	64*16-800MHZ	K4W1G1646E-BC12
0001	Hynix- Vega die	64*16-800MHZ	H5TQ163DPR-12C
0010	Hynix- Vega die	128*16-800MHZ	H5TQ263BPR-12C
0011	Samsung- C die	128*16-800MHZ	K4W2G1646C-BC12
0100	Micron	128*16-800MHZ	MT44L128M16HA-125:D
0101	Reserved	Reserved	Reserved
1000	Hynix- Vega die	64*16-900MHZ	H5TQ163DPR-11C
0111	Samsung- E die	64*16-900MHZ	K4W1G1646E-BC11
1001	Samsung- G die	64*16-900MHZ	K4W1G1646G-BC11
1010	Hynix- Vega die	128*16-900MHZ	H5TQ263BPR-11C
1011	Samsung- G die	128*16-900MHZ	K4W2G1646G-BC11
1100	Reserved	Reserved	Reserved
1101	Reserved	Reserved	Reserved
1110	Reserved	Reserved	Reserved
1111	Reserved	Reserved	Reserved

GPIO15		GPIO20		V-CORE
L	0	0	0	0.9V
M	0	1	1V	1V
H	1	0	1.1V (Default)	1.1V
TBD	1	1	1	NA

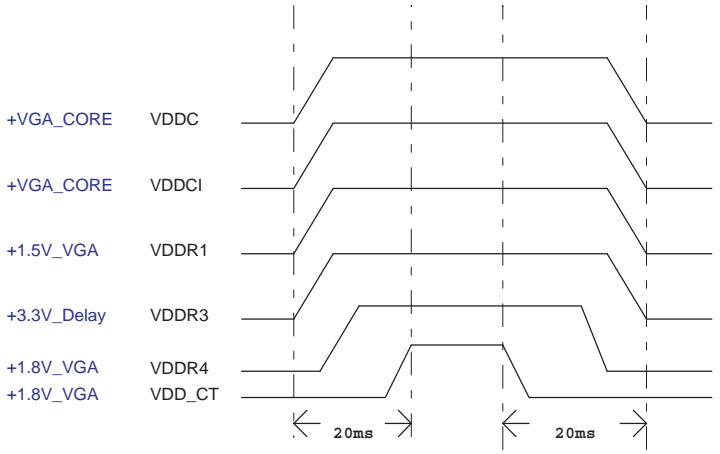




CONFIGURATION STRAPS			RECOMMENDED SETTINGS 0= DO NOT INSTALL RESISTOR 1 = INSTALL 10K RESISTOR X = DESIGN DEPENDANT NA = NOT APPLICABLE
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	<b>Transmitter Power Savings Enable</b> 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	<b>PCI Express Transmitter De-emphasis Enable</b> 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	1
BIF_GEN2_EN_A	GPIO2	Enable CLKREQ# Power Management 0 - CLKREQ# power management capability is disabled 1 - CLKREQ# power management capability is enabled	0
RSVD BIF_VGA_DIS RSVD	GPIO8 GPIO9 GPIO21	VGA ENABLED	0 0 0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
RSVD AUD[1] AUD[0]	GENERICC HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	0 0 11

AMD RESERVED CONFIGURATION STRAPS		
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET		
H2SYNC	GENERICC	
PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET		
GPIO21_BB_EN		

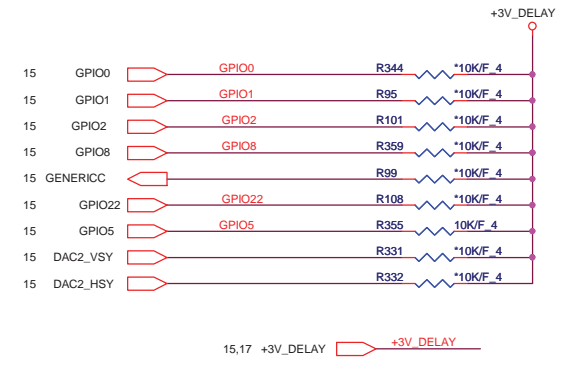
Power Up/Down Sequence



Memory Aperture size

GPIO9 BIOSROM	GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0
0	256M	0	1
0	64M	0	0
0	32M	0	1
0	512M	1	0
0	1G	1	0
0	2G	1	1
0	4G	1	1

It is a shared pin strap with CONFIG[2:0] if BIOS\_ROM\_EN is set to 0.

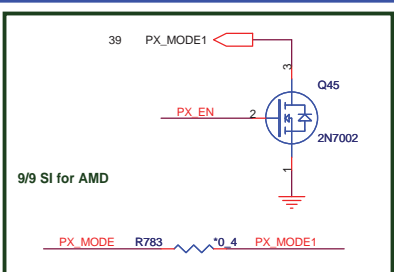
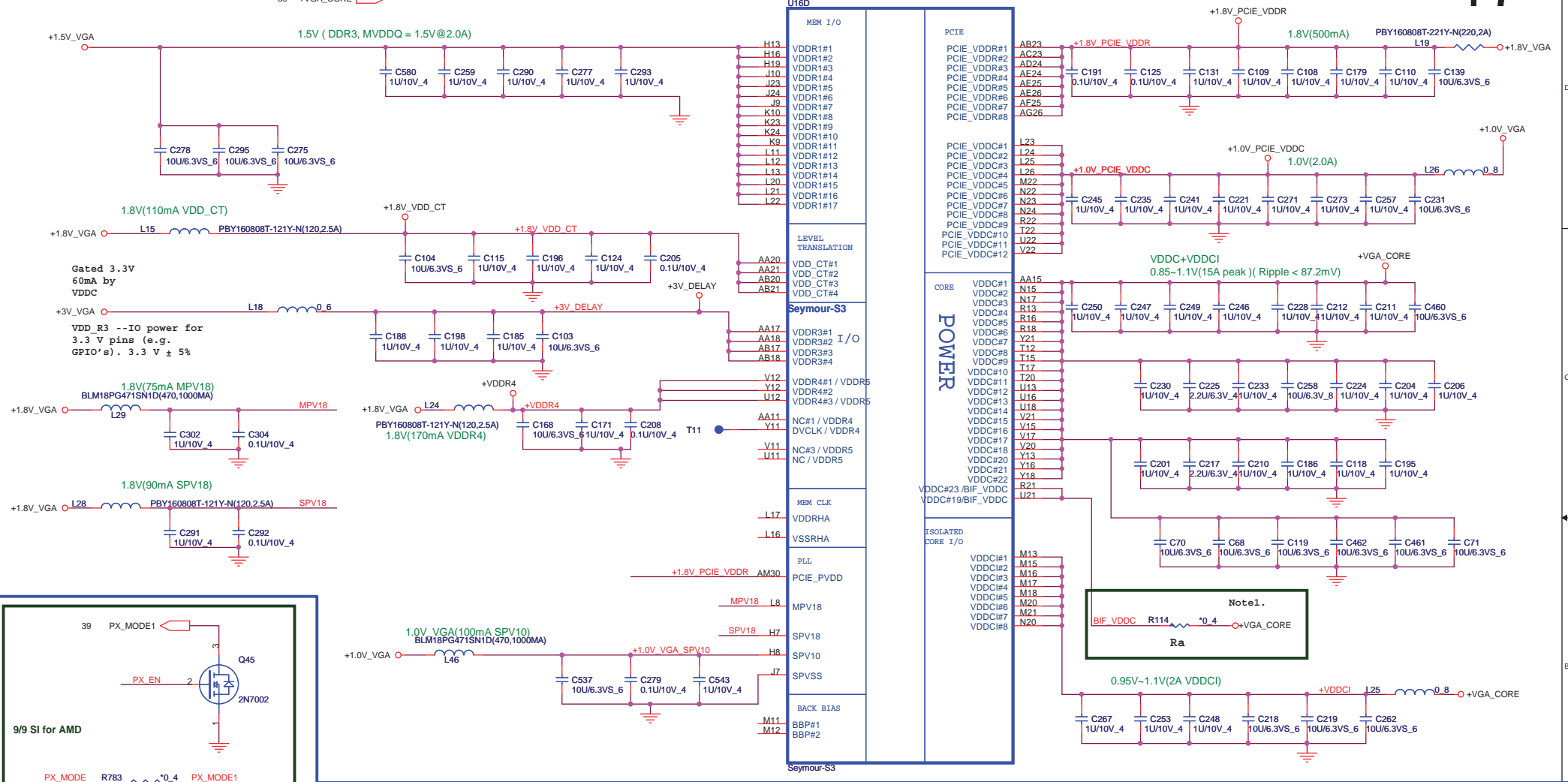


**PROJECT : R13**  
**Quanta Computer Inc.**

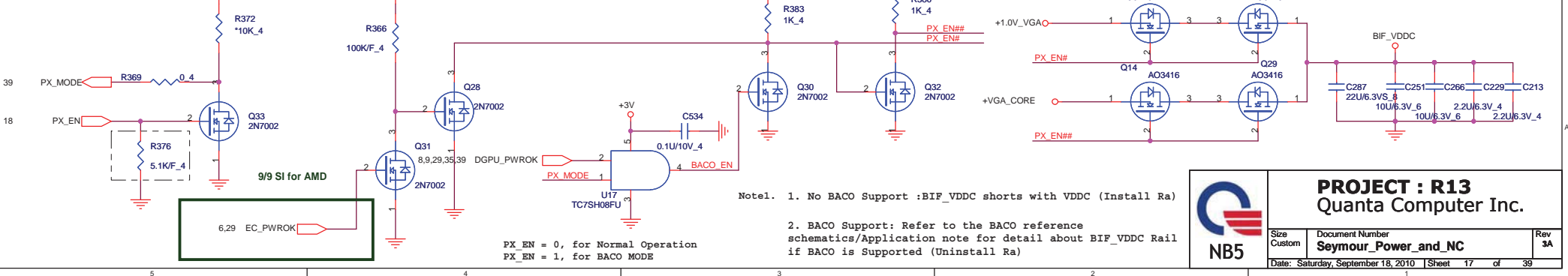
Size Custom	Document Number <b>Seymour GND / LVDS/ Straps</b>	Rev <b>3A</b>
Date: Saturday, September 18, 2010   Sheet 16 of 39		



- 6,7,10,21,22,23,25,28,30,38 +5V
- 2,6,7,8,9,10,12,13,14,20,21,22,23,24,25,27,28,29,30,33,38,39 +3V
- 14,15,35 +1.0V\_VGA
- 39 +3V\_VGA
- 39 +VGA\_CORE



Support BACO Mode

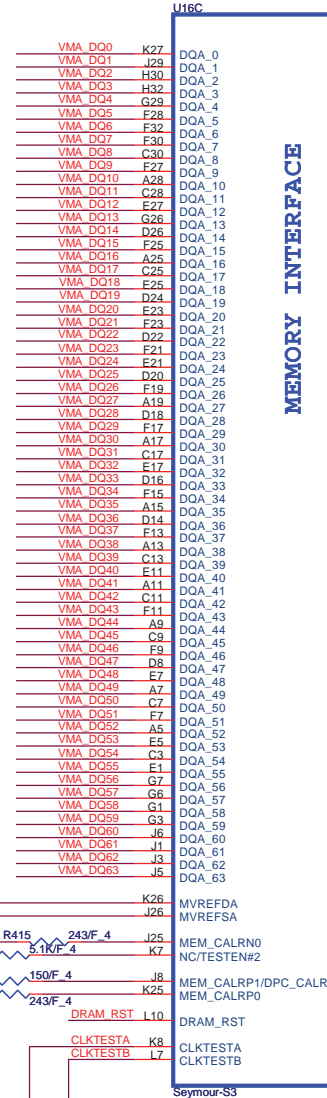
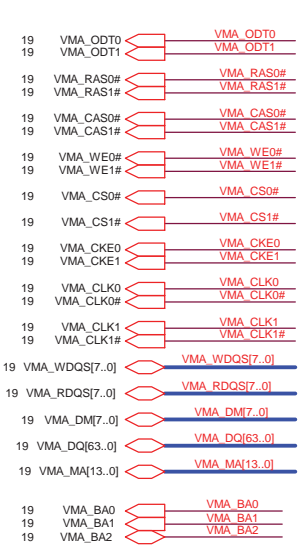


- Note1. 1. No BACO Support :BIF\_VDDC shorts with VDDC (Install Ra)  
 2. BACO Support: Refer to the BACO reference schematics/Application note for detail about BIF\_VDDC Rail if BACO is Supported (Uninstall Ra)

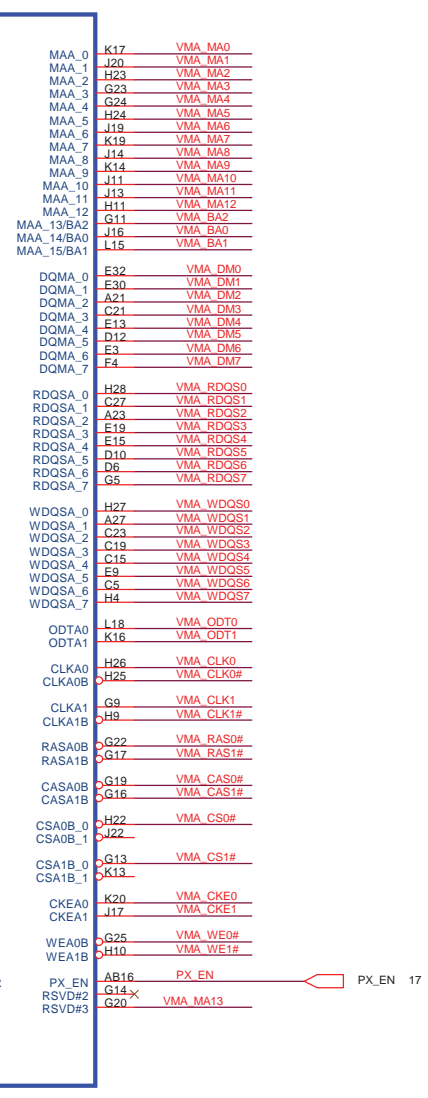


**PROJECT : R13**  
**Quanta Computer Inc.**

Size Custom	Document Number Seymour_Power_and_NC	Rev 3A
Date: Saturday, September 18, 2010 Sheet 17 of 39		

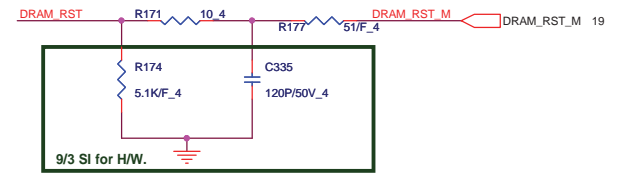
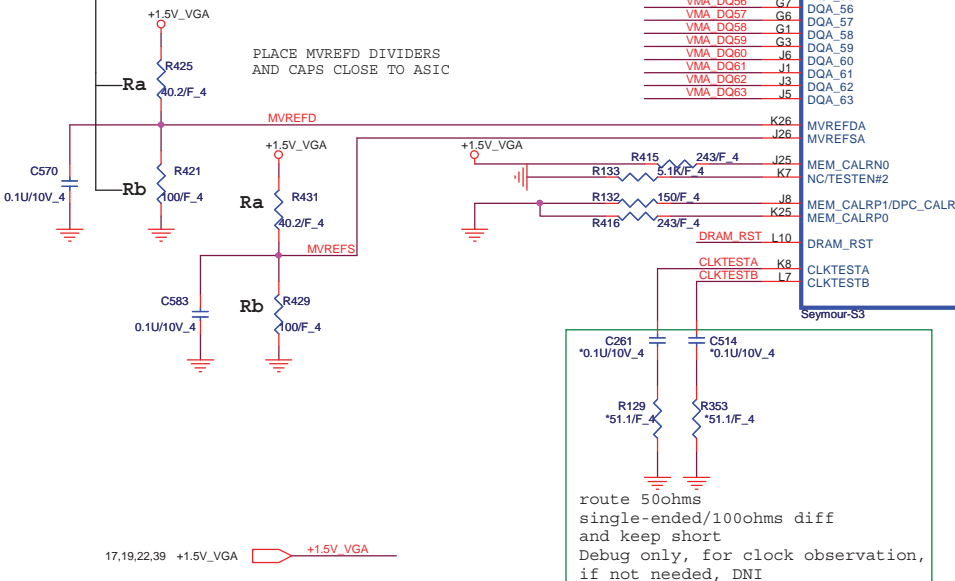


MEMORY INTERFACE



support 1Gbit  
VRAM ( 64M X 16 )

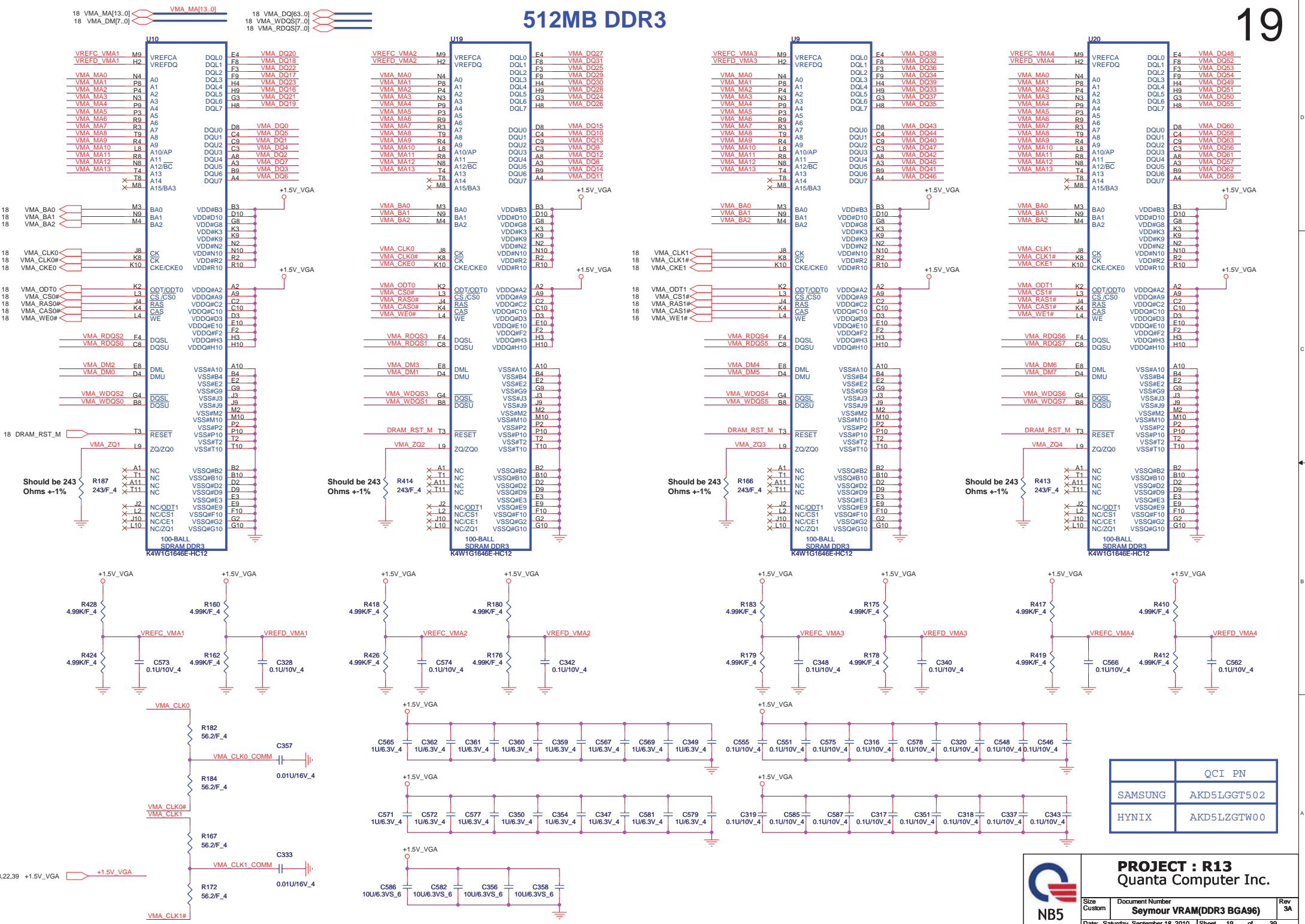
DIVIDER RESISTORS	GDDR5	DDR3
MVREF TO 1.8V (Ra)	40.2R	40.2R
MVREF TO GND (Rb)	100R	100R



**PROJECT : R13**  
Quanta Computer Inc.

Size Custom	Document Number Seymour/MEM_Interface	Rev 3A
Date: Saturday, September 18, 2010 Sheet 18 of 39		

512MB DDR3

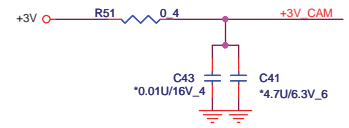
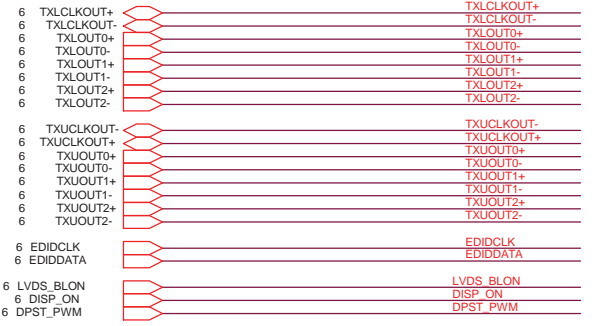
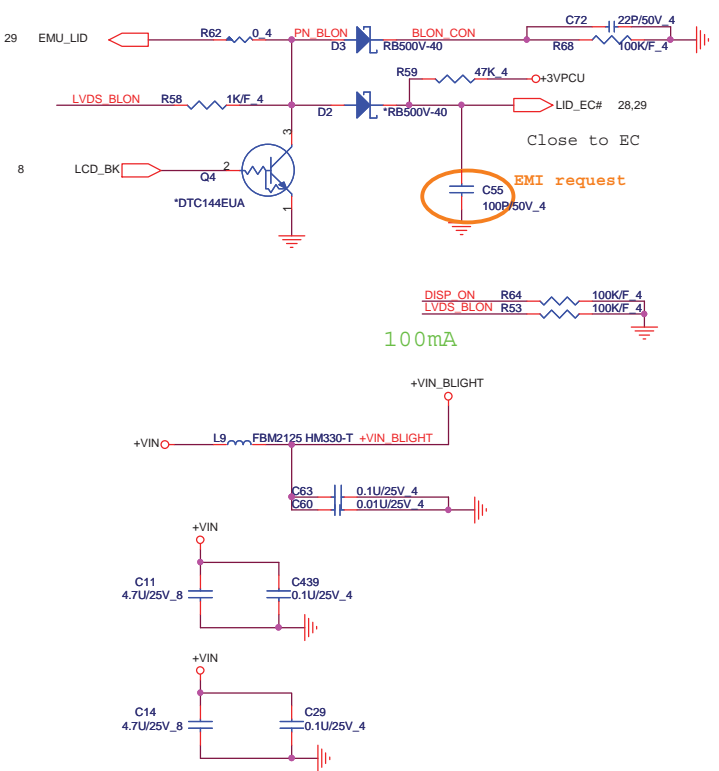


	QCI PN
SAMSUNG	AKD5LGGT502
HYNIX	AKD5LZGTW00

**PROJECT : R13**  
**Quanta Computer Inc.**

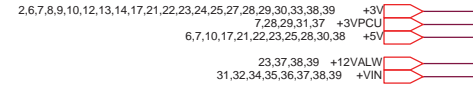
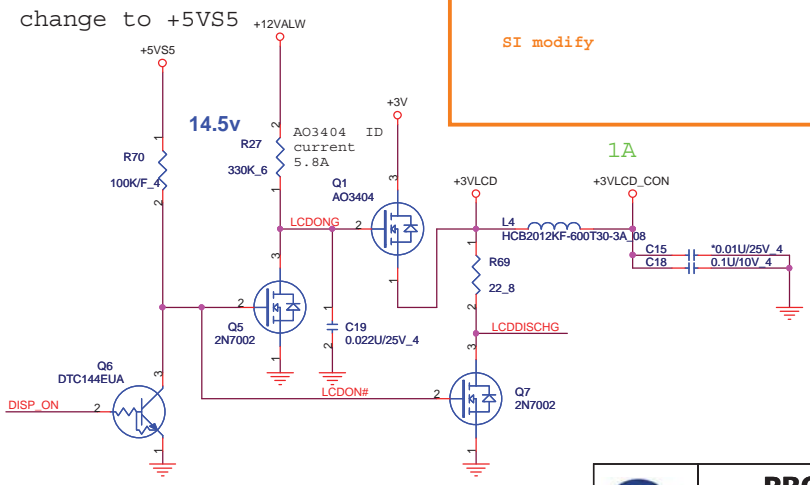
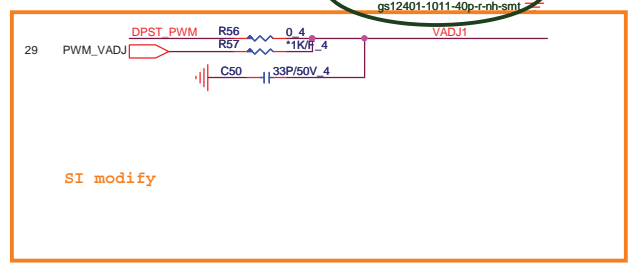
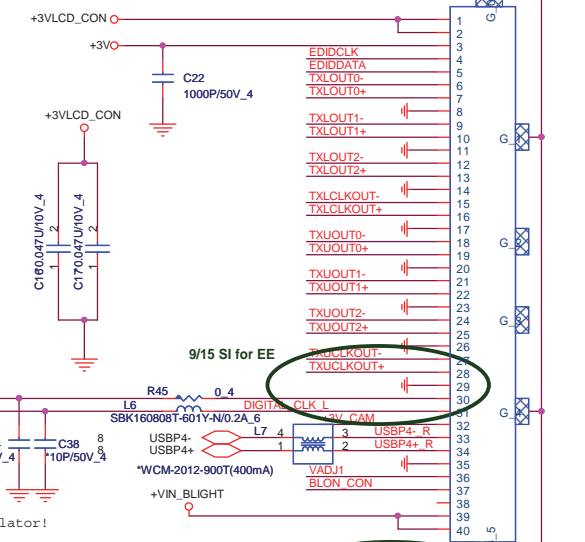
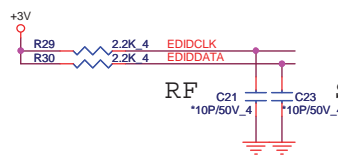
Size Custom Document Number **Seymour VRAM(DDR3 BGA96)** Rev 3A  
 Date: Saturday, September 18, 2010 | Sheet 19 of 39

# LID Switch



follow L7 location

USBP4- R52 0.4 USBP4- R  
 USBP4+ R54 0.4 USBP4+ R



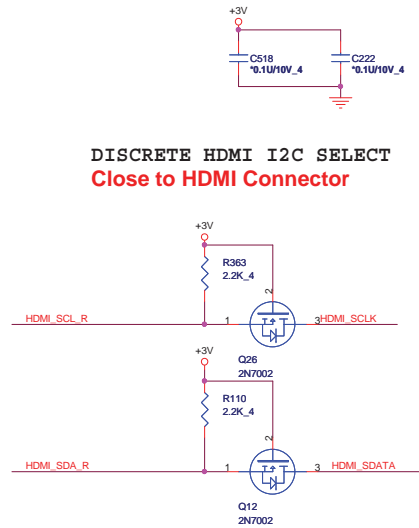


close to HDMI conn

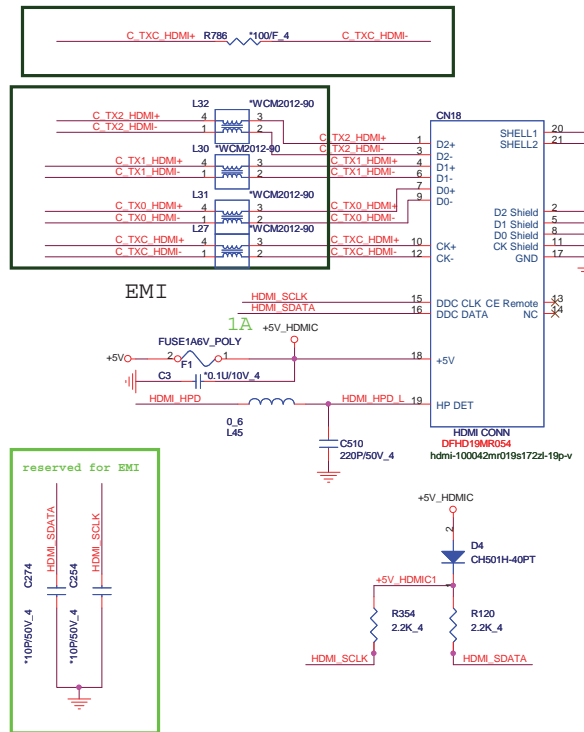
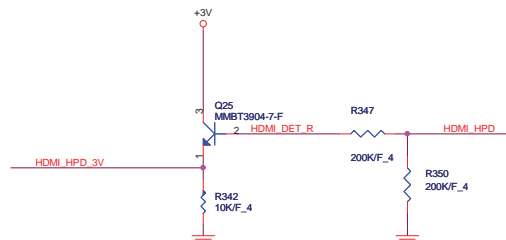
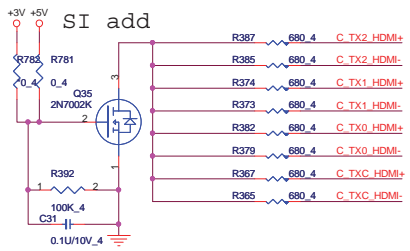
6	IN_CLK#	IN_CLK#	C290	0.1U/10V_4	C_TXC_HDMI-
6	IN_CLK	IN_CLK	C298	0.1U/10V_4	C_TXC_HDMI+
6	IN_DO#	IN_DO#	C307	0.1U/10V_4	C_TX0_HDMI-
6	IN_DO	IN_DO	C309	0.1U/10V_4	C_TX0_HDMI+
6	IN_D1#	IN_D1#	C298	0.1U/10V_4	C_TX1_HDMI-
6	IN_D1	IN_D1	C303	0.1U/10V_4	C_TX1_HDMI+
6	IN_D2#	IN_D2#	C313	0.1U/10V_4	C_TX2_HDMI-
6	IN_D2	IN_D2	C314	0.1U/10V_4	C_TX2_HDMI+



### DISCRETE HDMI I2C SELECT Close to HDMI Connector

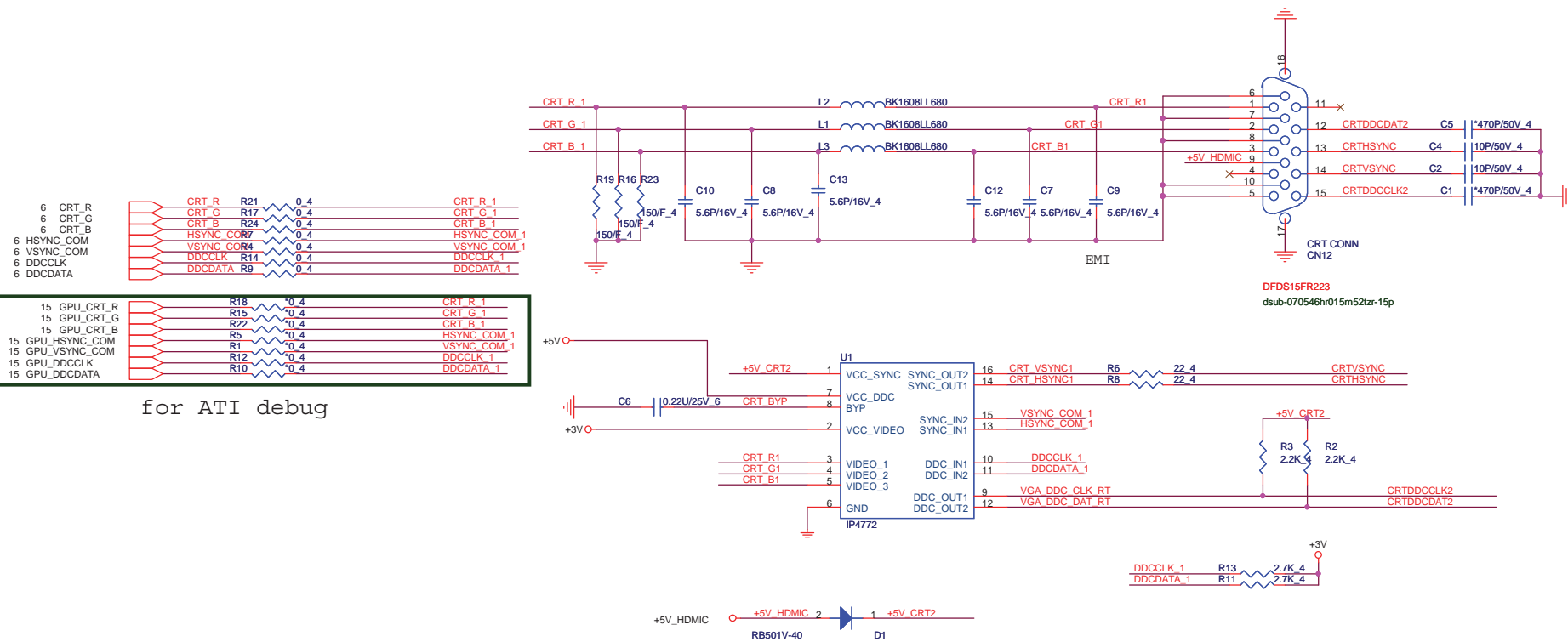


SI add

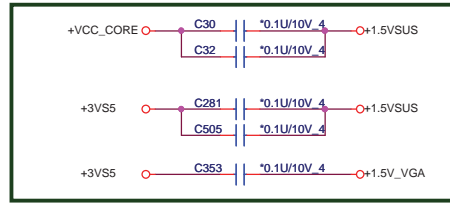
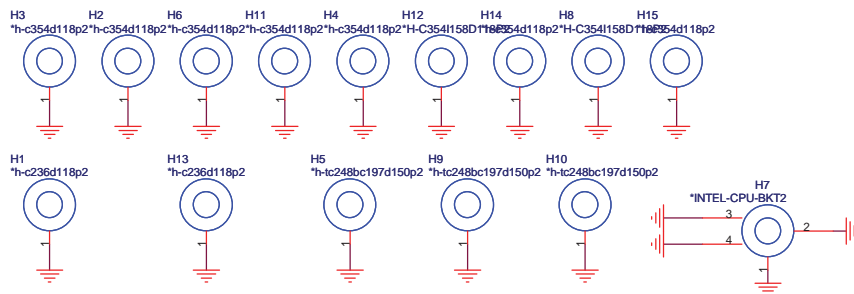


**PROJECT : R13**  
Quanta Computer Inc.

# CRT PORT



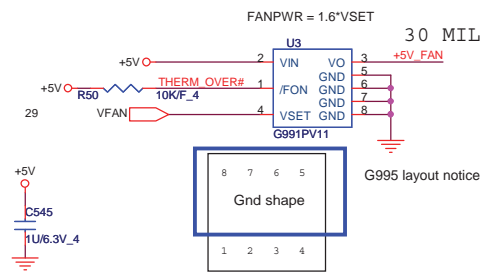
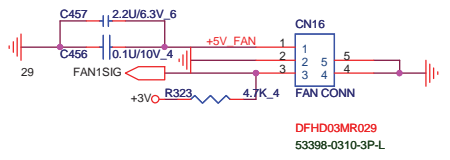
# HOLE



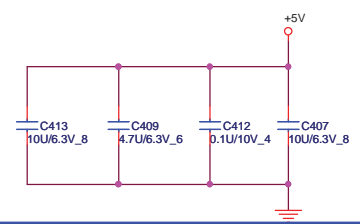
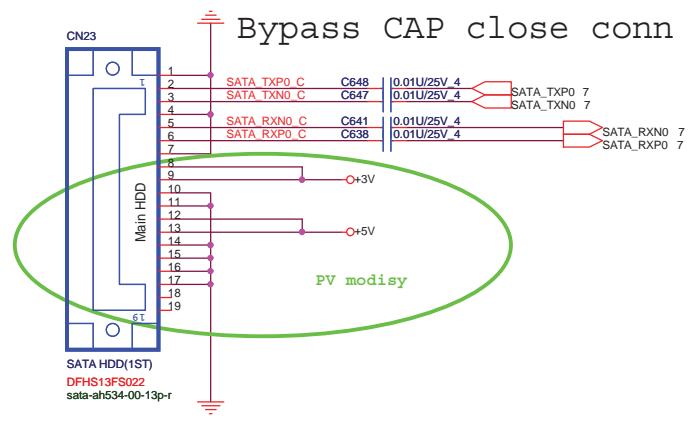
RF solution

	<b>PROJECT : R13</b> Quanta Computer Inc.	
	Size Custom Document Number <b>CRT,Hole</b>	Rev <b>3A</b>
Date: Saturday, September 18, 2010 Sheet 22 of 39		

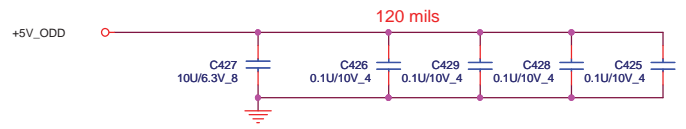
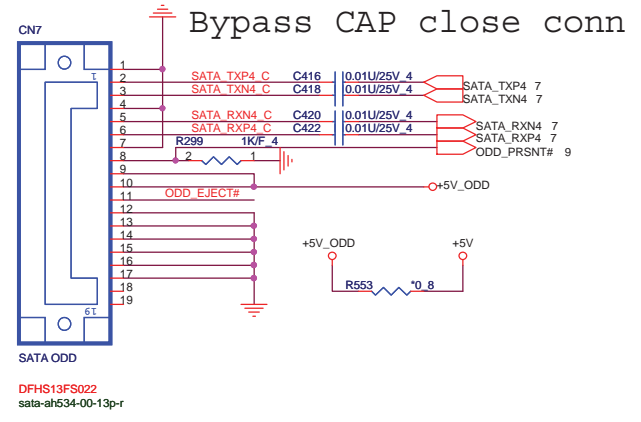
### CPU FAN



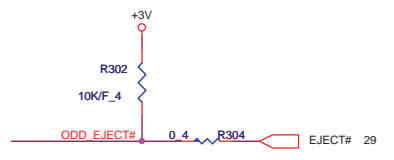
### SATA HDD CONNECTOR



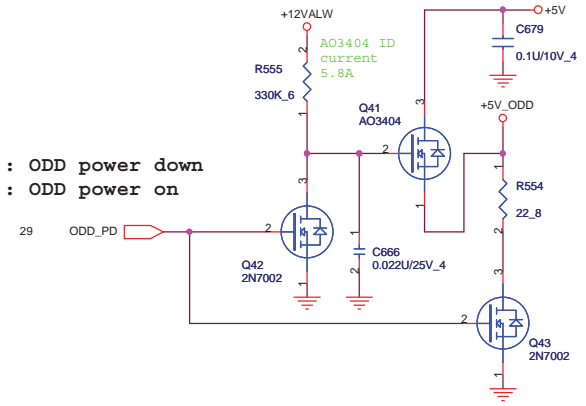
### SATA ODD CONNECTOR



follow INTEL DG change eject PU to +3V.



High : ODD power down  
Low : ODD power on



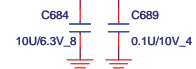
2,8,14,27,29,30 PLTRST#

8 CLK\_PCIE\_REQ2# R542 0.4 CLK\_PCIE\_REQ2# R

8 PCIE\_TXP3\_CARD  
8 PCIE\_TXN3\_CARD  
8 CLK\_PCIE\_CARDP  
8 CLK\_PCIE\_CARDN

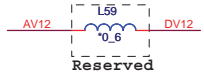
8 PCIE\_RXP3\_CARD  
8 PCIE\_RXN3\_CARD

+3VCARD

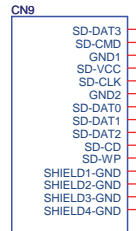


+3V3 cap place close chip

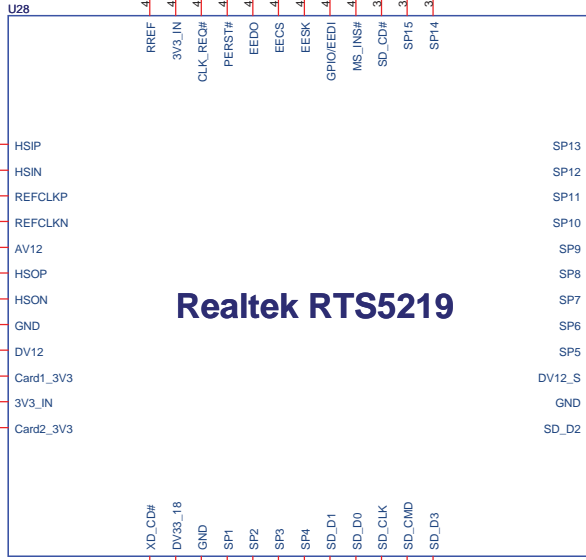
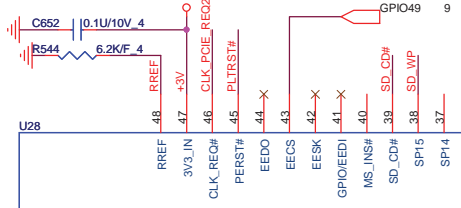
RTS5159 max output current for ..  
XD card 250mA  
SD/MMC 250mA  
MS/MSPRO 250mA



Reserved



CARD READER SOCKET  
DFHD11MR003  
SDCARD-CS1S-038-11P-SMT  
9/6 SI for SMT.

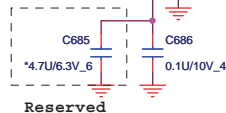


### Realtek RTS5219

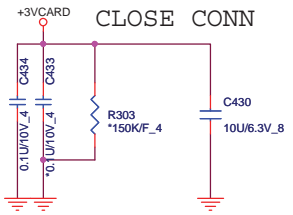
Footprint lqfp48-9x9-5-1\_6h

SP13  
SP12  
SP11  
SP10  
SP9  
SP8  
SP7  
SP6  
SP5  
DV12\_S  
GND  
SD\_D2

R3019-R3024, C3009 close to chip pin



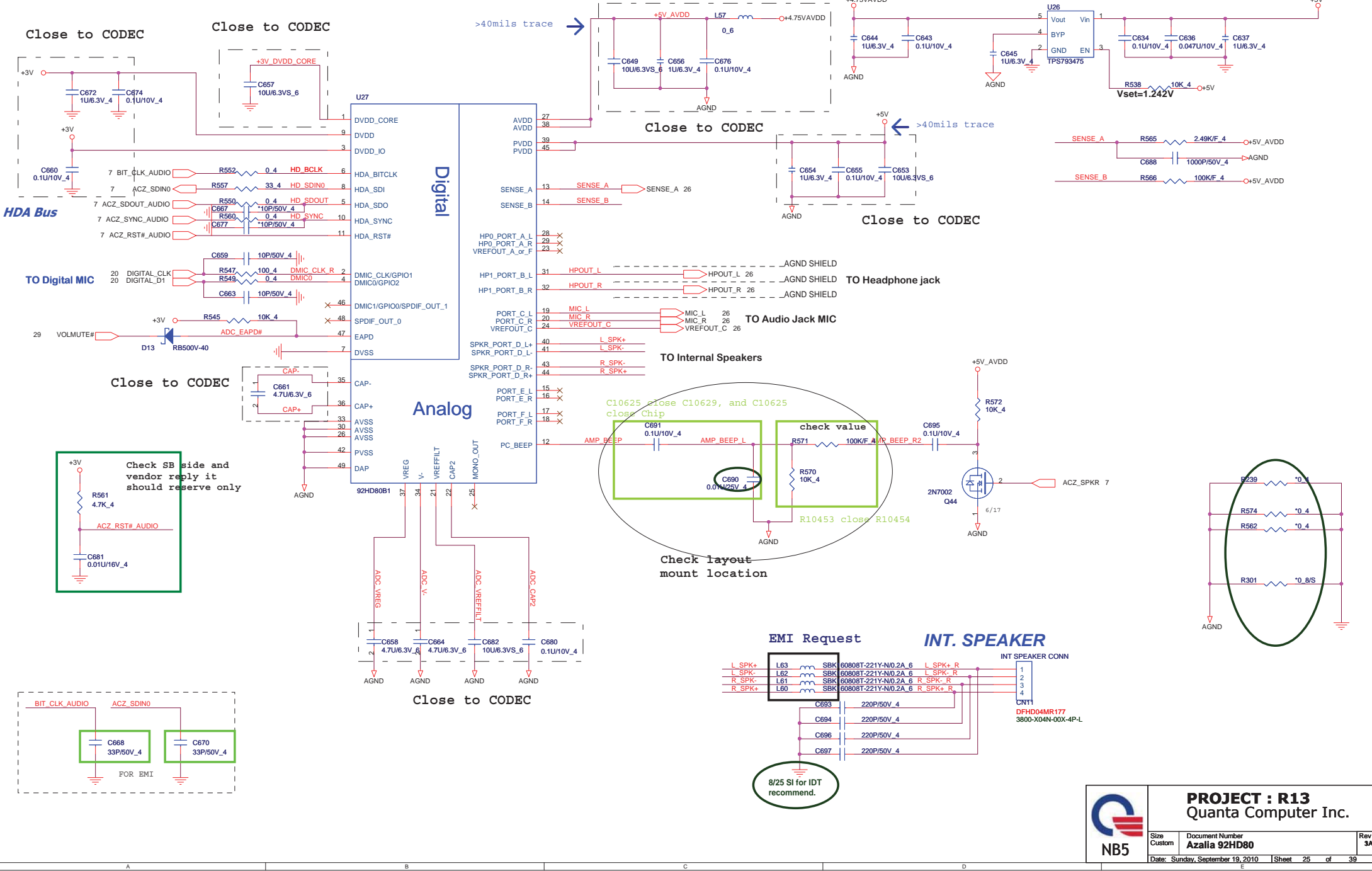
Reserved



PROJECT : R13  
Quanta Computer Inc.

Size Custom	Document Number RTS5219 & CR SOCKET & HOLE	Rev 3A
Date: Saturday, September 18, 2010   Sheet 24 of 39		

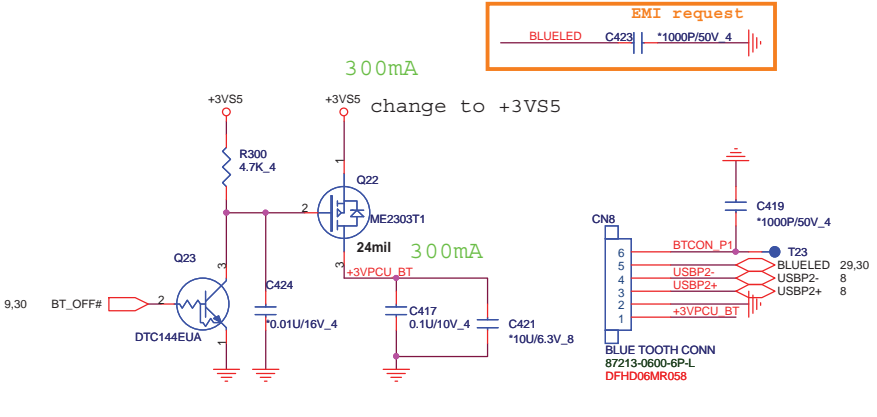
2,6,7,8,9,10,12,13,14,17,20,21,22,23,24,27,28,29,30,33,38,39 +3V  
 6,7,10,17,21,22,23,28,30,38 +5V



	<b>PROJECT : R13</b>	
	Quanta Computer Inc.	
Size Custom	Document Number <b>Azalia 92HD80</b>	Rev <b>3A</b>
Date: Sunday, September 19, 2010   Sheet 25 of 39		

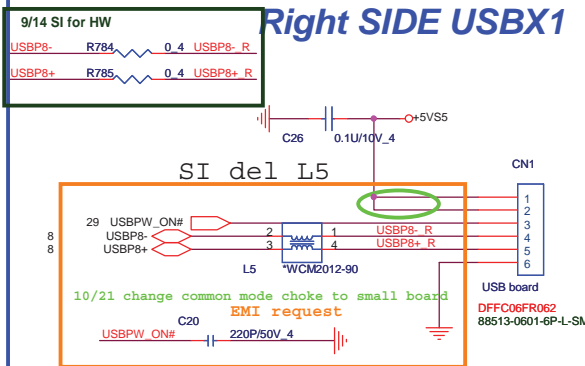
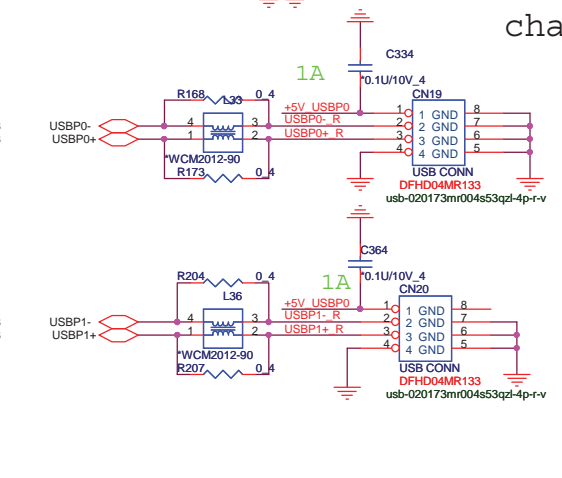
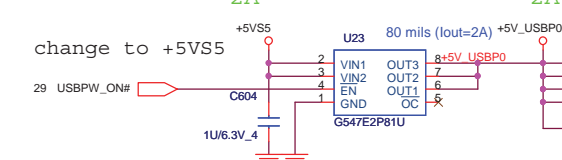


# BLUETOOTH

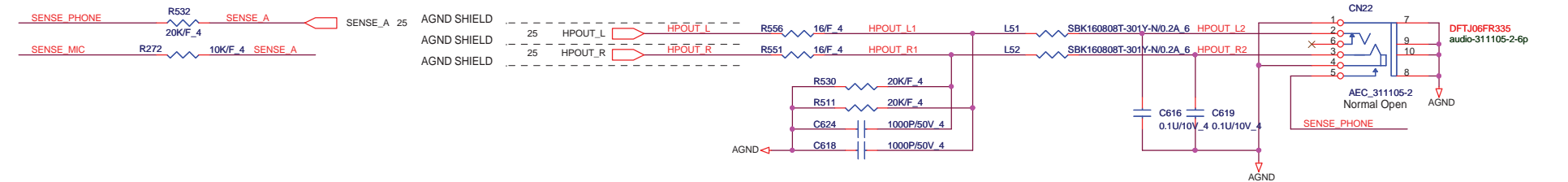


# LEFT SIDE USBX2

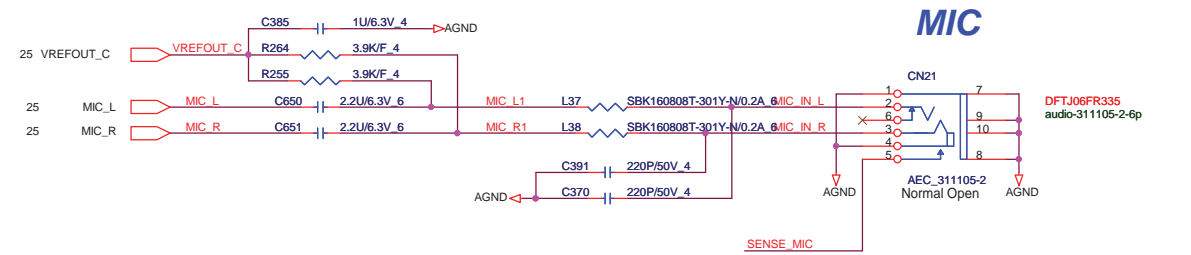
change to AL000547005



# Line out

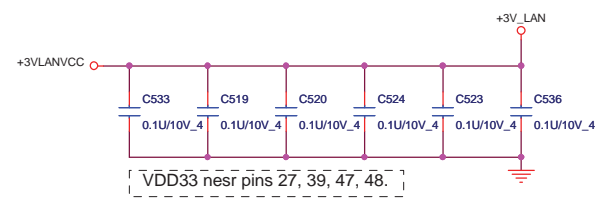
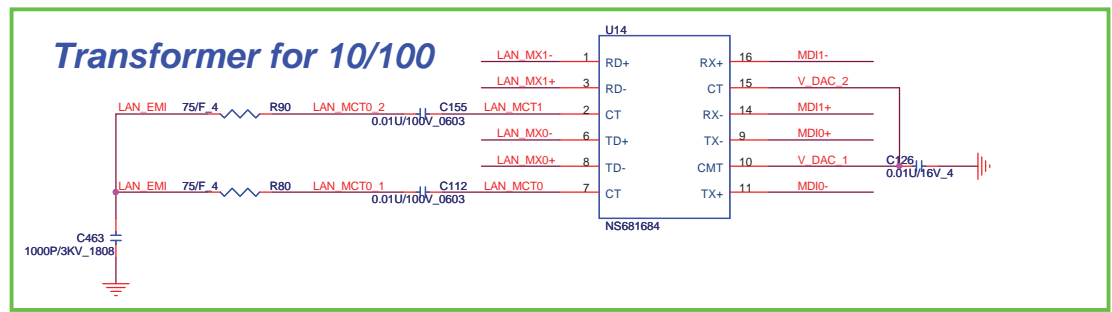
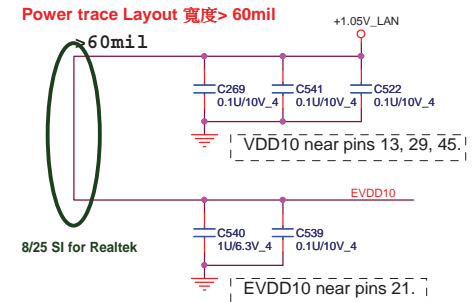
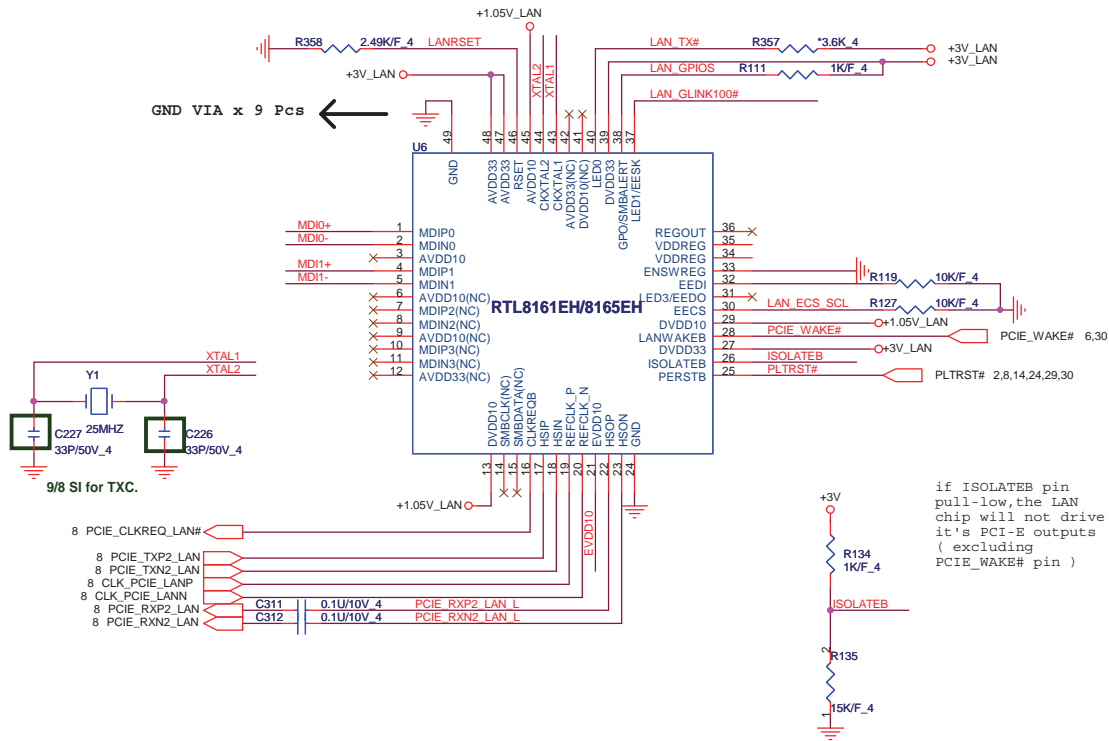


# MIC

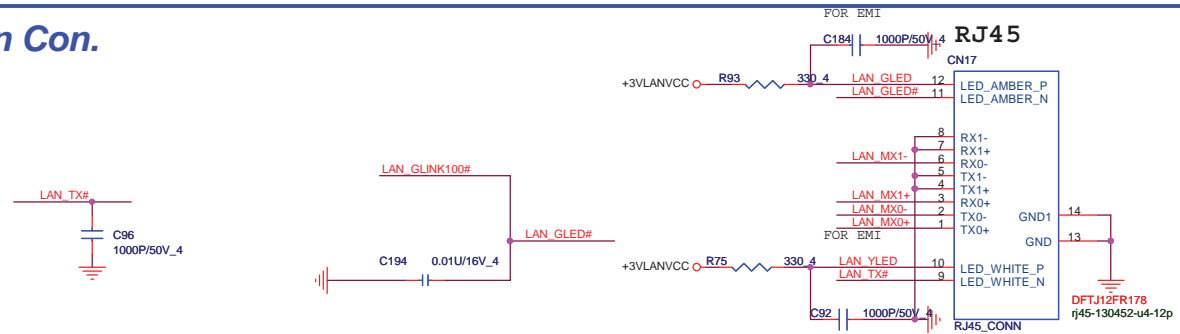


PROJECT : R13  
Quanta Computer Inc.

Size Custom	Document Number	Rev 3A
USB/BT/Audio Jack		
Date: Saturday, September 18, 2010	Sheet 26	of 39



Lan Con.



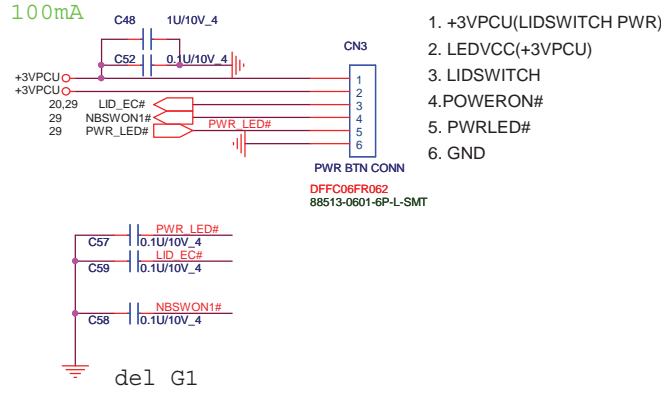
2,6,7,8,9,10,12,13,14,17,20,21,22,23,24,25,28,29,30,33,38,39



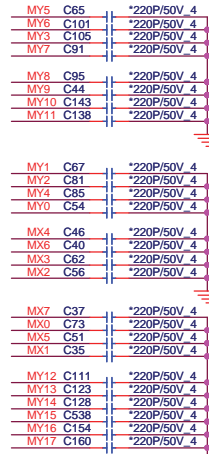
**PROJECT : R13**  
Quanta Computer Inc.

Size Custom	Document Number <b>RTL8165EH</b>	Rev 3A
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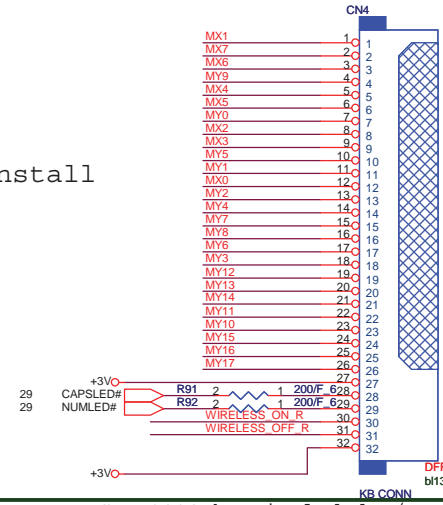
# POWER BOTTON CONNECT



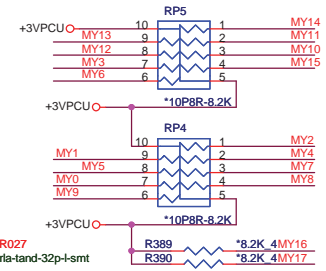
# KEYBOARD Con.



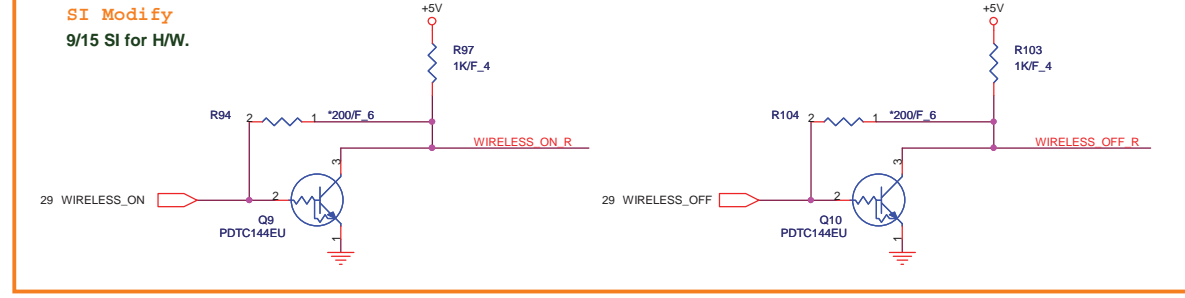
SI un-install



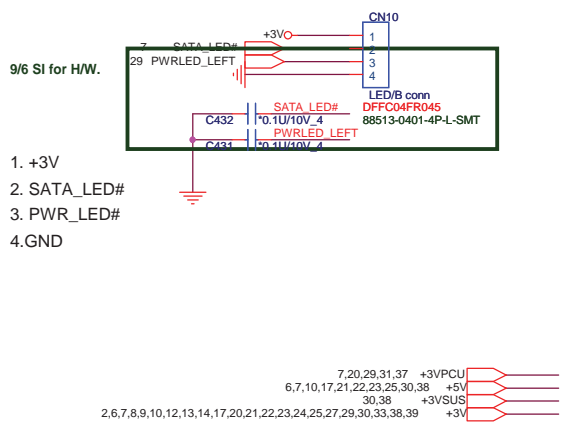
# KEYBOARD PULL-UP



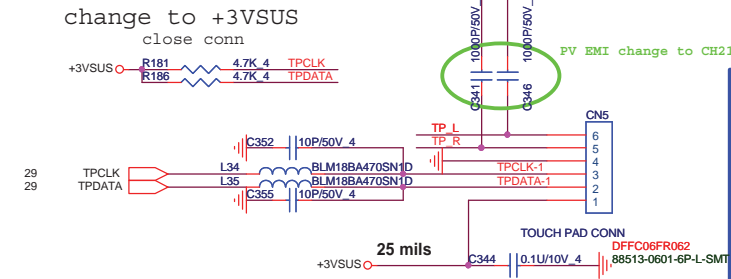
EC KB3930 has included K/B pull-up resistor and function



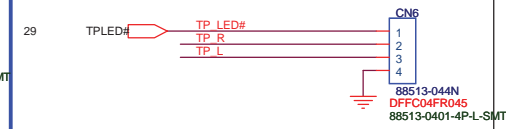
# LED Con.

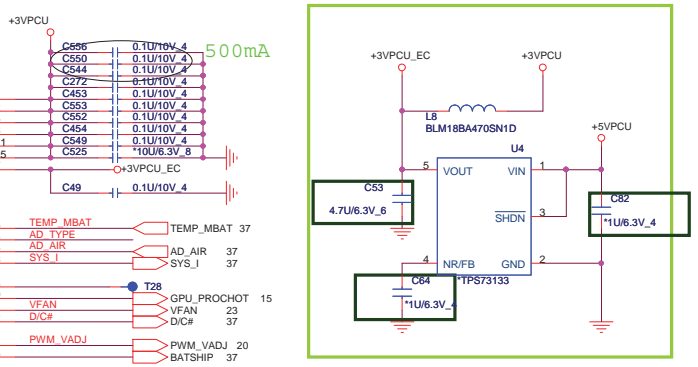
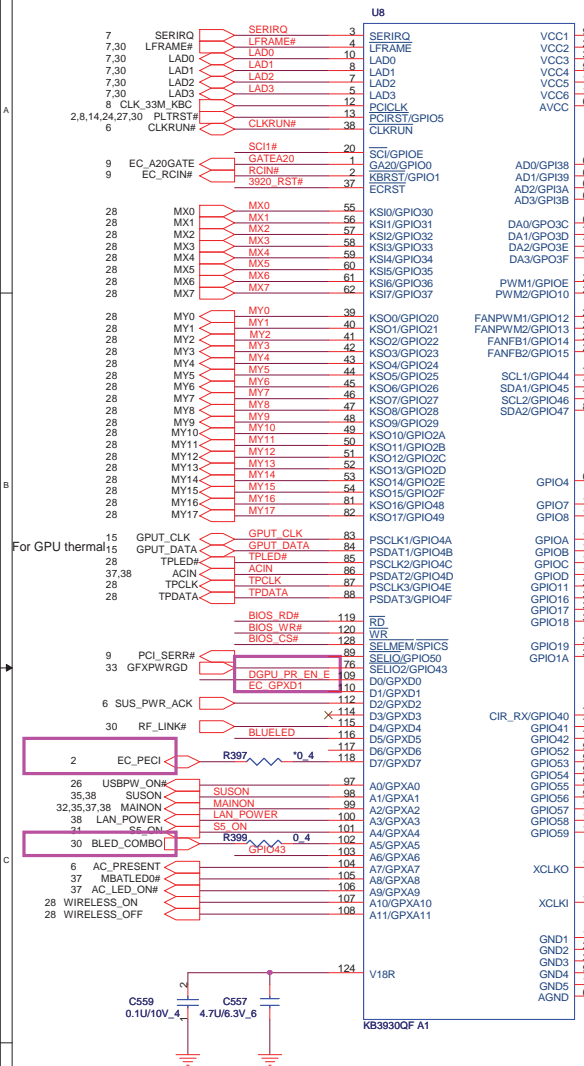


# TOUCH PAD Con.

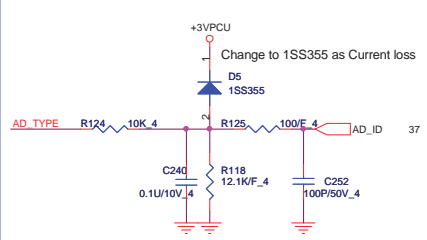


# To TOUCH PAD SW board

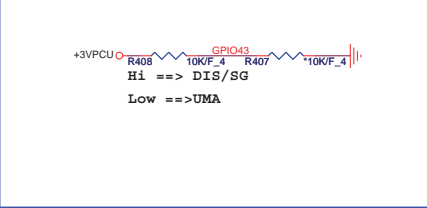




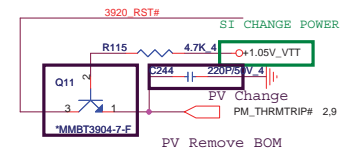
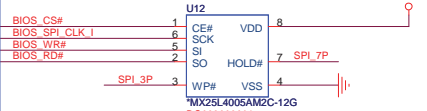
### adapter Type check



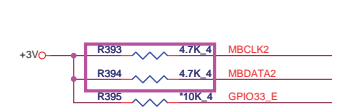
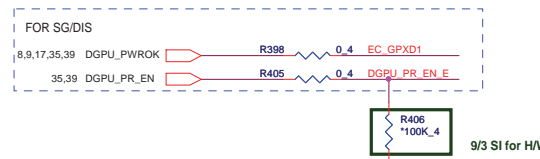
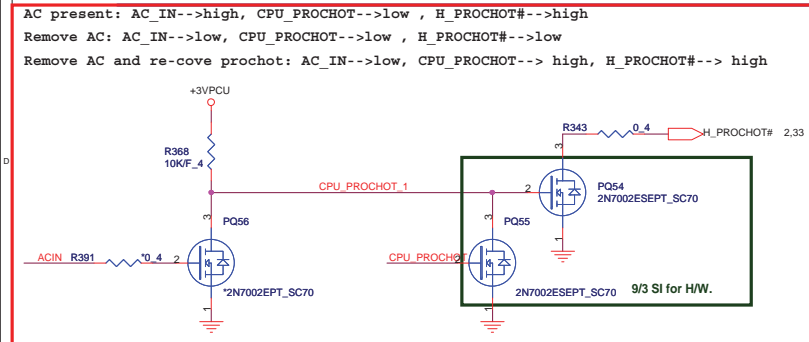
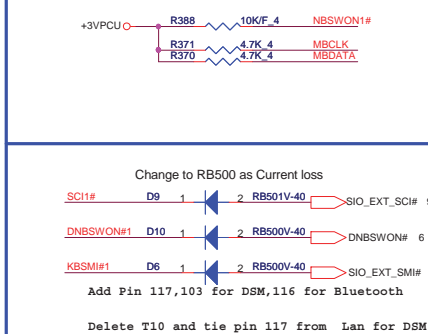
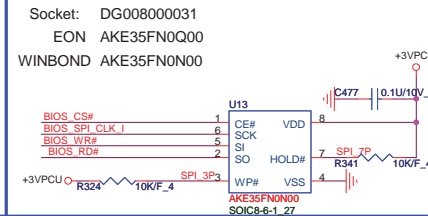
### adapter select for EC



### 128K byte SPI EC ROM



### 512K byte SPI EC ROM



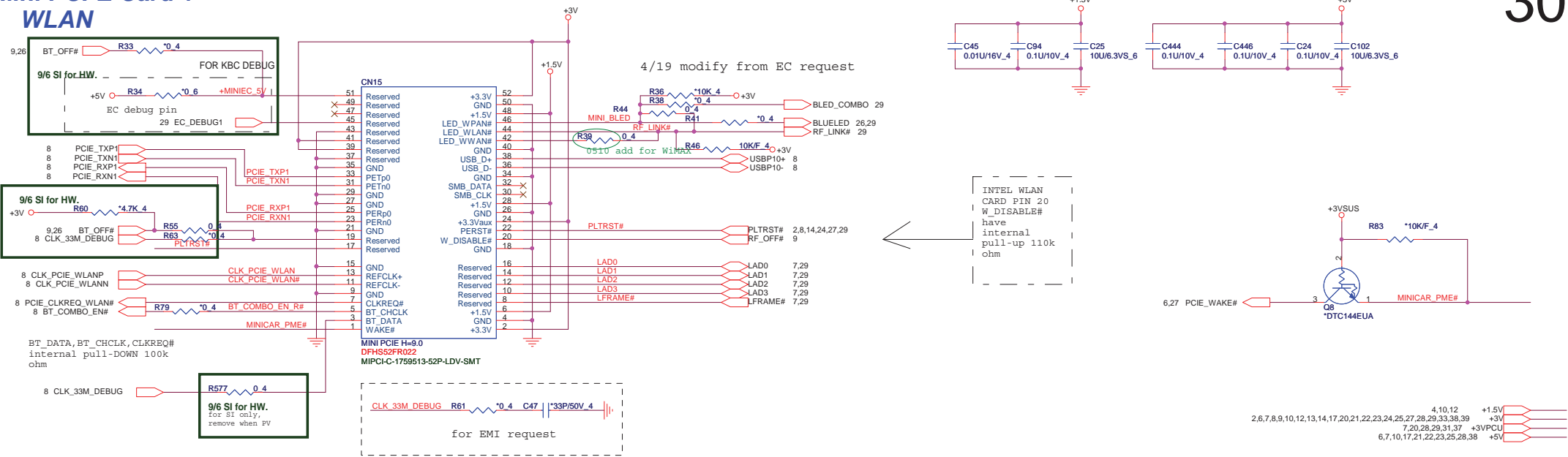
**PROJECT : R13**  
**Quanta Computer Inc.**

Size Custom    Document Number **EC (KB3926)ROM**    Rev **3A**

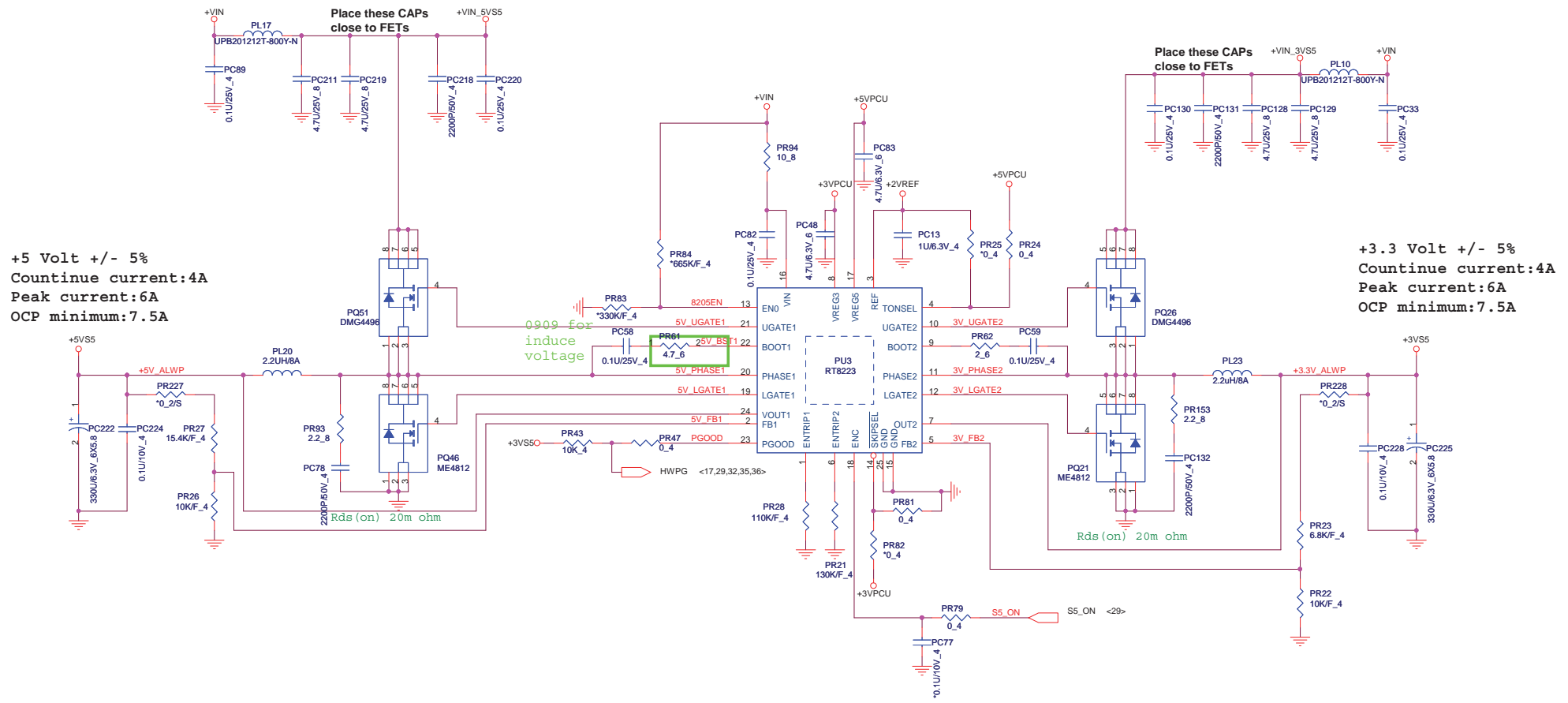
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2,6,7,8,9,10,12,13,14,17,20,21,22,23,24,25,27,28,30,33,38,39 +3V  
7,20,28,31,37 +3VPCU  
31,37 +5VPCU

# Mini PCI-E Card 1 WLAN




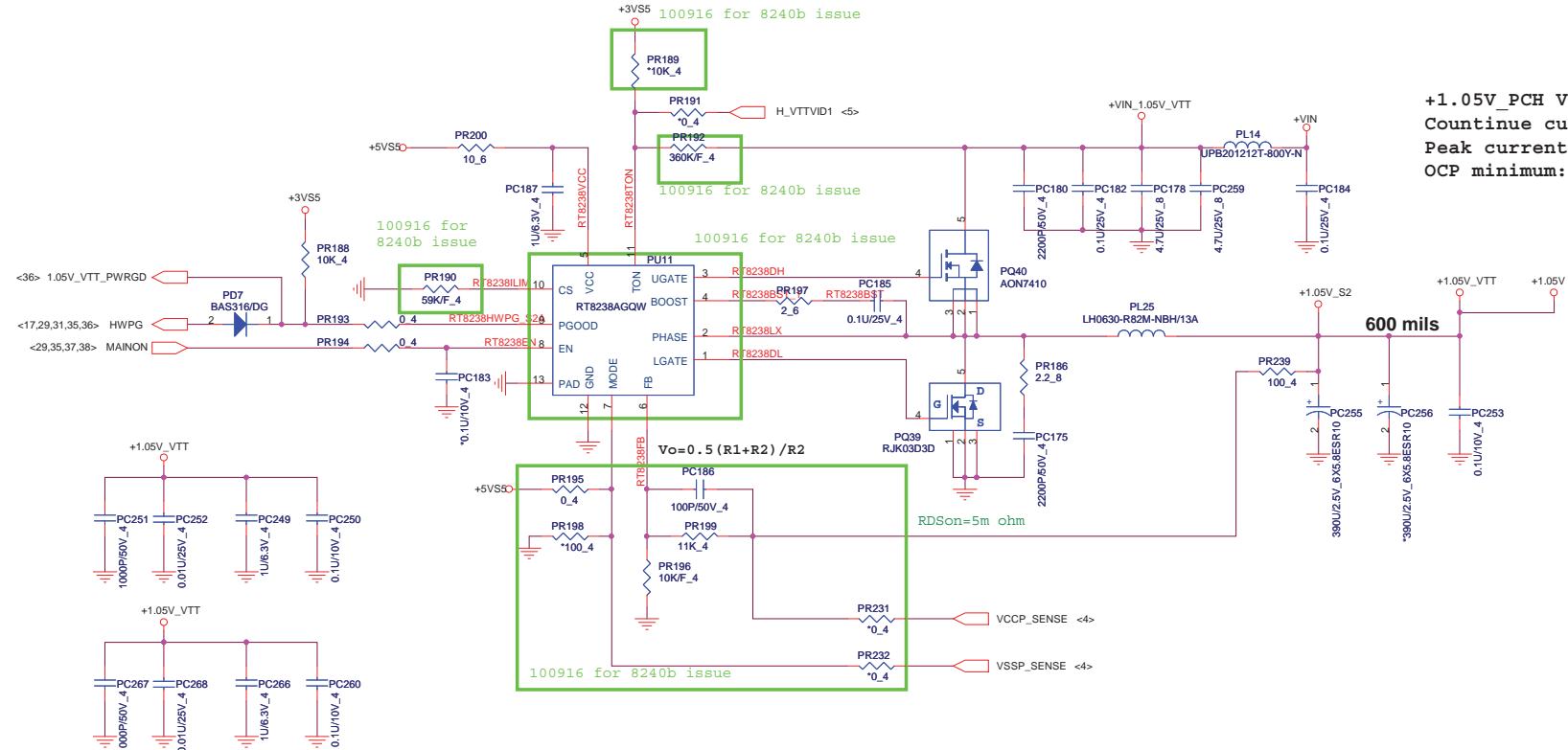




**+5 Volt +/- 5%**  
 Countinue current:4A  
 Peak current:6A  
 OCP minimum:7.5A

**+3.3 Volt +/- 5%**  
 Countinue current:4A  
 Peak current:6A  
 OCP minimum:7.5A

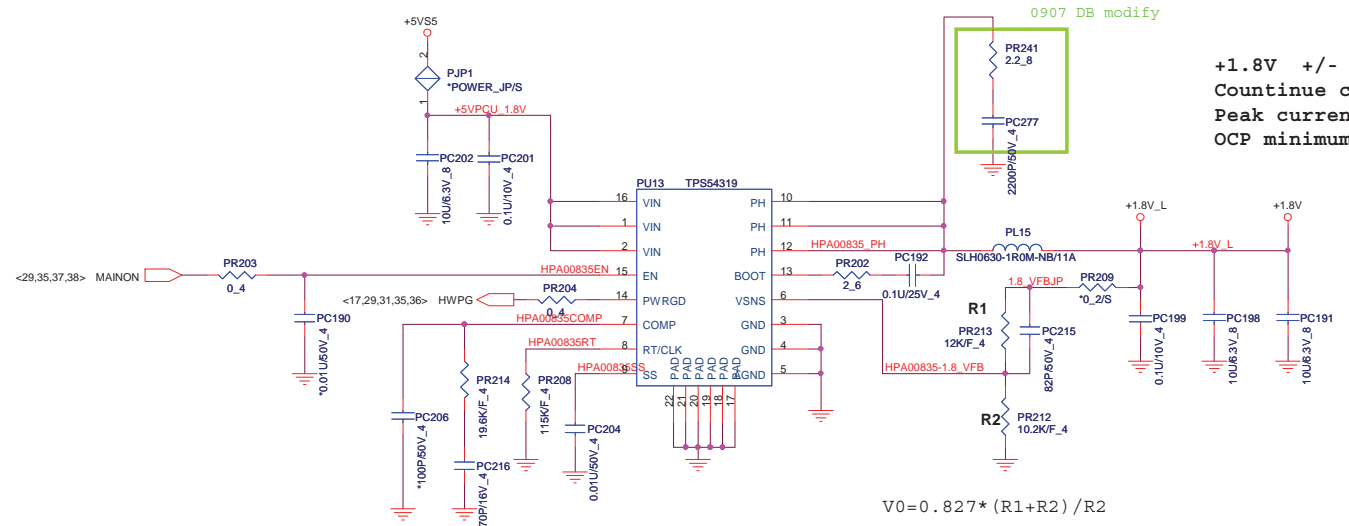
	<b>PROJECT : R13</b>		Rev 3A
	Quanta Computer Inc.		
	Size Custom	Document Number <b>+5V/+3V (RT8206B)</b>	
Date: Saturday, September 18, 2010   Sheet 31 of 39			



+1.05V\_PCH Volt +/- 5%  
 Countinue current:10A  
 Peak current: 12A  
 OCP minimum: 14.5A


$$V_o = 0.5 (R1+R2) / R2$$

RDSon=5m ohm

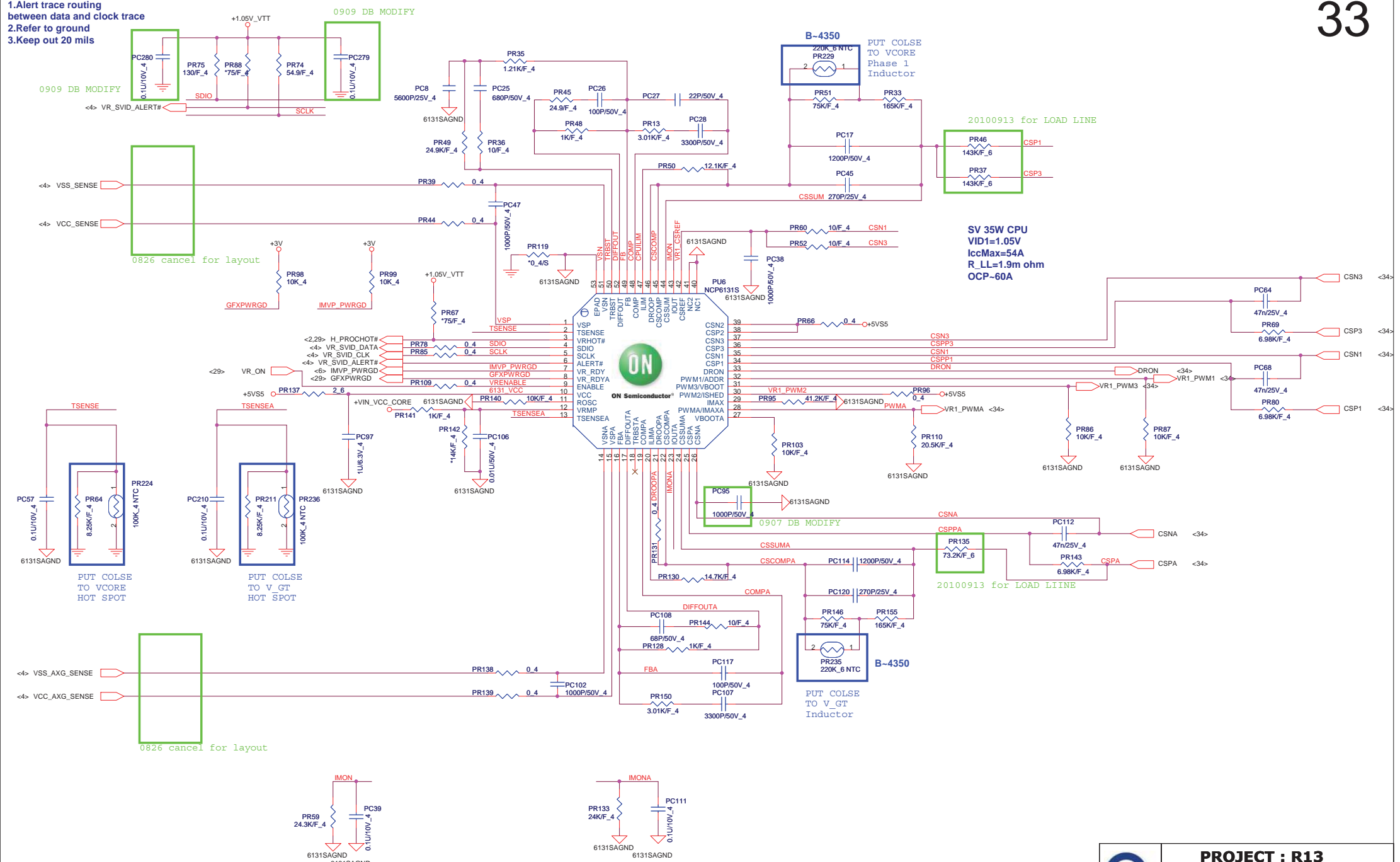


+1.8V +/- 5%  
 Countinue current:1.5A  
 Peak current: 2.5A  
 OCP minimum 4A

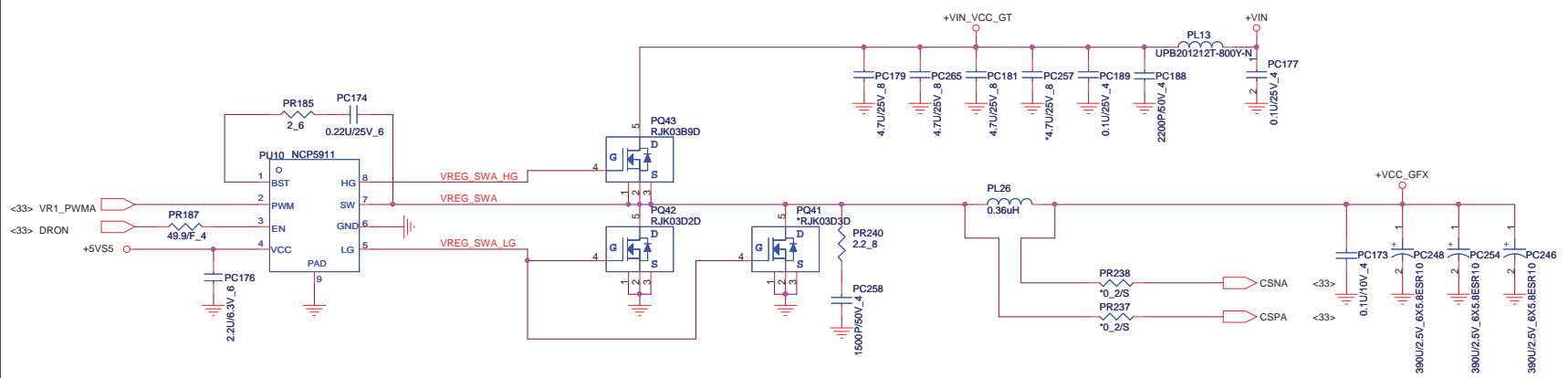
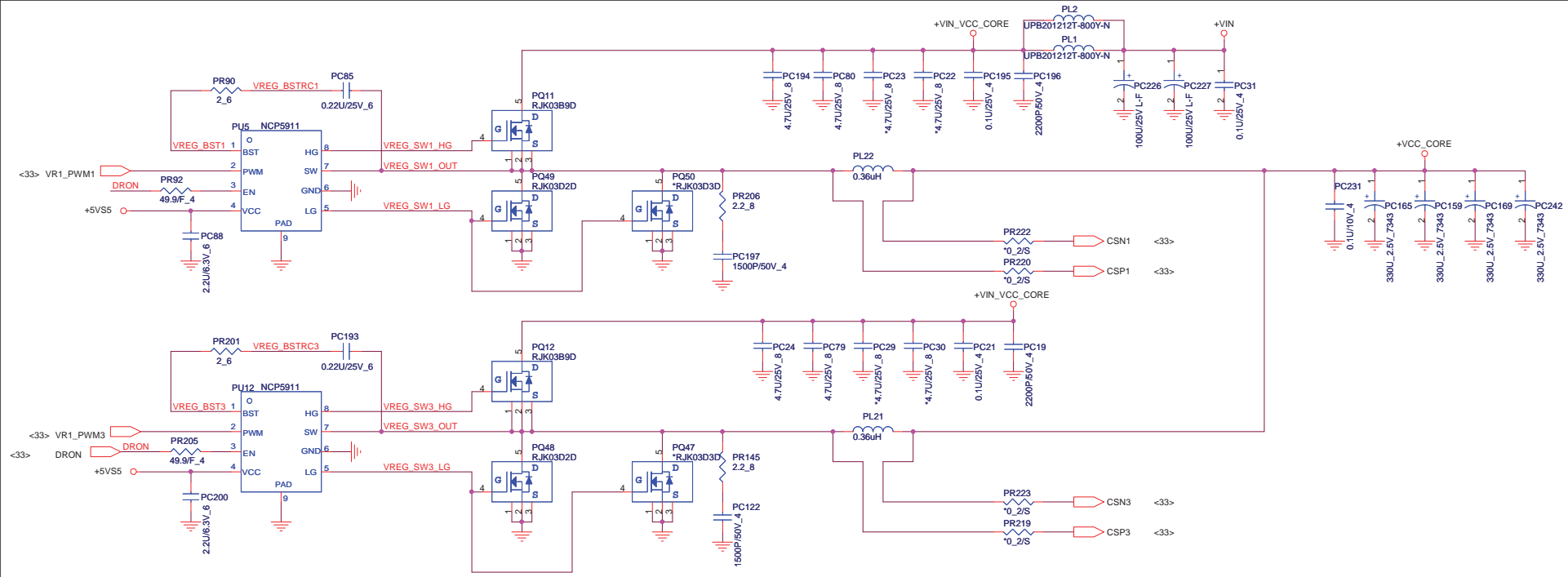
$$V_o = 0.827 * (R1+R2) / R2$$


	<b>PROJECT : R13</b>		Rev 3A
	Quanta Computer Inc.		
	Size Custom	Document Number +1.1V VTT / PCH	

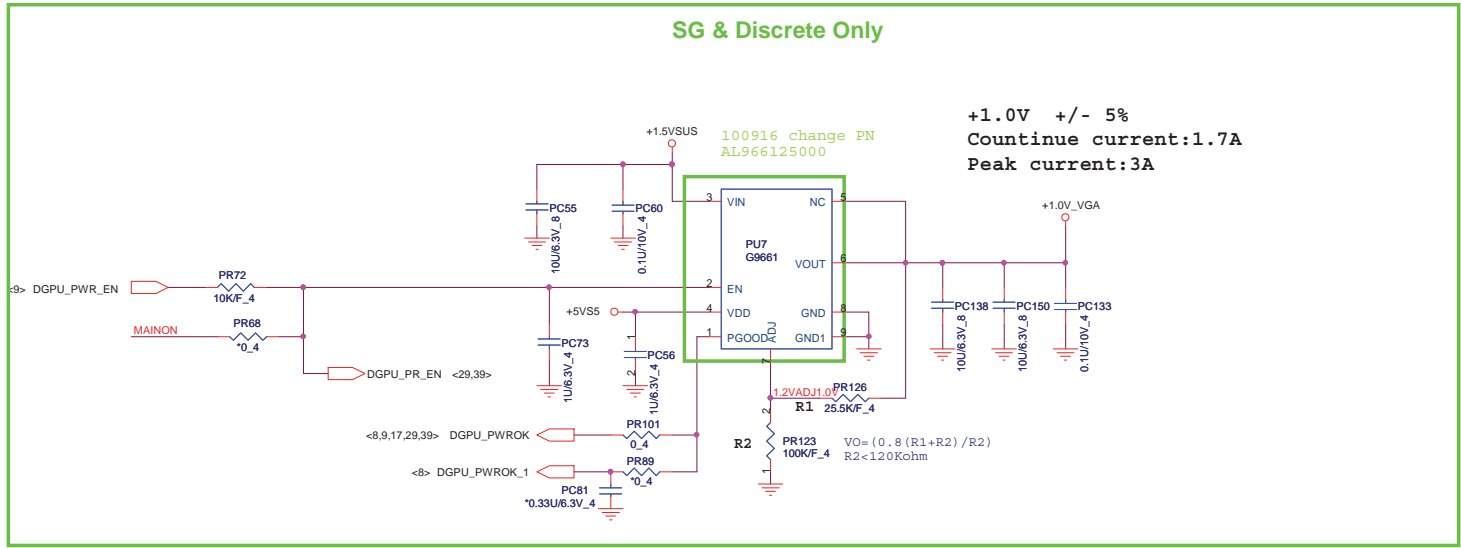
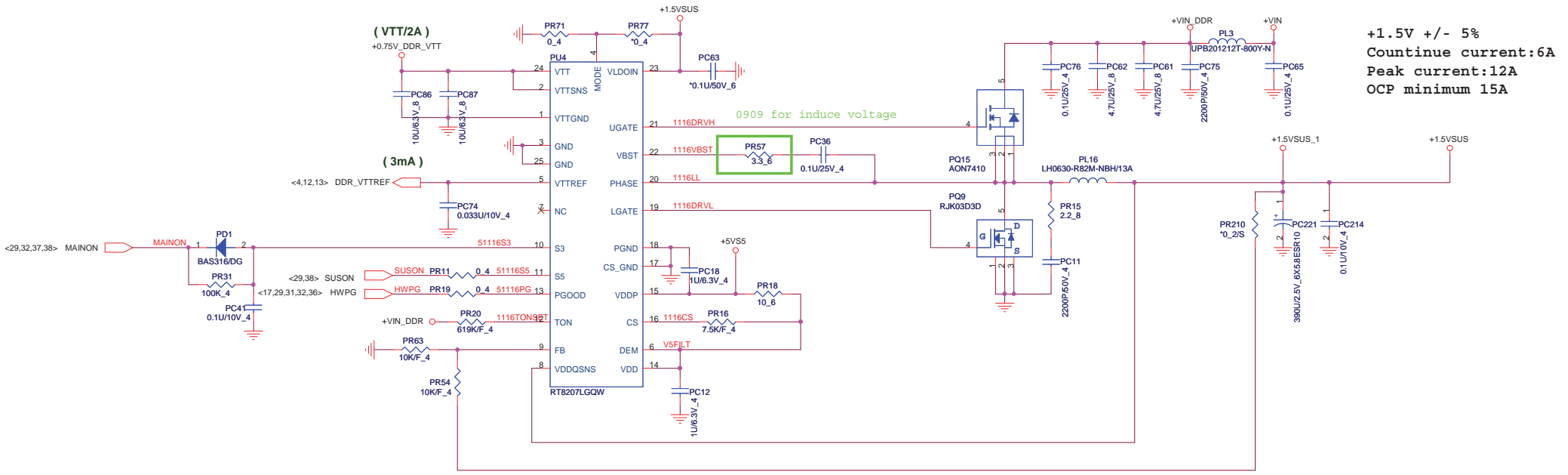
- 1.Alert trace routing between data and clock trace
- 2.Refer to ground
- 3.Keep out 20 mils



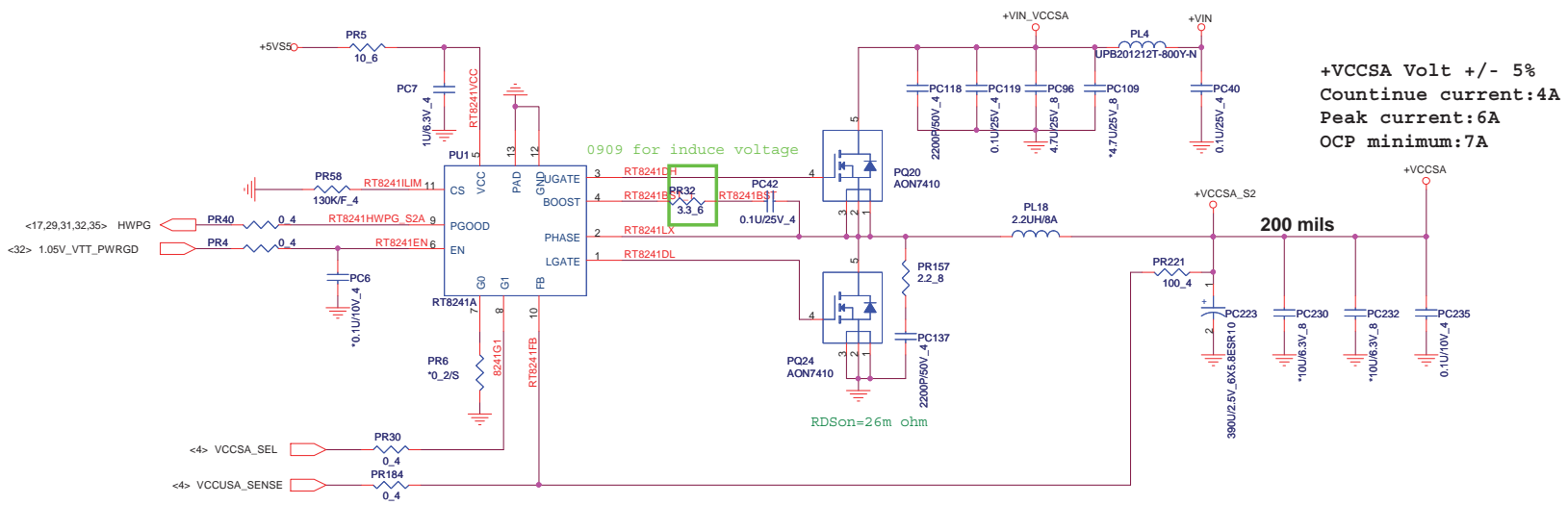
	<b>PROJECT : R13</b>		Rev 3A
	Quanta Computer Inc.		
	Size Custom	Document Number <b>CPU Core1 (NCP6131S)</b>	



 <p><b>NB5</b></p>	<p><b>PROJECT : R13</b> Quanta Computer Inc.</p>	
	<p>Size: Custom</p>	<p>Document Number: <b>CPU Core2 (NCP5911)</b></p>
<p>Date: Saturday, September 18, 2010   Sheet 34 of 39</p>		





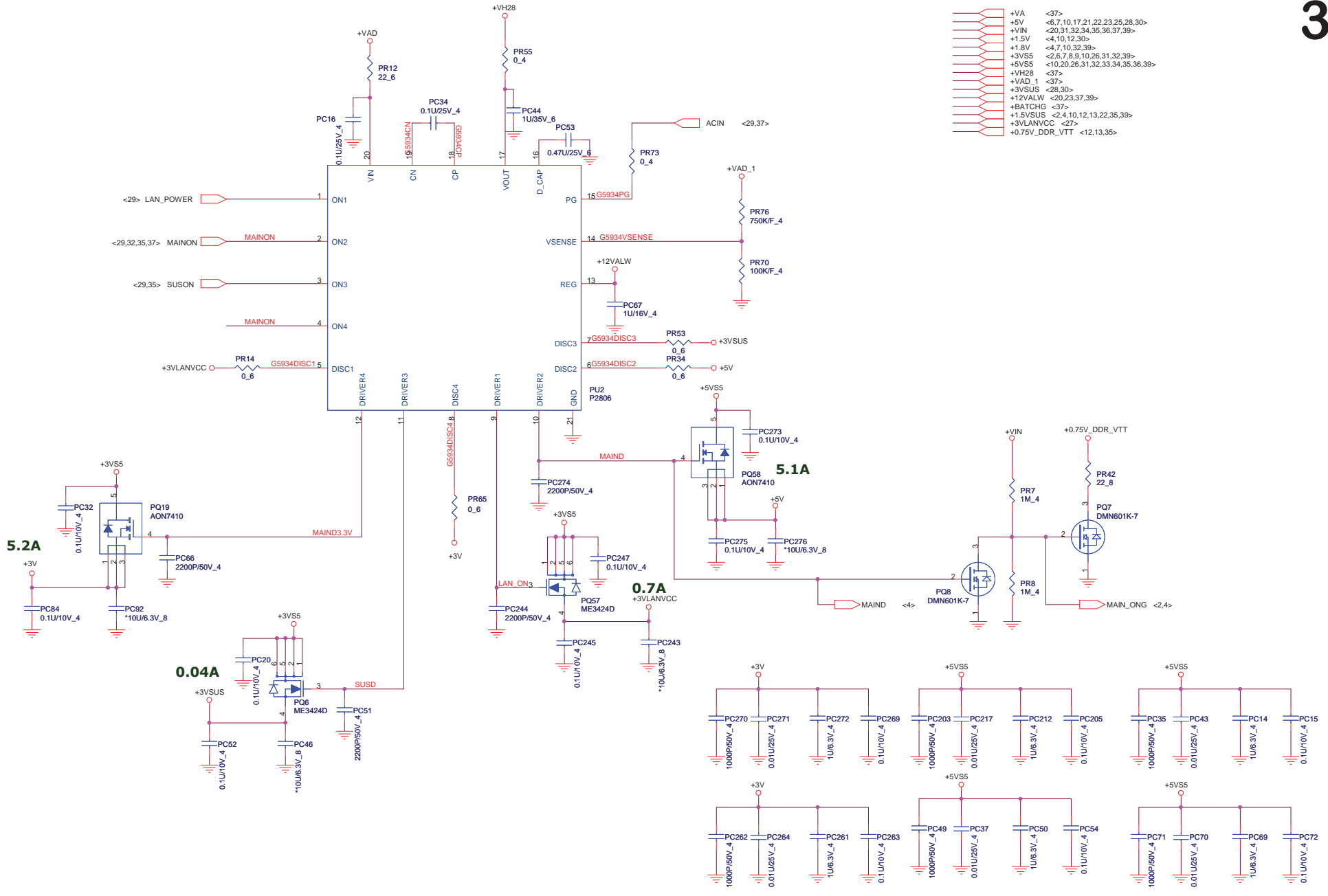



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 Quanta Computer Inc.

Size Custom	Document Number +1.1V VTT / PCH	Rev 3A
Date: Saturday, September 18, 2010   Sheet 36 of 39		

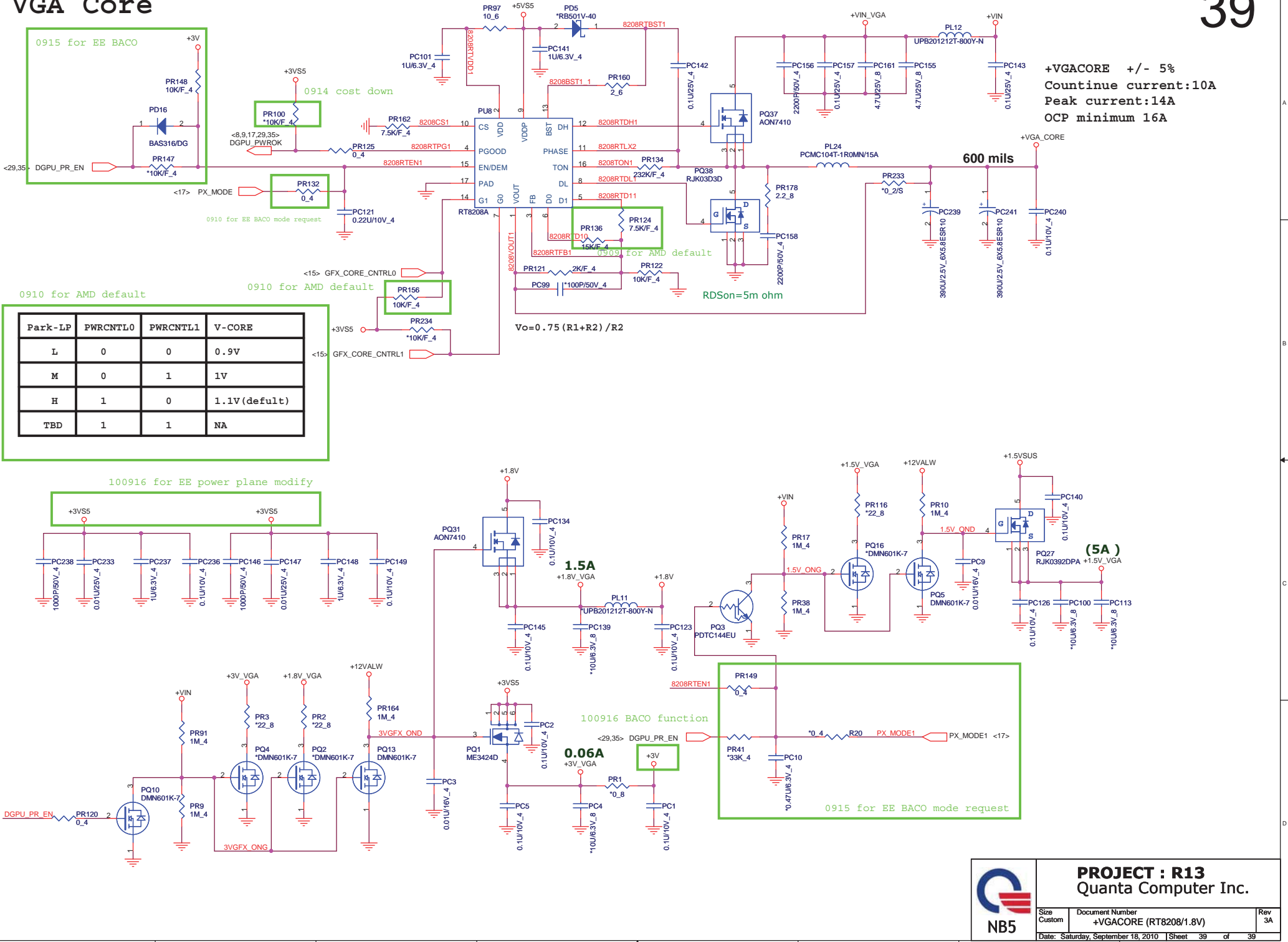


- +VA <37>
- +5V <6,7,10,17,21,22,23,25,28,30>
- +VIN <20,31,32,34,35,36,37,39>
- +1.5V <4,10,12,30>
- +1.8V <4,7,10,32,39>
- +3VS5 <2,6,7,8,9,10,26,31,32,39>
- +5VS5 <10,20,26,31,32,33,34,35,36,39>
- +VH28 <37>
- +VAD <37>
- +VAD\_1 <37>
- +3VSUS <28,30>
- +12VALW <20,23,37,39>
- +BATCHG <37>
- +1.5VSUS <2,4,10,12,13,22,35,39>
- +3VLAVCC <27>
- +0.75V\_DDR\_VTT <12,13,35>



	<b>PROJECT : R13</b>	
	Quanta Computer Inc.	
Size Custom	Document Number Dis-charge IC (G5934)	Rev 3A
Date: Saturday, September 18, 2010   Sheet 38 of 39		

+VGACORE +/- 5%  
 Countinue current:10A  
 Peak current:14A  
 OCP minimum 16A



0915 for EE BACO

0914 cost down

<8,9,17,29,35> DGPU\_PWROK

0910 for EE BACO mode request

0910 for AMD default

0910 for AMD default

<15> GFX\_CORE\_CNTRL0

<15> GFX\_CORE\_CNTRL1

Park-LP	PWRCNTL0	PWRCNTL1	V-CORE
L	0	0	0.9V
M	0	1	1V
H	1	0	1.1V (default)
TBD	1	1	NA

$V_o = 0.75 (R1 + R2) / R2$

100916 for EE power plane modify

100916 BACO function

0915 for EE BACO mode request



**PROJECT : R13**  
 Quanta Computer Inc.

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