

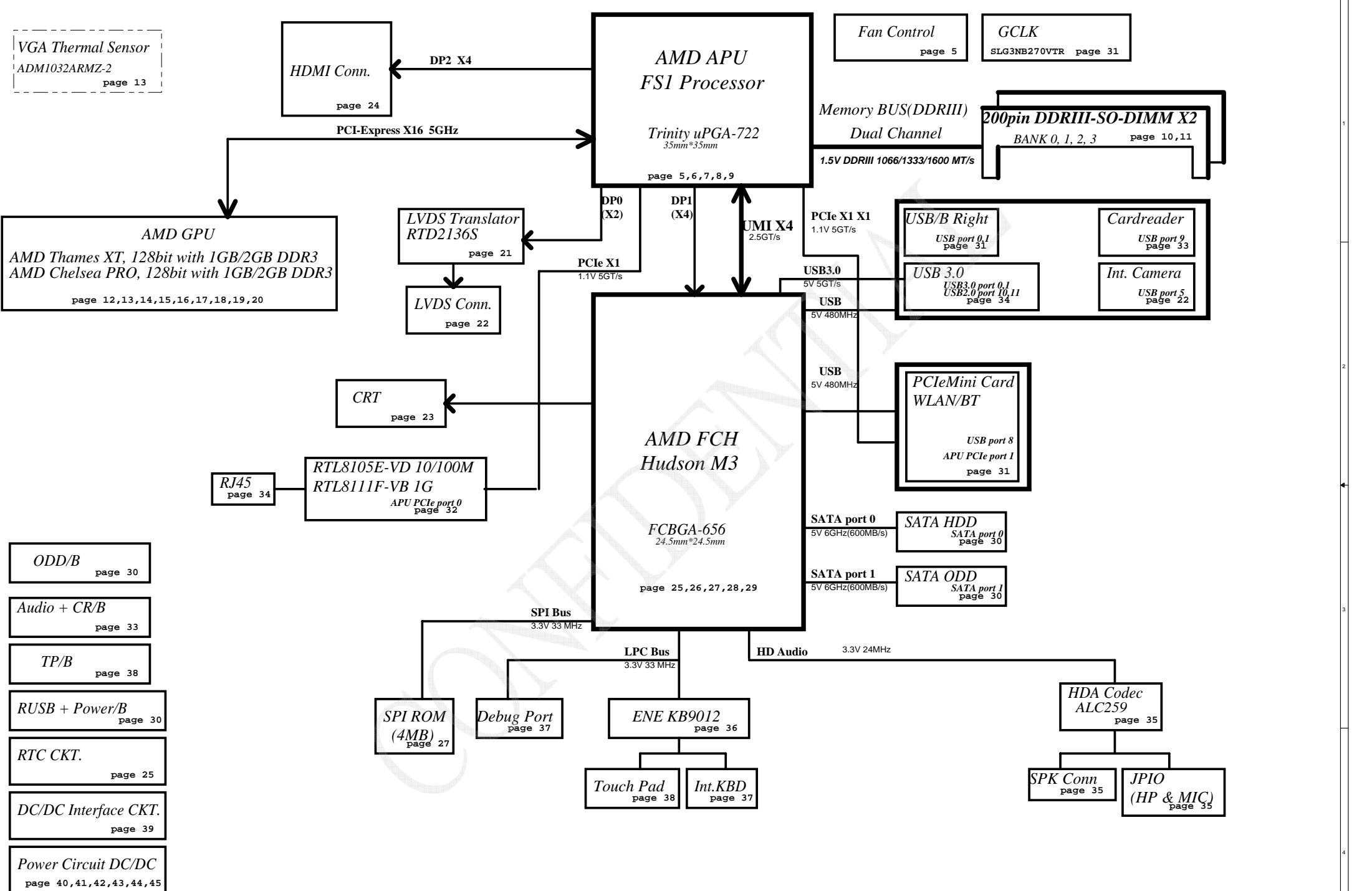
QMLE4/5

Eureka Discrete

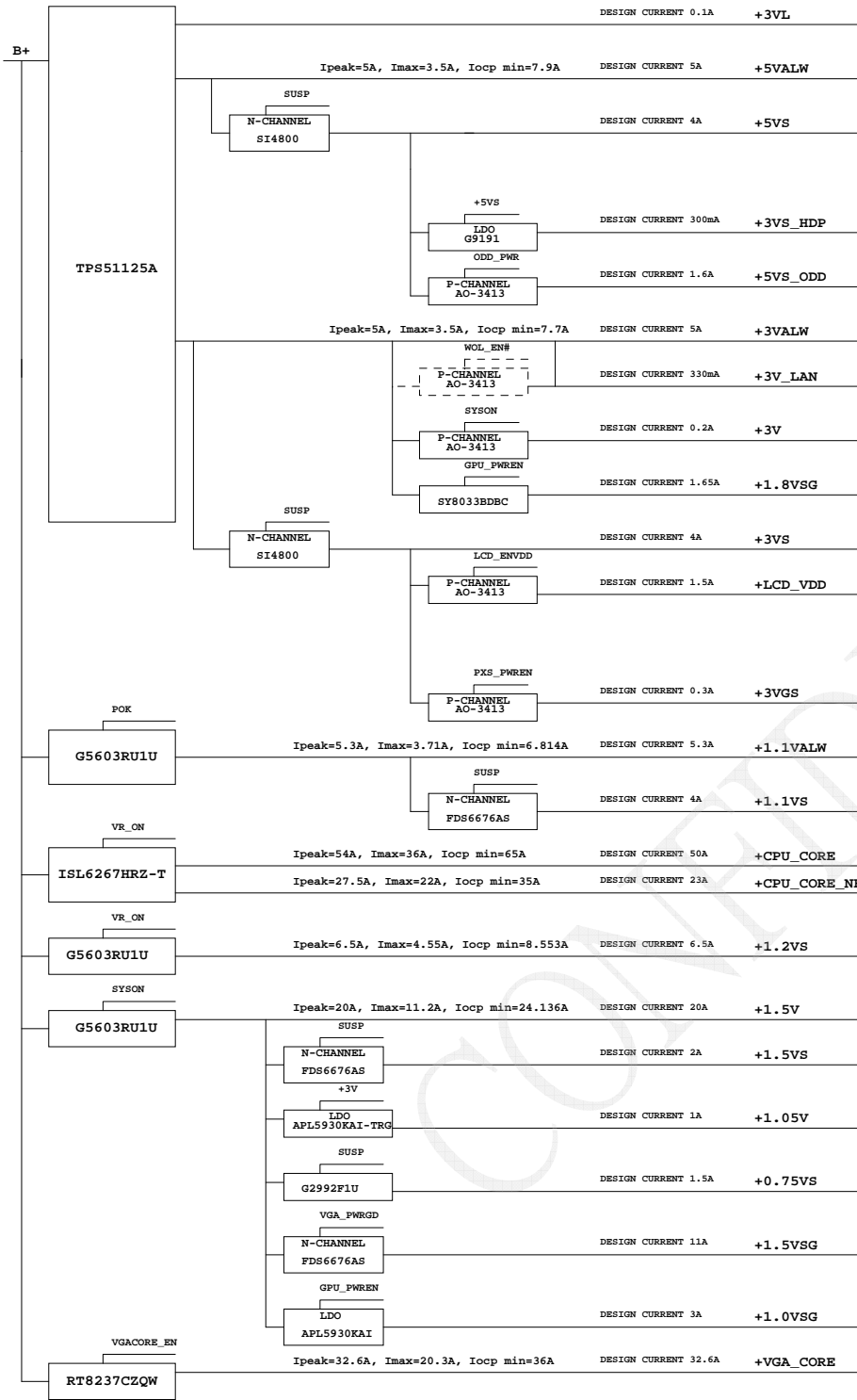
LA-8863P REV 0.3 Schematic

AMD Trinity APU / Hudson M3 FCH
Thames XT & Chelsea PRO
2012-03-13 Rev 0.3

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Voltage Rails

(O MEANS ON X MEANS OFF)

power plane / State	+RTCVC	B+	+5VL +3VL	+5VALW +3VALW +1.1VALW +VSB	+1.5V +3V +1.05V	+5VS +3VS +2.5VS +1.5VS +1.2VS +1.1VS +0.75VS +CPU_CORE +CPU_CORE_NB +VGA_CORE +3VGS +1.8VSG +1.5VSG +1.0VSG
	S0	O	O	O	O	O
S1	O	O	O	O	O	O
S3	O	O	O	O	O	X
S5 S4/AC	O	O	O	O	X	X
S5 S4/ Battery only	O	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X	X

BTO Option Table

Function	HDMI			SKU		
description	HDMI			SKU		
explain	UMA PowerXpress		COMMON	UMA	PowerXpress	Discrete
BTO	IHDMI@		HDMI@	UMA@	UMA@+VGA@+PXS@	VGA@+DIS@

Function	MINI PCI-E SLOT	LAN				
description		LAN				
explain		10/100M	GIGA			
BTO		8105ELDO@	8105ESWR@	8111E@		

Function		Cam & Mic	Panel		
description		Cam & Mic	Panel (DIS@)		
explain		Cam & Mic			
BTO		CAM@			

Function	GPIO for PowerXpress		Chipset			
description	PowerXpress (PXS@)		FCH		GPU	
explain	PowerXpress Enable	Crossfire Enable	Hudson-M3		Whistler Pro	
BTO	PXSEN@	CROSSEN@	HUDM3R1@	HUDM3R3@	WHPROR1@	WHPROR3@

Function	PowerXpress		FCH		
description	PowerXpress		FCH		
explain	BACO mode	Non-BACO	Hudson-M2	Hudson-M3	
BTO	BACO@	NOBACO@	M2@	M3@	

FCH SM Bus Address (SCL0/SDA0)



Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	90 H	1001 000xb
+3VS	DDR SO-DIMM 1	92 H	1001 001xb
+3VS	WLAN		

EC SM Bus1 Address

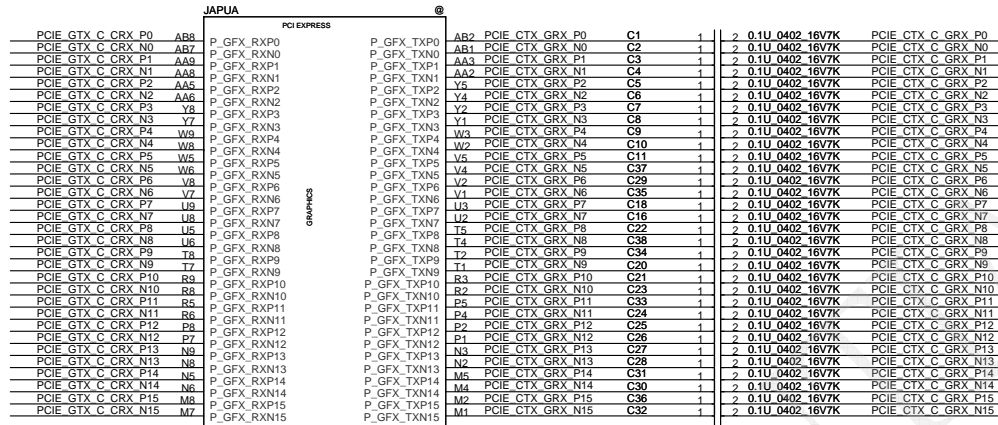
EC SM Bus2 Address

Power	Device	HEX	Address	Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 011x b	+3VS	APU Thermal Sensor	98 H	1001 100x b
+3VL	Charger IC	12 H	0001 001x b	+3VS	GPU Internal Thermal	82 H	1000 001x b
EC SM Bus3 Address				+3VS	GPU External Thermal	9A H	1001 101x b
+3VS	LVDS EEPROM	A8 H	1010 1000 b	+3VS	GPU External Thermal	9A H	1001 101x b

STATE	SIGNAL	SLP_S3#	SLP_S5#
Full ON		HIGH	HIGH
S1 (Power On Suspend)		HIGH	HIGH
S3 (Suspend to RAM)		LOW	HIGH
S4 (Suspend to Disk)		LOW	HIGH
S5 (Soft OFF)		LOW	LOW
G3		LOW	LOW

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 <12> PCIE_GTX_C_CRX_N[0..15] 

PCIE_CTX_C_GRX_P[0..15] <12> 
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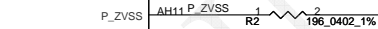
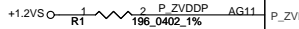


LAN <32> PCIE_FRX_C_LANTX_P0
 <32> PCIE_FRX_C_LANTX_N0
 <31> PCIE_FRX_WLANTX_P1
 <31> PCIE_FRX_WLANTX_N1

LAN <32> PCIE_FTX_C_LANRX_P0
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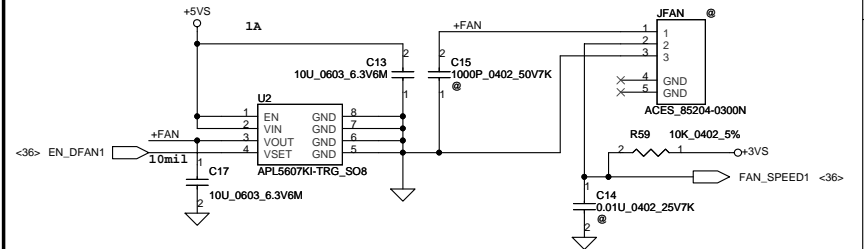
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 <25> UMI_MTX_C_FRX_N3

<25> UMI_FTX_C_MRX_P0
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 <25> UMI_FTX_C_MRX_P1
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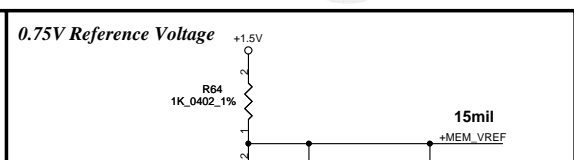
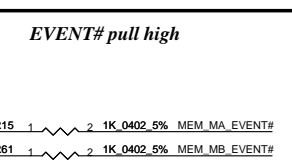
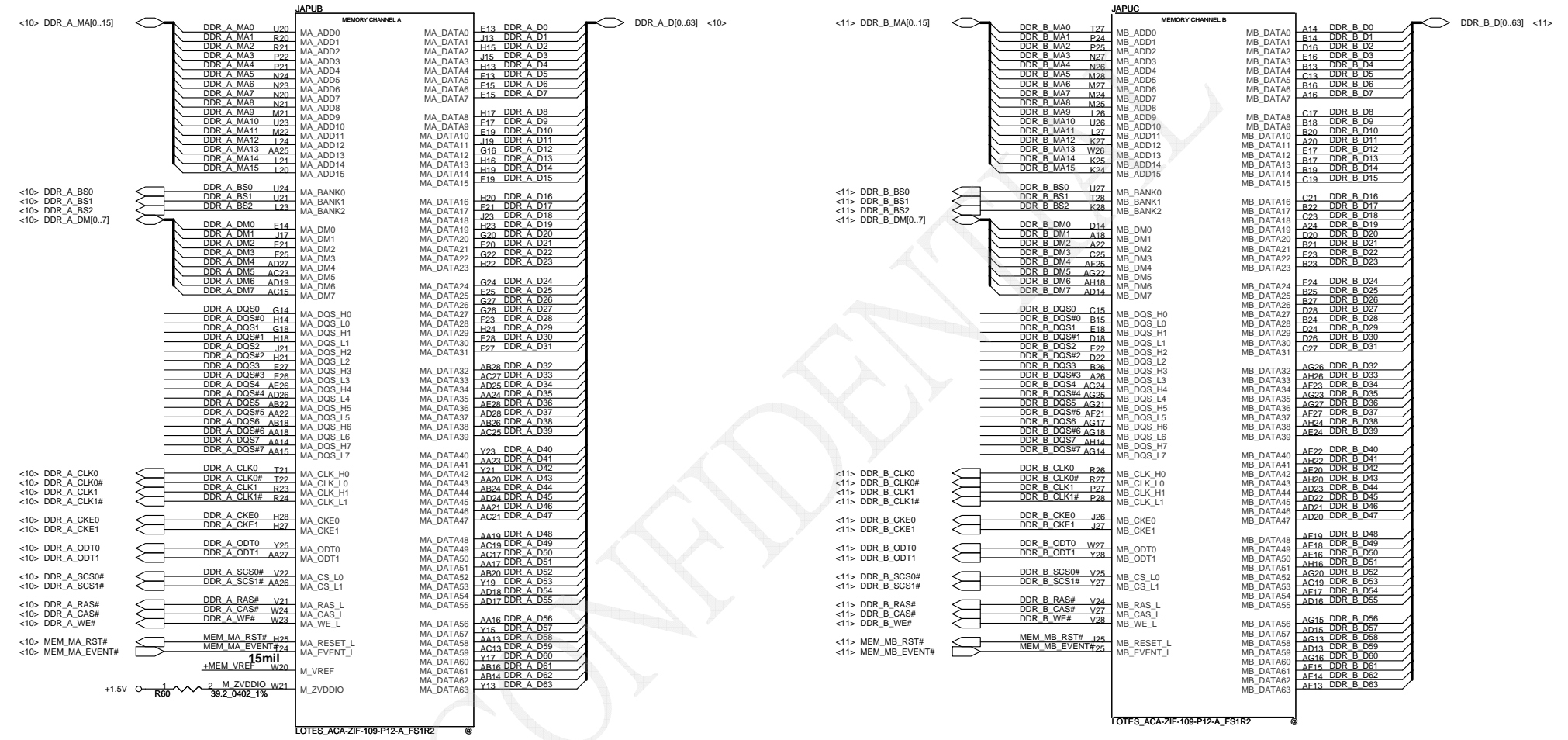
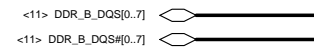
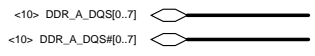


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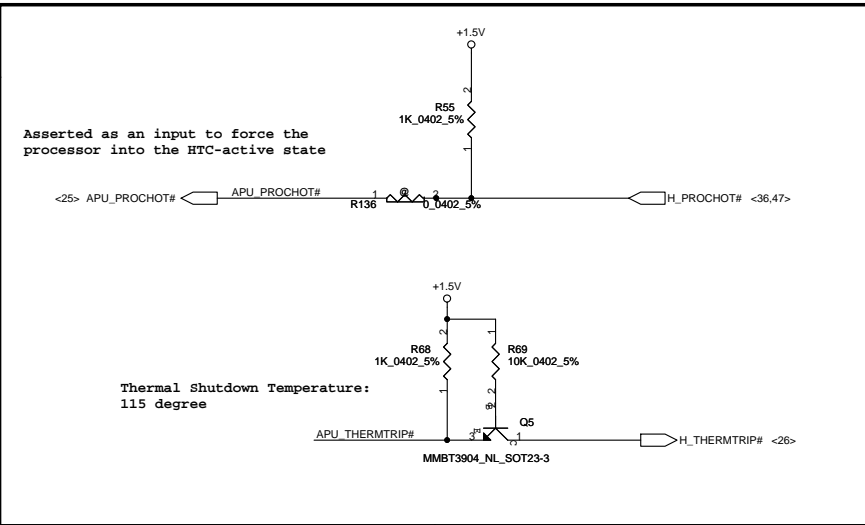
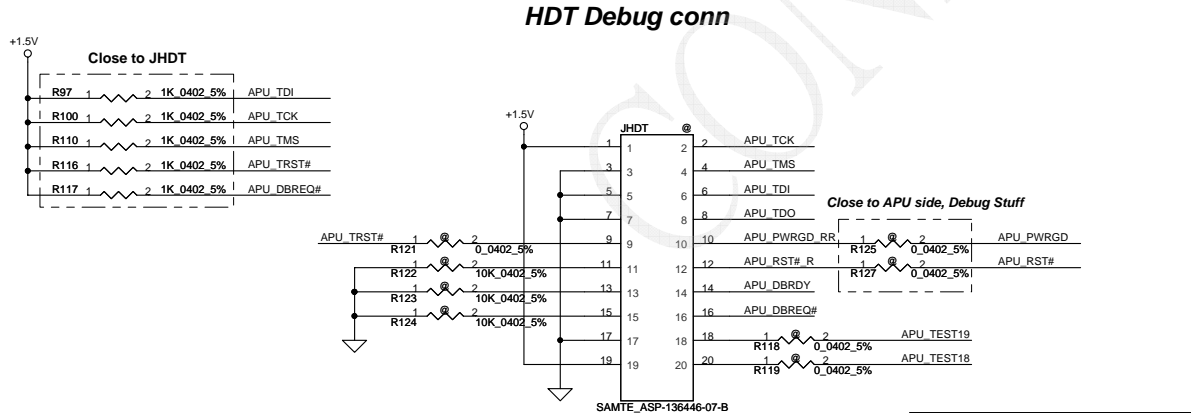
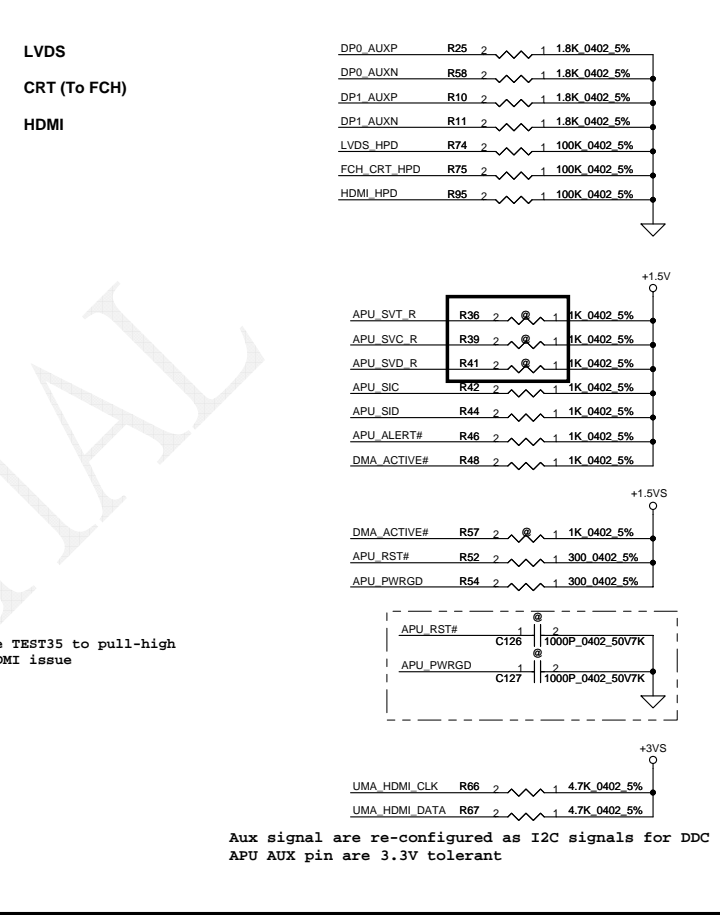
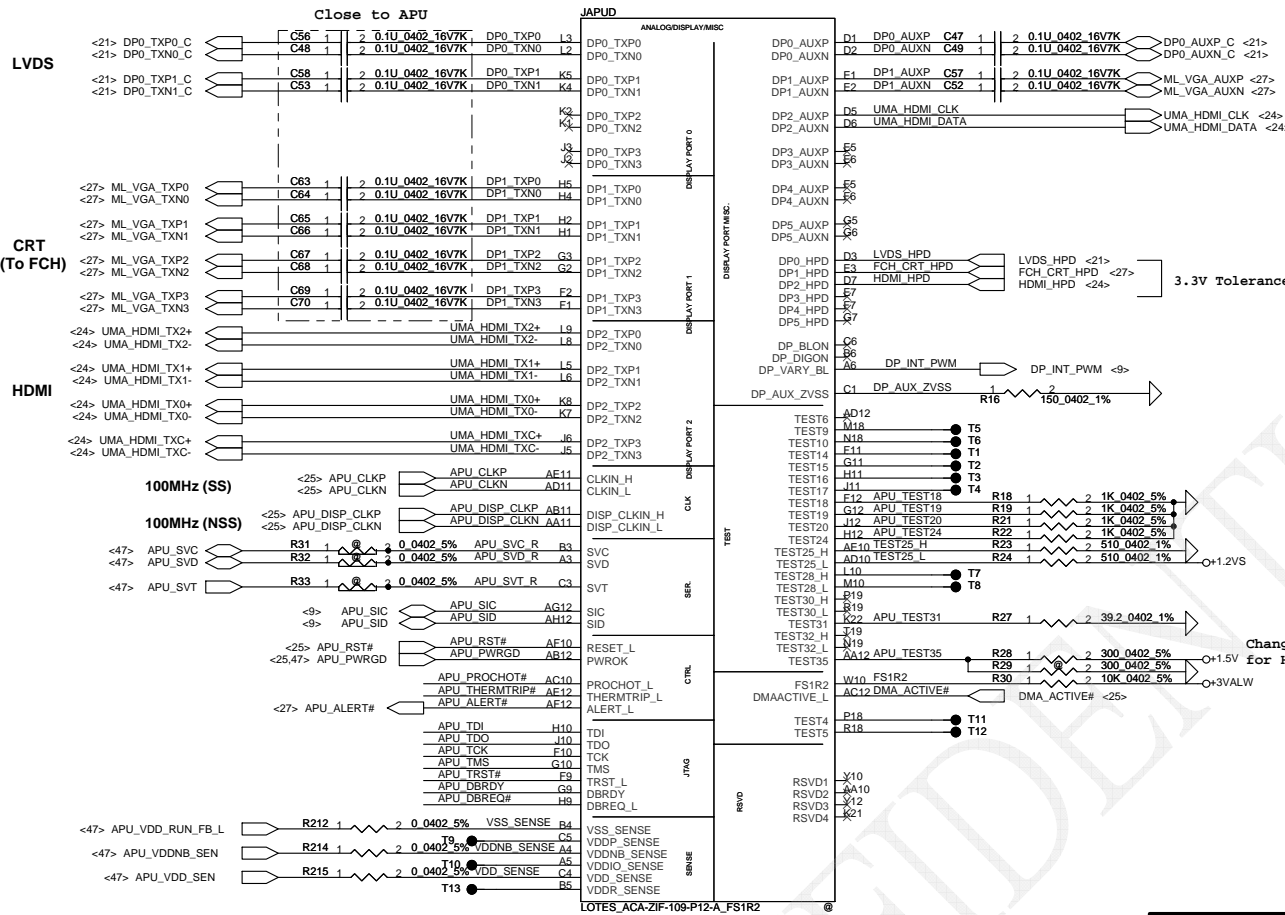
FAN Control Circuit



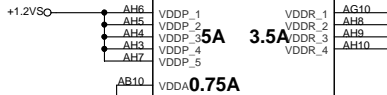
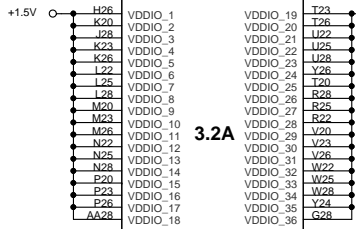
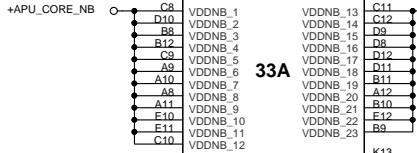
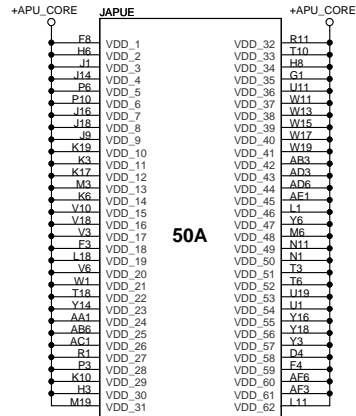
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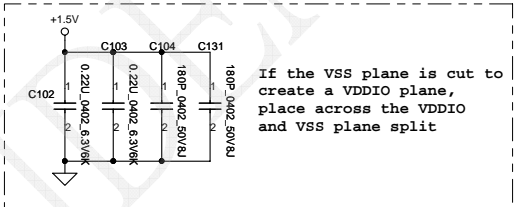
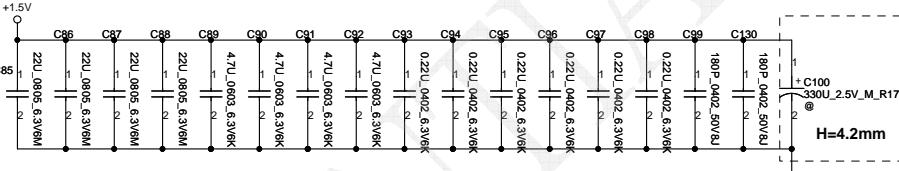
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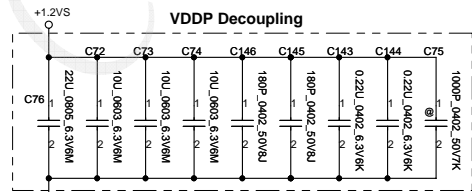
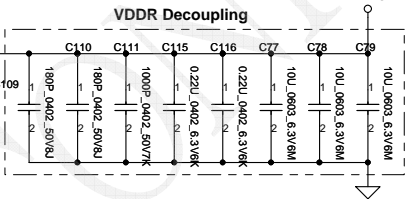
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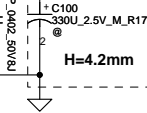
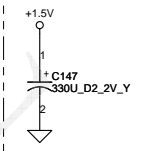
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If the VSS plane is cut to create a VDDIO plane, place across the VDDIO and VSS plane split



Co-layout with C100 on PVT



JAPUF

J20	VSS_1	VSS_73	A19
L4	VSS_74	VSS_74	A21
R7	VSS_3	VSS_75	A23
W18	VSS_4	VSS_76	A25
A15	VSS_5	VSS_77	A7
AB17	VSS_6	VSS_78	AA4
AC22	VSS_7	VSS_79	AA7
AE21	VSS_8	VSS_80	AB13
AF24	VSS_9	VSS_81	AB16
AH23	VSS_10	VSS_82	AB19
AH25	VSS_11	VSS_83	AB21
B7	VSS_12	VSS_84	AB23
C14	VSS_13	VSS_85	AB27
C2	VSS_14	VSS_86	AB9
C20	VSS_15	VSS_87	AC14
C22	VSS_16	VSS_88	AC16
C24	VSS_17	VSS_89	AC18
C26	VSS_18	VSS_90	AC20
C28	VSS_19	VSS_91	AC22
D13	VSS_20	VSS_92	AC24
D15	VSS_21	VSS_93	AC26
D17	VSS_22	VSS_94	AC4
D19	VSS_23	VSS_95	AC7
D23	VSS_24	VSS_96	AC11
D25	VSS_25	VSS_97	AD3
D27	VSS_26	VSS_98	AE13
D29	VSS_27	VSS_99	AE15
E4	VSS_28	VSS_100	AE17
E9	VSS_29	VSS_101	M9
F14	VSS_30	VSS_102	N4
F16	VSS_31	VSS_103	N7
F18	VSS_32	VSS_104	N7
F20	VSS_33	VSS_105	R10
F22	VSS_34	VSS_106	T11
F26	VSS_35	VSS_107	R4
F28	VSS_36	VSS_108	T9
G15	VSS_37	VSS_109	U10
G17	VSS_38	VSS_110	U4
G19	VSS_39	VSS_111	U7
G21	VSS_40	VSS_112	V11
G23	VSS_41	VSS_113	V11
G26	VSS_42	VSS_114	AE19
G4	VSS_43	VSS_115	AE23
J22	VSS_44	VSS_116	AE25
J24	VSS_45	VSS_117	AE27
J4	VSS_46	VSS_118	AE4
J7	VSS_47	VSS_119	AE7
J7	VSS_48	VSS_120	AE14
K11	VSS_49	VSS_121	AE16
K14	VSS_50	VSS_122	AE18
K9	VSS_51	VSS_123	AE20
AC11	VSS_52	VSS_124	AE22
L19	VSS_53	VSS_125	AE26
L7	VSS_54	VSS_126	AE28
M11	VSS_55	VSS_127	AE9
AG11	VSS_56	VSS_128	AG4
V19	VSS_57	VSS_129	AG7
V9	VSS_58	VSS_130	AH13
W16	VSS_59	VSS_131	AH15
W4	VSS_60	VSS_132	AH17
w7	VSS_61	VSS_133	AH19
Y11	VSS_62	VSS_134	AH21
V20	VSS_63	VSS_135	P3
Y22	VSS_64	VSS_136	C18
Y9	VSS_65	VSS_138	D21
A17	VSS_66	VSS_138	W14
A13	VSS_67	VSS_139	P17
K16	VSS_68	VSS_140	C7
F24	VSS_69	VSS_141	E8
G8	VSS_70	VSS_142	K18
H7	VSS_71	VSS_143	W12
I8	VSS_72	VSS_143	I8

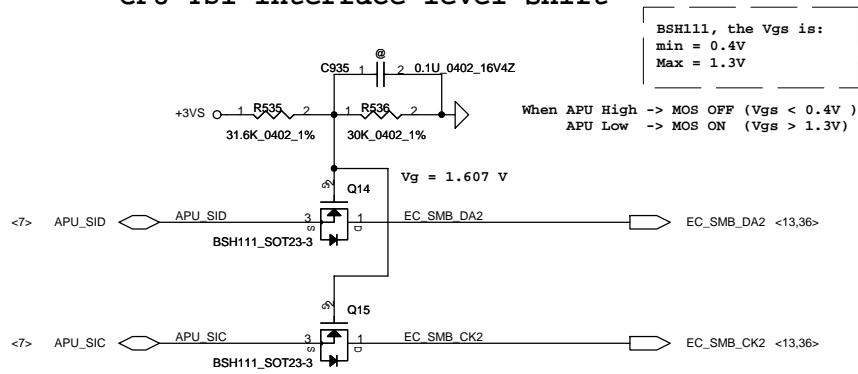
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Demo Board Capacitor

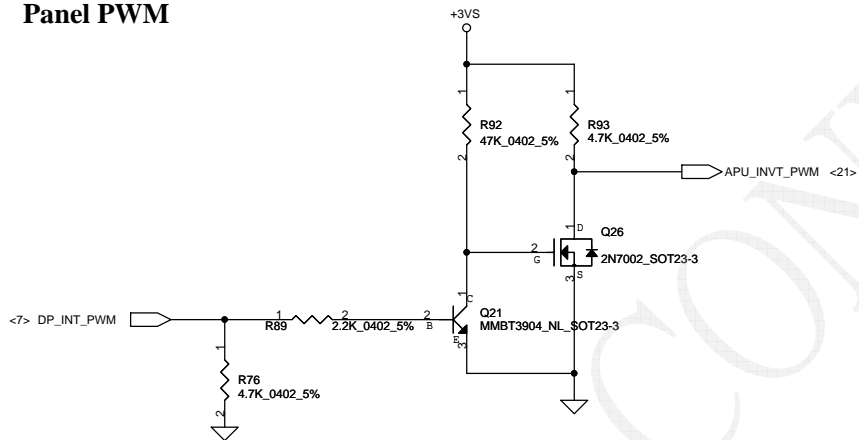
APU_CORE 22uF x 10 0.22uF x 2 0.01uF x 3 180pF x 2	CORE_NB 22uF x 2 10uF x 1 0.22uF x 2 180pF x 3	CORE_NB_CAP 180pF x 1 0.22uF x 6 +2(split) 180pF x 1 + 2(split)	VDDIO_SUS (CPU side) 22uF x 4 4.7uF x 4 0.22uF x 6 +2(split) 180pF x 1 + 2(split)
VDDP 0.22uF x 2 180pF x 2	VDDR 0.22uF x 2 1nF x 1 180pF x 2	VDDA 4.7uF x 1 0.22uF x 1 3.3nF x 1	VDDIO_SUS (DIMM x2) 100uF x 2 0.1uF x 12

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CPU TSI interface level shift

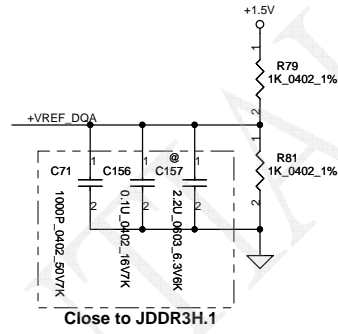
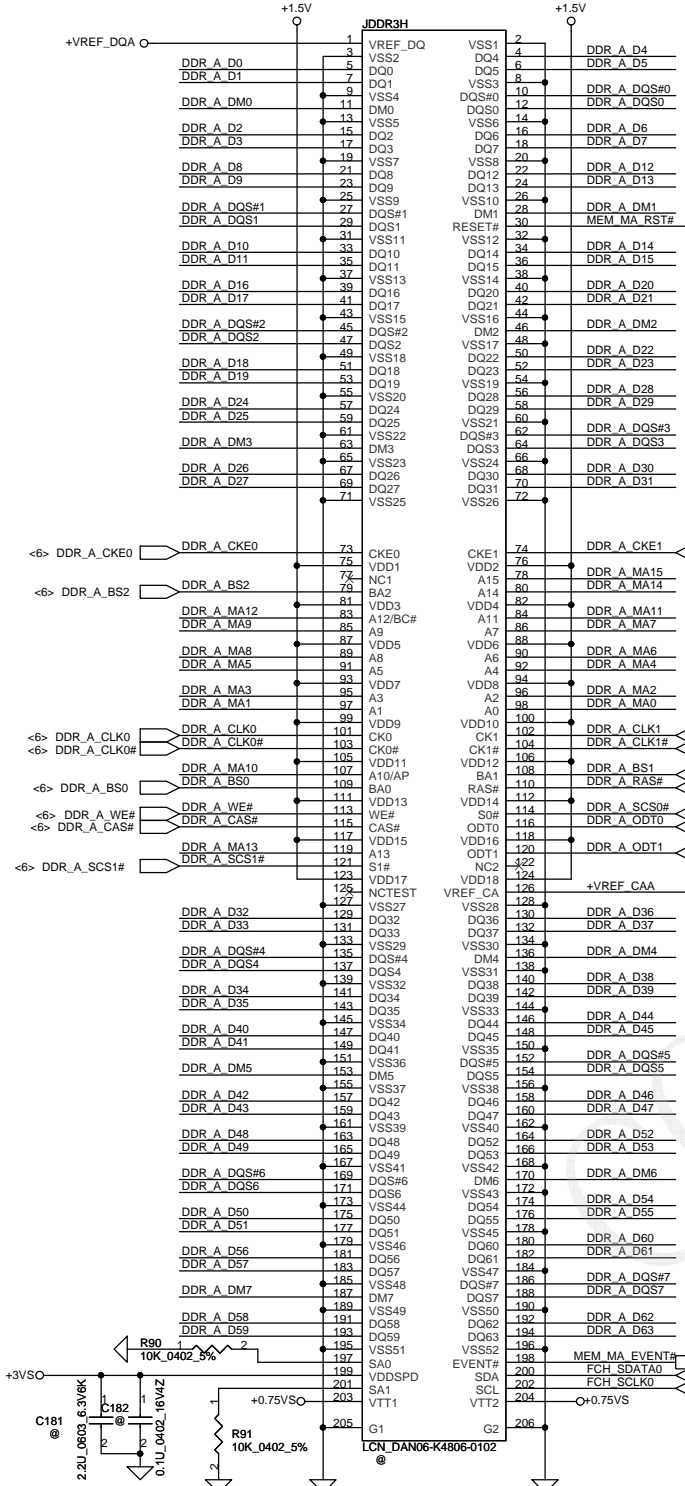


Panel PWM

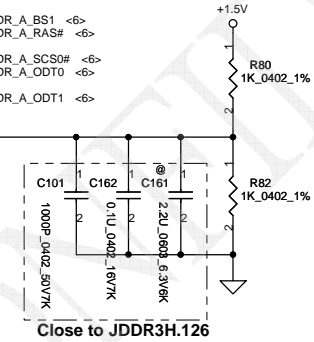
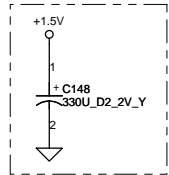


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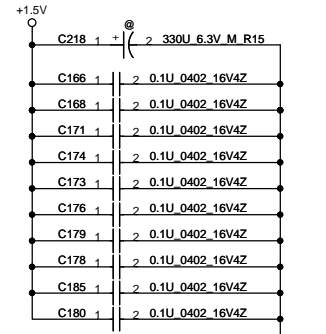
DDR3 SO-DIMM A Standard Type



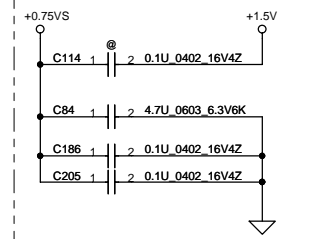
Co-layout with C218 on PVT



Layout Note:
Place near JDDR3H



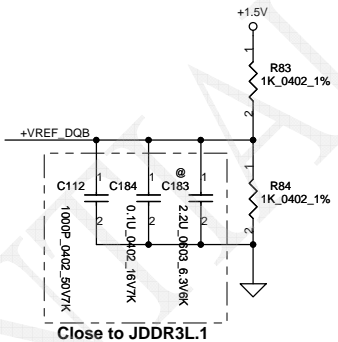
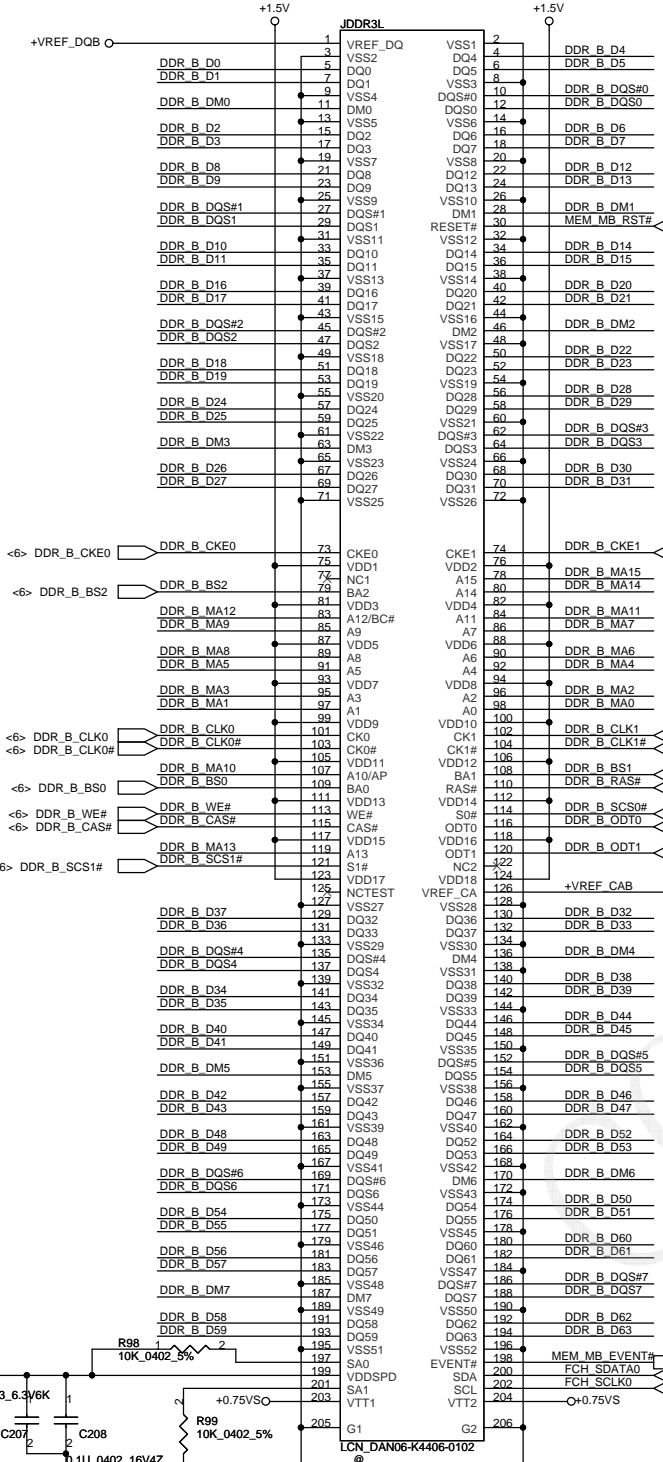
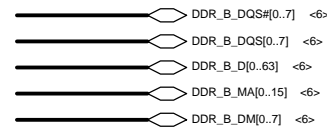
Layout Note:
Place near JDDR3H.203 and 204



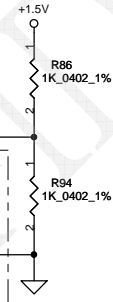
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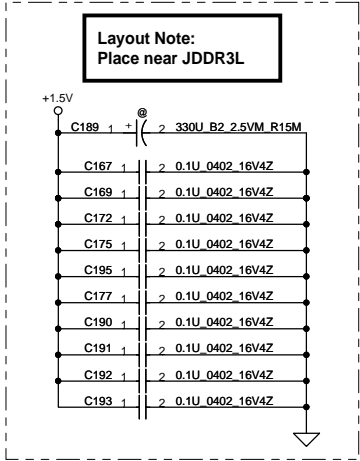
DDR3 SO-DIMM B Standard Type



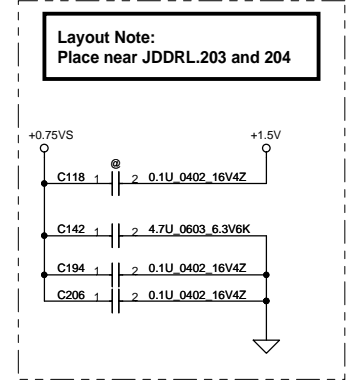
Close to JDDR3L.1



Close to JDDR3L.126



Layout Note:
Place near JDDR3L



Layout Note:
Place near JDDR.L203 and 204

Change SODIMM1 Smbus address to A2(SA0=1, SA1=0) on DVT

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<5> PCIE_CTX_C_GRX_P[0..15] PCIE_CTX_C_GRX_P[0..15]
 <5> PCIE_CTX_C_GRX_N[0..15] PCIE_CTX_C_GRX_N[0..15]

PCIE GTX_C_CRX_P[0..15] PCIE GTX_C_CRX_P[0..15] <5>
 PCIE GTX_C_CRX_N[0..15] PCIE GTX_C_CRX_N[0..15] <5>

Close to UV1

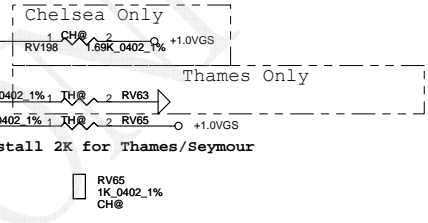
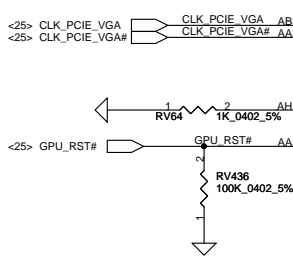
PCIE_CTX_C_GRX_P	PCIE_CTX_C_GRX_N	PCIE_TX0P	PCIE_TX0N	PCIE_TX1P	PCIE_TX1N	PCIE_TX2P	PCIE_TX2N	PCIE_TX3P	PCIE_TX3N	PCIE_TX4P	PCIE_TX4N	PCIE_TX5P	PCIE_TX5N	PCIE_TX6P	PCIE_TX6N	PCIE_TX7P	PCIE_TX7N	PCIE_TX8P	PCIE_TX8N	PCIE_TX9P	PCIE_TX9N	PCIE_TX10P	PCIE_TX10N	PCIE_TX11P	PCIE_TX11N	PCIE_TX12P	PCIE_TX12N	PCIE_TX13P	PCIE_TX13N	PCIE_TX14P	PCIE_TX14N	PCIE_TX15P	PCIE_TX15N
AA38	Y37	Y33	Y32	W33	W32	U33	U32	U30	U29	T33	T32	T30	T29	P33	P32	P30	P29	N33	N32	N30	N29	L33	L32	L30	L29	K33	K32	J33	J32	K30	K29	H33	H32
PCIE GTX_C_CRX P0	PCIE GTX_C_CRX N0	PCIE GTX_C_CRX P0	PCIE GTX_C_CRX N0	PCIE GTX_C_CRX P1	PCIE GTX_C_CRX N1	PCIE GTX_C_CRX P2	PCIE GTX_C_CRX N2	PCIE GTX_C_CRX P3	PCIE GTX_C_CRX N3	PCIE GTX_C_CRX P4	PCIE GTX_C_CRX N4	PCIE GTX_C_CRX P5	PCIE GTX_C_CRX N5	PCIE GTX_C_CRX P6	PCIE GTX_C_CRX N6	PCIE GTX_C_CRX P7	PCIE GTX_C_CRX N7	PCIE GTX_C_CRX P8	PCIE GTX_C_CRX N8	PCIE GTX_C_CRX P9	PCIE GTX_C_CRX N9	PCIE GTX_C_CRX P10	PCIE GTX_C_CRX N10	PCIE GTX_C_CRX P11	PCIE GTX_C_CRX N11	PCIE GTX_C_CRX P12	PCIE GTX_C_CRX N12	PCIE GTX_C_CRX P13	PCIE GTX_C_CRX N13	PCIE GTX_C_CRX P14	PCIE GTX_C_CRX N14	PCIE GTX_C_CRX P15	PCIE GTX_C_CRX N15
0.1U 0402 16V7K	0.1U 0402 16V7K	0.1U 0402 16V7K	0.1U 0402 16V7K	0.1U 0402 16V7K	0.1U 0402 16V7K	0.1U 0402 16V7K	0.1U 0402 16V7K	0.1U 0402 16V7K	0.1U 0402 16V7K	0.1U 0402 16V7K	0.1U 0402 16V7K	0.1U 0402 16V7K	0.1U 0402 16V7K	0.1U 0402 16V7K	0.1U 0402 16V7K	0.1U 0402 16V7K	0.1U 0402 16V7K	0.1U 0402 16V7K	0.1U 0402 16V7K	0.1U 0402 16V7K	0.1U 0402 16V7K	0.1U 0402 16V7K	0.1U 0402 16V7K	0.1U 0402 16V7K	0.1U 0402 16V7K	0.1U 0402 16V7K	0.1U 0402 16V7K	0.1U 0402 16V7K	0.1U 0402 16V7K	0.1U 0402 16V7K	0.1U 0402 16V7K	0.1U 0402 16V7K	
2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
CV73	CV74	CV71	CV72	CV69	CV70	CV67	CV68	CV65	CV66	CV63	CV64	CV61	CV62	CV59	CV60	CV57	CV58	CV55	CV56	CV53	CV54	CV51	CV52	CV49	CV50	CV47	CV48	CV45	CV46	CV43	CV44		
PCIE GTX_C_CRX P0	PCIE GTX_C_CRX N0	PCIE GTX_C_CRX P1	PCIE GTX_C_CRX N1	PCIE GTX_C_CRX P2	PCIE GTX_C_CRX N2	PCIE GTX_C_CRX P3	PCIE GTX_C_CRX N3	PCIE GTX_C_CRX P4	PCIE GTX_C_CRX N4	PCIE GTX_C_CRX P5	PCIE GTX_C_CRX N5	PCIE GTX_C_CRX P6	PCIE GTX_C_CRX N6	PCIE GTX_C_CRX P7	PCIE GTX_C_CRX N7	PCIE GTX_C_CRX P8	PCIE GTX_C_CRX N8	PCIE GTX_C_CRX P9	PCIE GTX_C_CRX N9	PCIE GTX_C_CRX P10	PCIE GTX_C_CRX N10	PCIE GTX_C_CRX P11	PCIE GTX_C_CRX N11	PCIE GTX_C_CRX P12	PCIE GTX_C_CRX N12	PCIE GTX_C_CRX P13	PCIE GTX_C_CRX N13	PCIE GTX_C_CRX P14	PCIE GTX_C_CRX N14	PCIE GTX_C_CRX P15	PCIE GTX_C_CRX N15		

PCI EXPRESS INTERFACE

LVDS Interface

LVDS CONTROL	VARY_BLDIGON	AK27	AK27
TXCLK_UP_DPF3P	TXCLK_UN_DPF3N	AK35	AK36
TXOUT_U0P_DPF2P	TXOUT_U0N_DPF2N	AK38	AK37
TXOUT_U1P_DPF1P	TXOUT_U1N_DPF1N	AH35	AH36
TXOUT_U2P_DPF0P	TXOUT_U2N_DPF0N	AG38	AH37
TXOUT_U3P	TXOUT_U3N	AF35	AG36
TXCLK_LP_DPE3P	TXCLK_LN_DPE3N	AP34	AR34
TXOUT_L0P_DPE2P	TXOUT_L0N_DPE2N	AW37	AL35
TXOUT_L1P_DPE1P	TXOUT_L1N_DPE1N	AR37	AL37
TXOUT_L2P_DPE0P	TXOUT_L2N_DPE0N	AP35	AR35
TXOUT_L3P	TXOUT_L3N	AN36	AR37

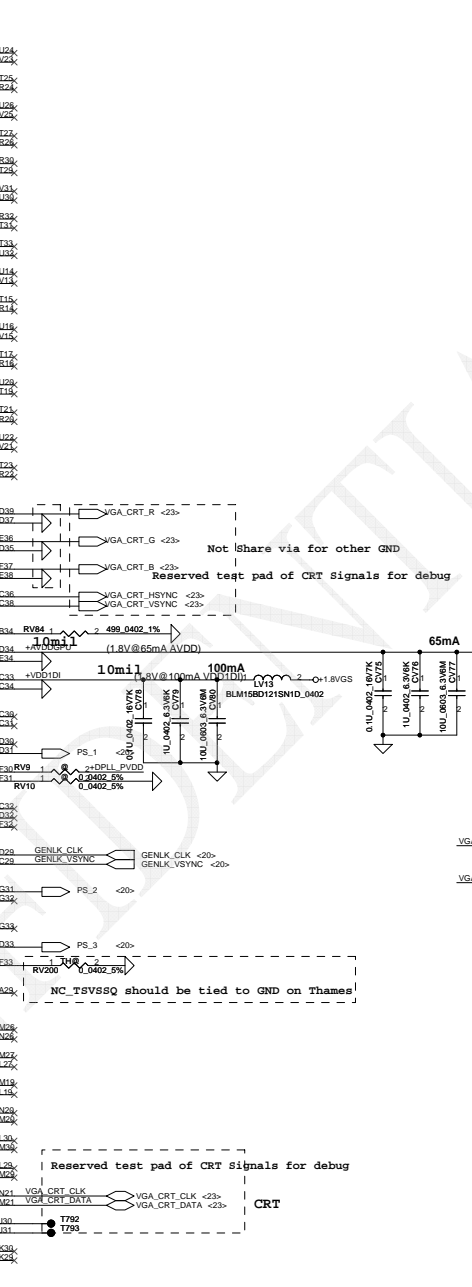
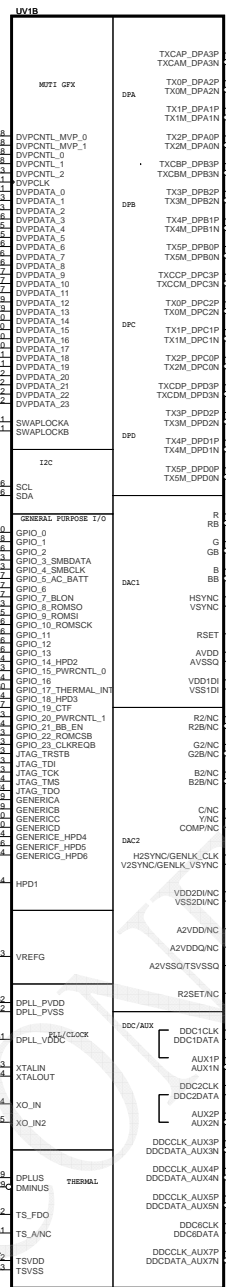
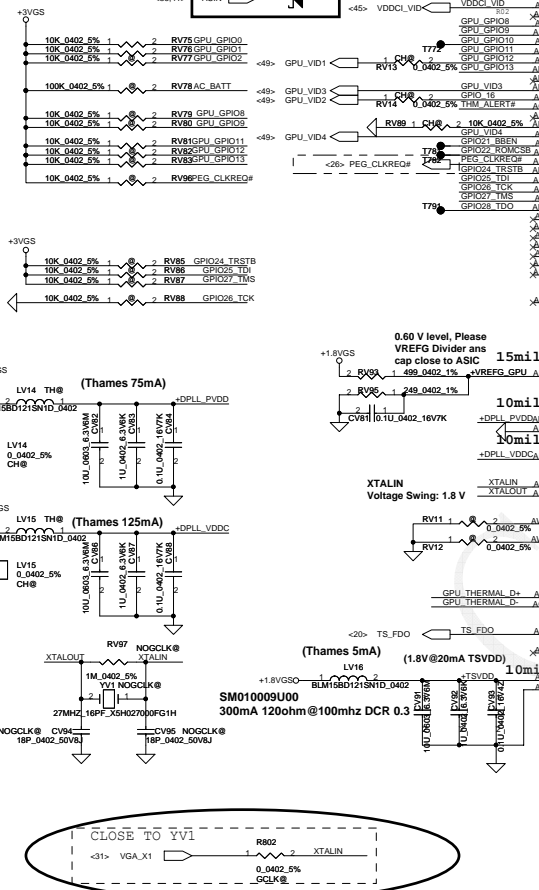
THAMES XT M2 TH@



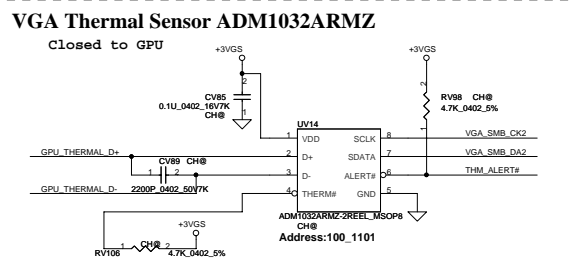
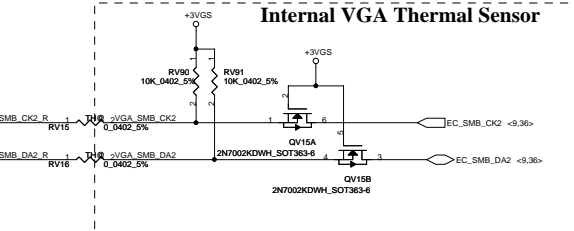
THAMES XT M2 THR3@
 Need to modify P/N

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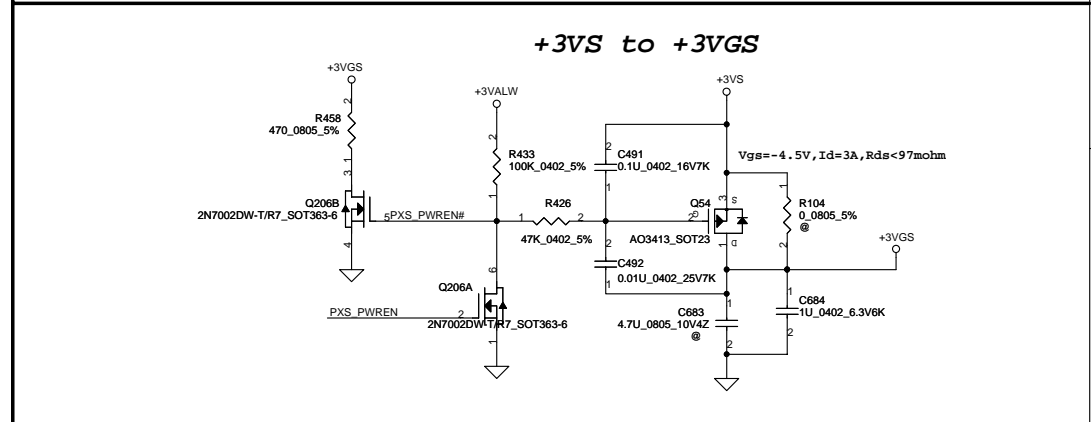
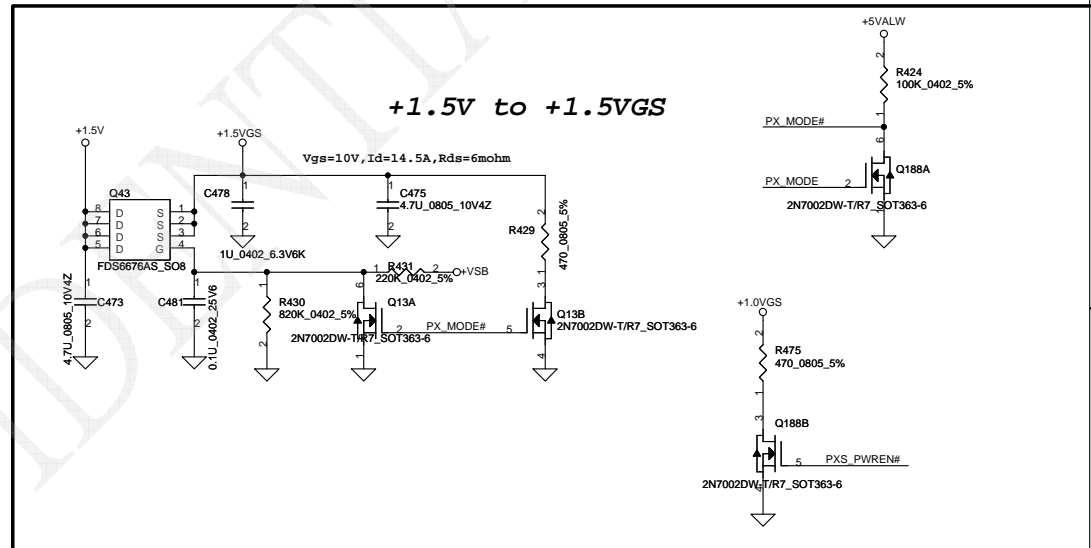
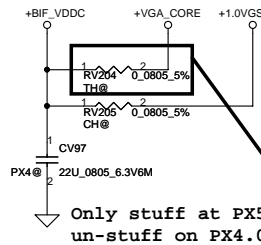
STRAPS



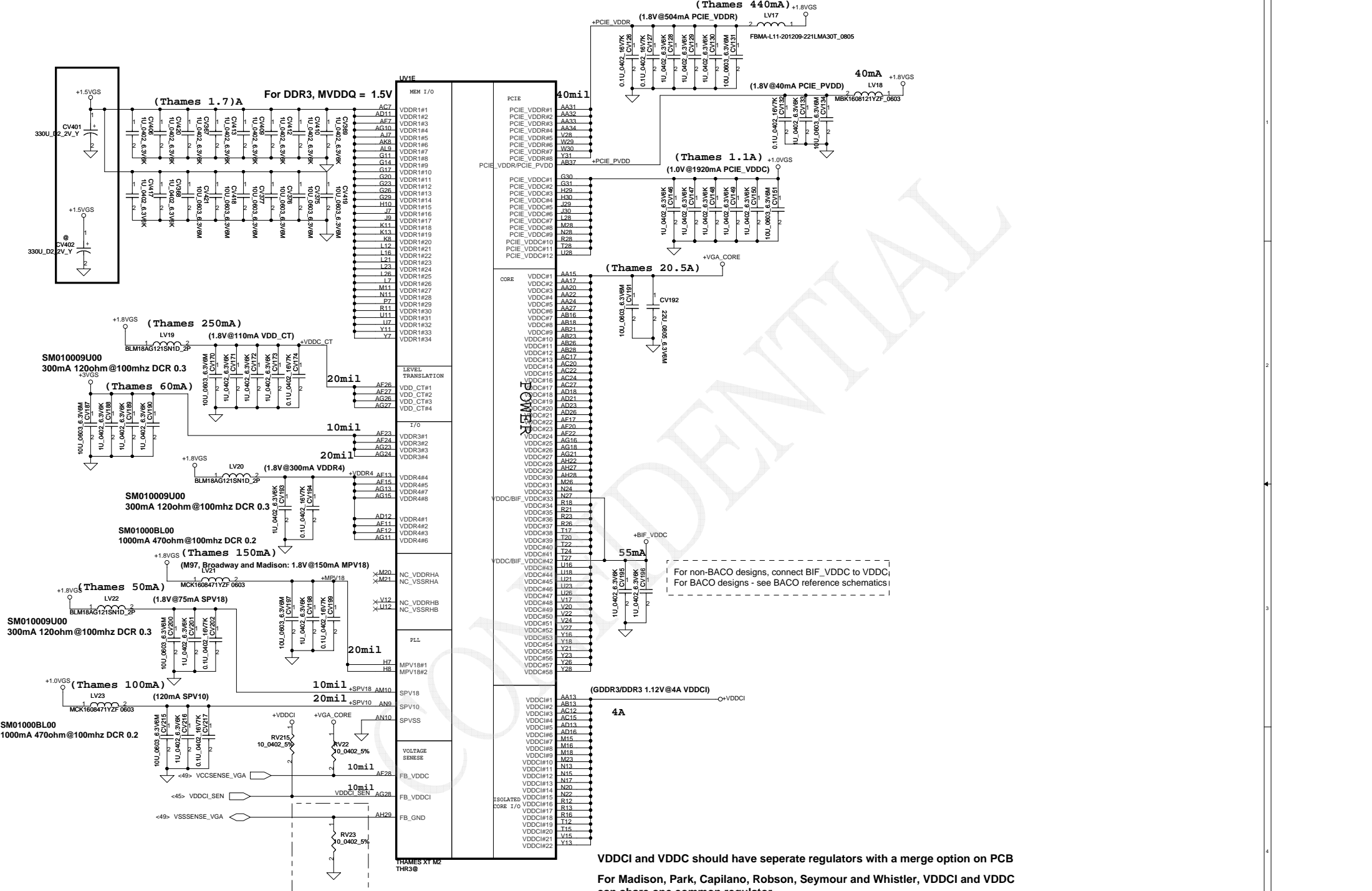
TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for desktop)



<25,26,44,49> PXS_PWREN PXS_PWREN RV102 1 0.0402_5% PX_MODE PX_MODE <45,49>
 for PX5.0 PX_MODE=1 for Normal Operation
 PX_MODE=0 to shut down VDDR3, PCIE_VDDC, 1.5VGS and 1.8VGS power rails



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VDDCI and VDDC should have separate regulators with a merge option on PCB
 For Madison, Park, Capilano, Robson, Seymour and Whistler, VDDCI and VDDC can share one common regulator

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UV1F

- AB39 PCIE_VSS#1
- E39 PCIE_VSS#2
- F34 PCIE_VSS#3
- F39 PCIE_VSS#4
- G33 PCIE_VSS#5
- G34 PCIE_VSS#6
- H31 PCIE_VSS#7
- H34 PCIE_VSS#8
- H39 PCIE_VSS#9
- J11 PCIE_VSS#10
- J34 PCIE_VSS#11
- K31 PCIE_VSS#12
- K34 PCIE_VSS#13
- K39 PCIE_VSS#14
- L31 PCIE_VSS#15
- L34 PCIE_VSS#16
- M34 PCIE_VSS#17
- M39 PCIE_VSS#18
- N31 PCIE_VSS#19
- N34 PCIE_VSS#20
- P31 PCIE_VSS#21
- P34 PCIE_VSS#22
- P39 PCIE_VSS#23
- R34 PCIE_VSS#24
- T31 PCIE_VSS#25
- T34 PCIE_VSS#26
- T39 PCIE_VSS#27
- U31 PCIE_VSS#28
- U34 PCIE_VSS#29
- V34 PCIE_VSS#30
- V39 PCIE_VSS#31
- W31 PCIE_VSS#32
- W34 PCIE_VSS#33
- Y34 PCIE_VSS#34
- Y39 PCIE_VSS#35

GND

- F15 GND#100
- F17 GND#101
- F19 GND#102
- F21 GND#103
- F23 GND#104
- F25 GND#105
- F27 GND#106
- F29 GND#107
- F31 GND#108
- F33 GND#109
- F7 GND#110
- F9 GND#111
- G2 GND#112
- G6 GND#113
- H9 GND#114
- J2 GND#115
- J27 GND#116
- J6 GND#117
- K4 GND#118
- K14 GND#119
- K7 GND#120
- L11 GND#121
- L17 GND#122
- L2 GND#123
- L22 GND#124
- L24 GND#125
- L6 GND#126
- M17 GND#127
- M22 GND#128
- M24 GND#129
- N16 GND#130
- N2 GND#131
- N19 GND#132
- N21 GND#133
- N23 GND#134
- N28 GND#135
- N6 GND#136
- R15 GND#137
- R17 GND#138
- R20 GND#139
- R22 GND#140
- R24 GND#141
- R27 GND#142
- R6 GND#143
- T11 GND#144
- T13 GND#145
- T18 GND#146
- T19 GND#147
- T23 GND#148
- T26 GND#149
- U15 GND#150
- U17 GND#151
- U2 GND#152
- U22 GND#153
- U24 GND#154
- U27 GND#155
- U6 GND#156
- V11 GND#157
- V16 GND#158
- V18 GND#159
- V21 GND#160
- V23 GND#161
- V26 GND#162
- W2 GND#163
- W6 GND#164
- Y15 GND#165
- Y17 GND#166
- Y20 GND#167
- Y22 GND#168
- Y24 GND#169
- Y27 GND#170
- U13 GND#171
- U15 GND#172
- V13 GND#173

- A3 GND#1
- A37 GND#2
- AA16 GND#3
- AA18 GND#4
- AA2 GND#5
- AA21 GND#6
- AA23 GND#7
- AA26 GND#8
- AA28 GND#9
- AA6 GND#10
- AB12 GND#11
- AB15 GND#12
- AB17 GND#13
- AB20 GND#14
- AB22 GND#15
- AB24 GND#16
- AB27 GND#17
- AC11 GND#18
- AC13 GND#19
- AC16 GND#20
- AC18 GND#21
- AC2 GND#22
- AC21 GND#23
- AC22 GND#24
- AC23 GND#25
- AC26 GND#26
- AC28 GND#27
- AD15 GND#28
- AD17 GND#29
- AD20 GND#30
- AD22 GND#31
- AD24 GND#32
- AD27 GND#33
- AD9 GND#34
- AE6 GND#35
- AF10 GND#36
- AF16 GND#37
- AF18 GND#38
- AF21 GND#39
- AG17 GND#40
- AG2 GND#41
- AG20 GND#42
- AG22 GND#43
- AG6 GND#44
- AG9 GND#45
- AH21 GND#46
- AH10 GND#47
- AJ11 GND#48
- AJ2 GND#49
- AJ28 GND#50
- AK6 GND#51
- AK11 GND#52
- AK31 GND#53
- AK7 GND#54
- AL11 GND#55
- AL14 GND#56
- AL17 GND#57
- AL2 GND#58
- AL20 GND#59
- AL21 GND#60
- AL23 GND#61
- AL26 GND#62
- AL32 GND#63
- AL6 GND#64
- AL8 GND#65
- AM11 GND#66
- AM31 GND#67
- AM9 GND#68
- AN2 GND#69
- AN11 GND#70
- AN20 GND#71
- AN30 GND#72
- AN8 GND#73
- AN9 GND#74
- AP11 GND#75
- AP7 GND#76
- AR9 GND#77
- AR5 GND#78
- B11 GND#79
- B13 GND#80
- B15 GND#81
- B17 GND#82
- B19 GND#83
- B21 GND#84
- B23 GND#85
- B25 GND#86
- B27 GND#87
- B29 GND#88
- B31 GND#89
- B33 GND#90
- B7 GND#91
- R9 GND#92
- C1 GND#93
- C30 GND#94
- E35 GND#95
- E6 GND#96
- F11 GND#97
- F13 GND#98

VSS_MECH#1
VSS_MECH#2
VSS_MECH#3

A39 MECH#1
AW1 MECH#2
AW39 MECH#3

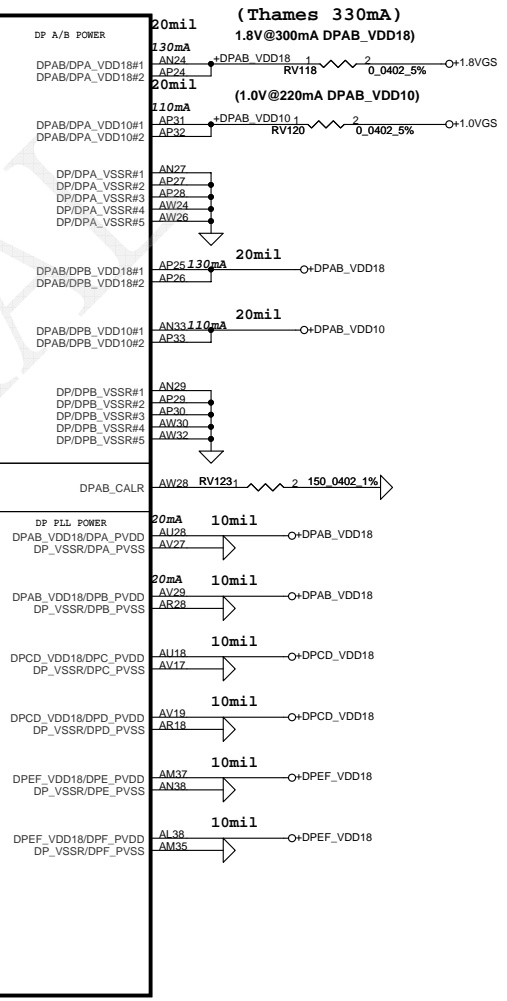
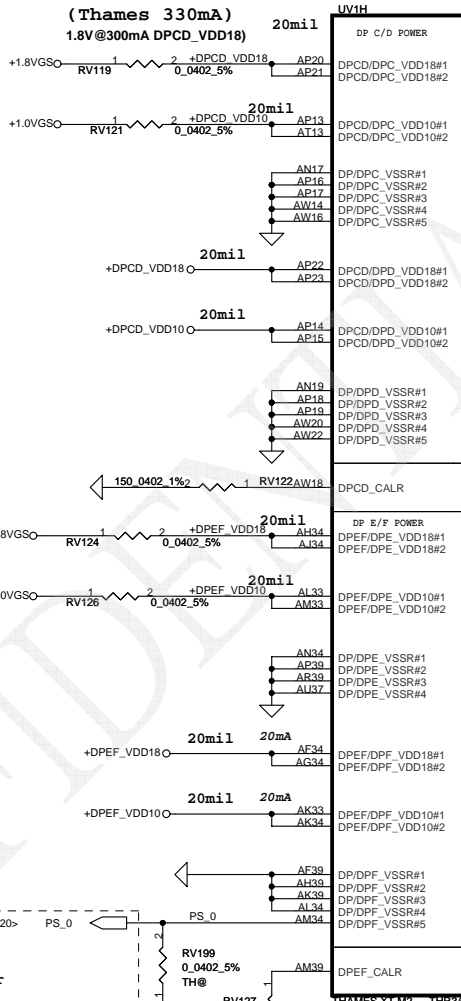
T821PAD
T831PAD
T841PAD

(Thames 220mA)
1.0V@220mA DPCD_VDD10

(Thames 330mA)
1.8V@300mA DPCD_VDD18

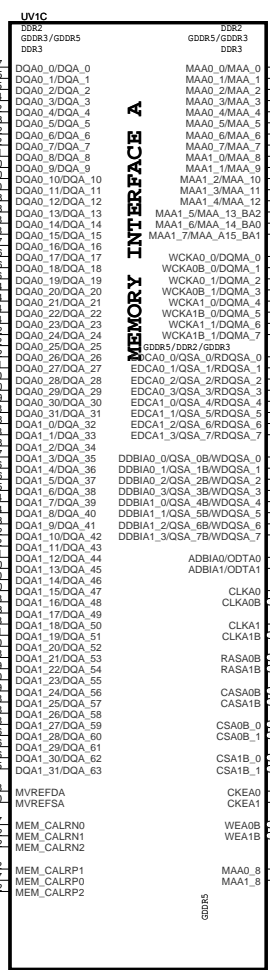
1.8V@300mA DPEF_VDD18
(Thames 330mA)

1.0V@240mA DPEF_VDD10
(Thames 220mA)



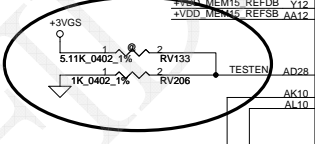
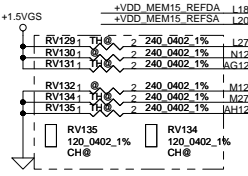
Thames/Seymour Only
Do not install for Heathrow/Chelsea
PS_0 Should be tied to GND on Thames/Seymour

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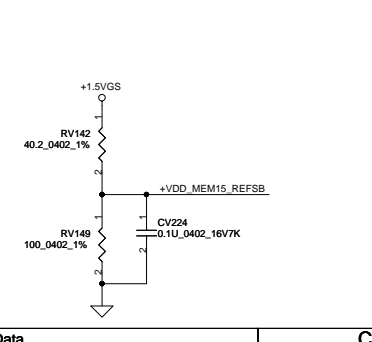
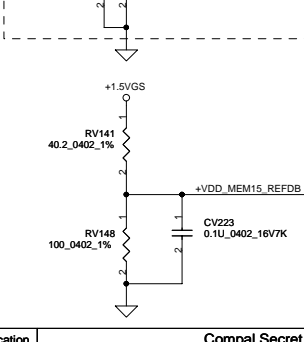
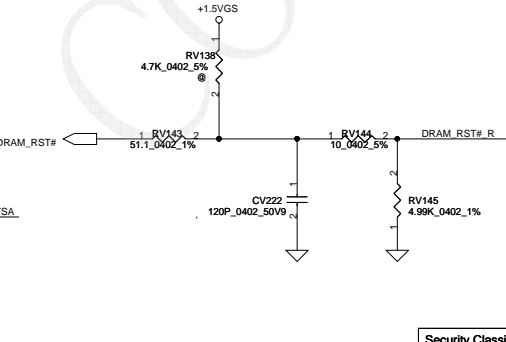
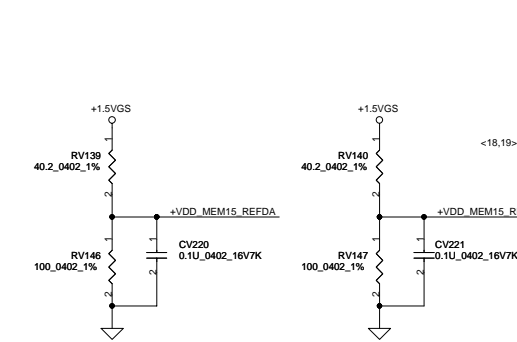
MEMORY INTERFACE A

MEMORY INTERFACE B



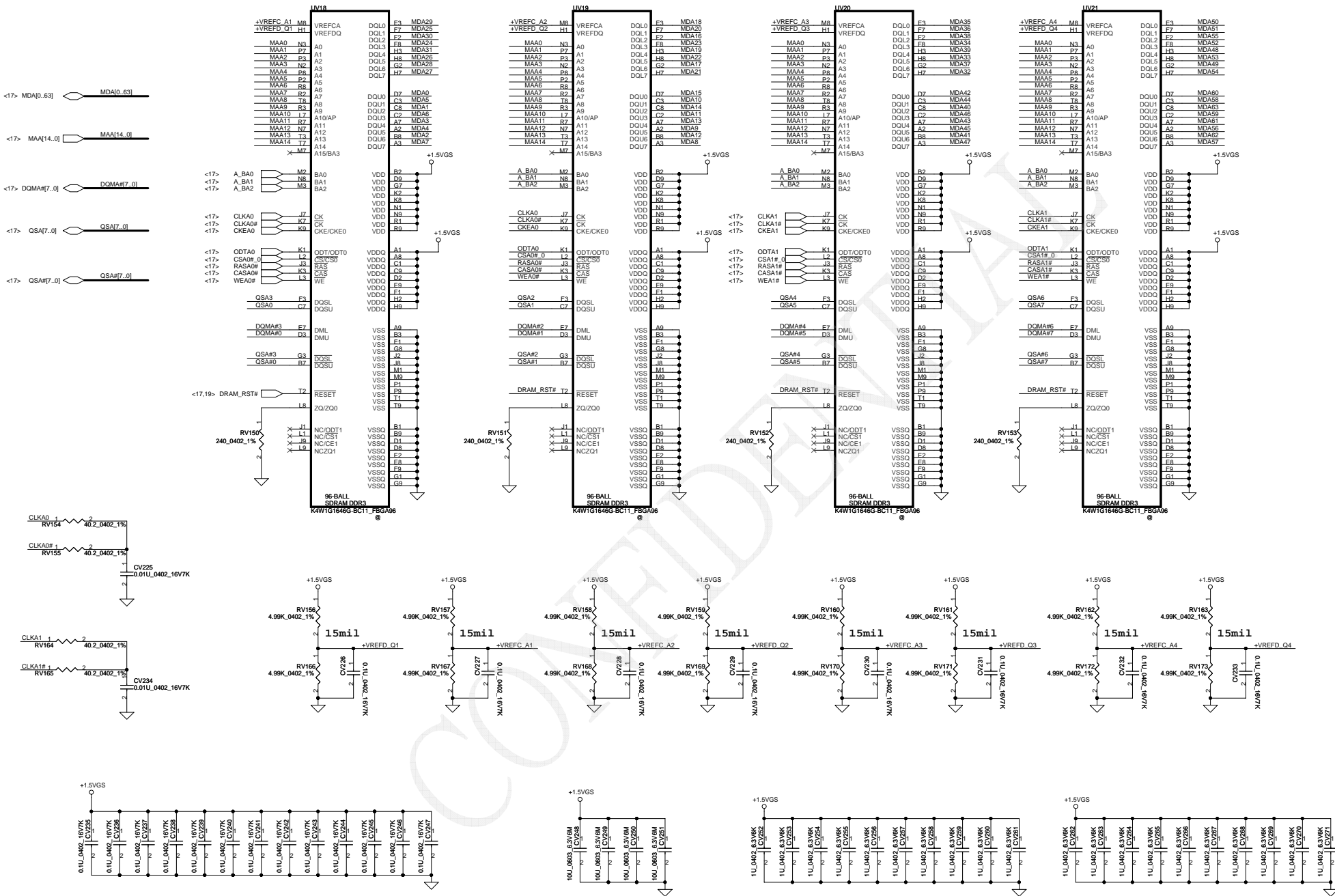
This basic topology should be used for DRAM_RST for DDR3/GDDR5. These Capacitors and Resistor values are an example only. The Series R and || cap values will depend on the DRAM load and will have to be calculated for different Memory_DRAM Load and board to pass Reset Signal Spec. Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except Rser2

route 50ohms single-ended/100ohms diff and keep short
Debug only, for clock observation, if not needed, DNI
5mil 5mil



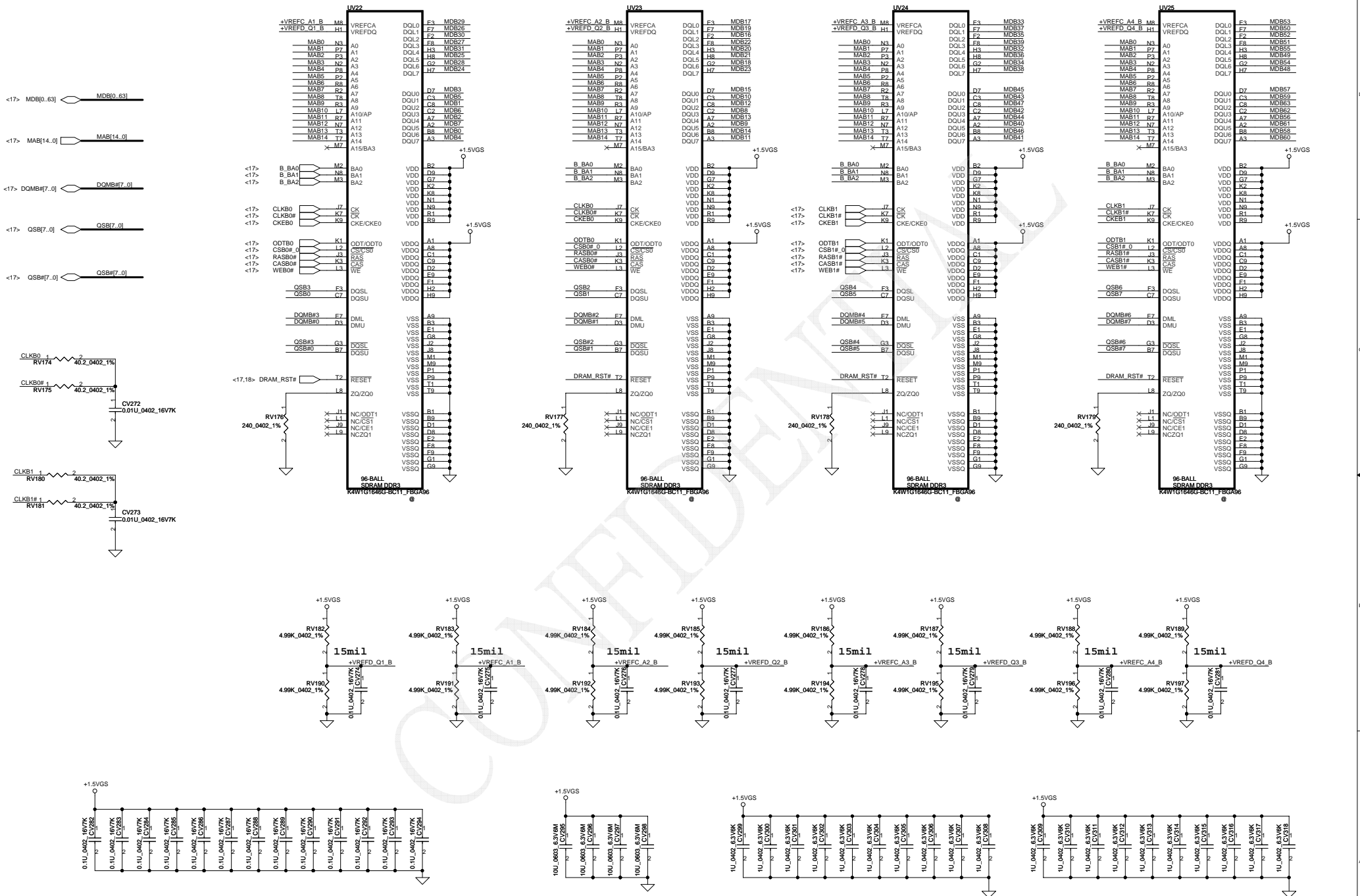
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CHANNEL A: 512MB/1024MB DDR3



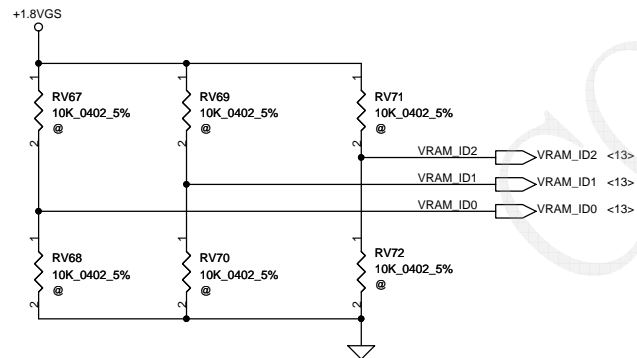
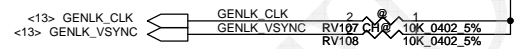
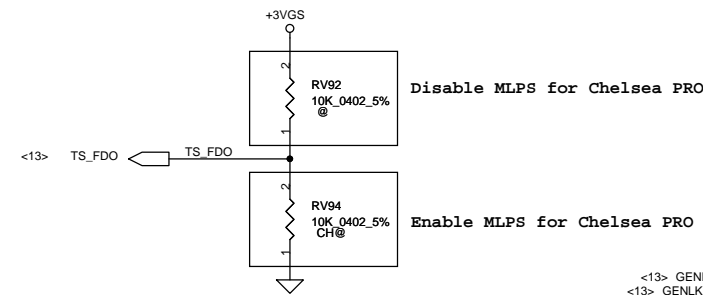
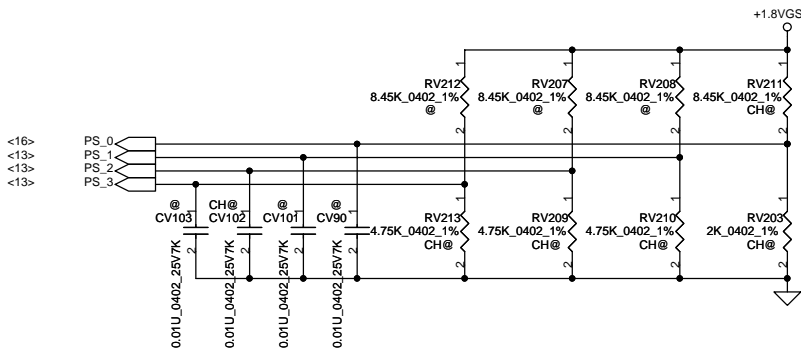
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CHANNEL B: 512MB/1024MB DDR3



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	Bits[5:4]	Bits[3:1]	Capacitor	R_pu	R_pd
PS_0	1 1	0 0 1	NC	8.45k	2k
PS_1	1 1	0 0 0	NC	NC	4.75k
PS_2	0 0	0 0 0	680 nF	NC	4.75k
PS_3	1 1	0 0 0	NC	NC	4.75k



VRAM Straps

	Vendor	VRAM_ID0	VRAM_ID1	VRAM_ID2
64MX16 (1G)	H5TQ1G63DFR-11C Hynix 1GB SA000041S20	RV68	RV70	RV72
*64MX16 (1G)	K4W1G1646G-BC11 Samsung 1GB SA00004GS00	RV67	RV70	RV72
128M16 (2G)	H5TQ2G63DFR-11C Hynix 2GB SA00003YO00	RV68	RV69	RV72
*128M16 (2G)	K4W2G1646C-BC11 Samsung 2GB SA000047Q00	RV67	RV69	RV72

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

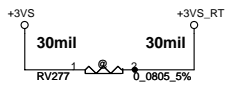
MLPS Bit	STRAPS	Conventional Pin Strap Equivalent	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
PS_0[3:1]	ROMIDCFG(2:0)	GPIO[13:11]	Memory aperture size select 256MB: 0 0 1	0 0 1
PS_0[4]	N/A	GENLK_VSYNC	Must be 1 at rest. (Chelsea PRO)	1
PS_1[1]	STRAP_BIF_GEN3_EN_A	GPIO2	PCIe Gen3 capability 0: 2.5GT/s 1: 5GT/s	0
PS_1[2]	STRAP_BIF_CLK_PM_EN	GPIO8	PCIe clock power management capability.	0
PS_1[3]	N/A	GENLK_CLK	Must be 0 at rest. (Chelsea PRO)	0
PS_1[4]	TX_PWRS_ENB	GPIO0	PCIe full TX output swing 0: Half swing 1: Full swing	1
PS_1[5]	TX_DEEMPH_EN	GPIO1	PCIe transmitter de-emphasis enable 0: Disable 1: Enable	1
PS_2[1] PS_2[2]	N/A	N/A	Reserved	N/A
PS_2[3]	BIOS_ROM_EN	GPIO_22_ROMCSB	Enable external BIOS ROM 0: Disable 1: Enable	0
PS_2[4]	VGA DIS	GPIO9	VGA disable 0: Enable 1: Disable	0
PS_2[5] PS_3[3:1]	N/A	N/A	Reserved	N/A
PS_0[5] PS_3[4] PS_3[5]	AUD_PORT_CONN_PINSTRAP[0] AUD_PORT_CONN_PINSTRAP[1] AUD_PORT_CONN_PINSTRAP[2]	N/A	Audio-capable display outputs 0 0 0 All endpoints are usable 1 1 1 No usable endpoints.	1 1 1
AUD[1] AUD[0]	HSYNC VSYNC		AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	0 0

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOs ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET

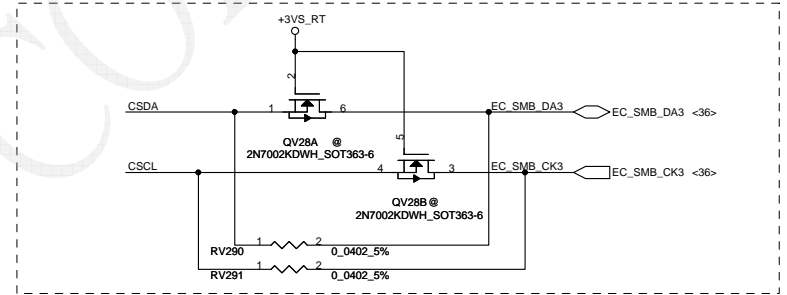
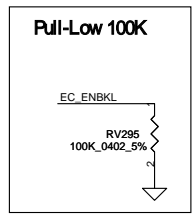
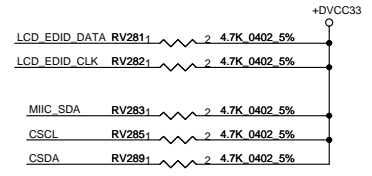
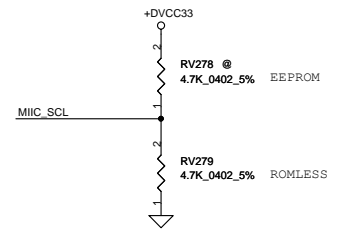
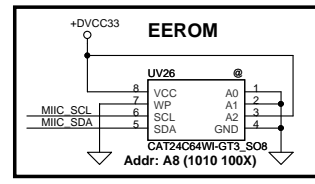
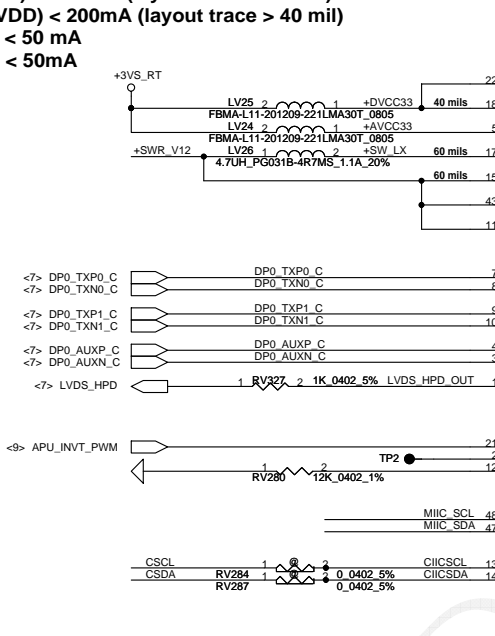
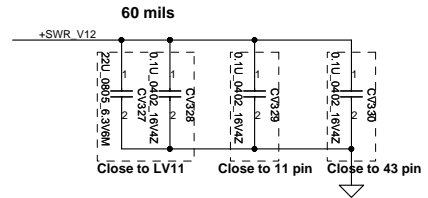
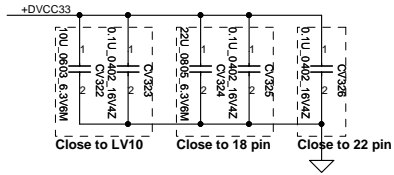
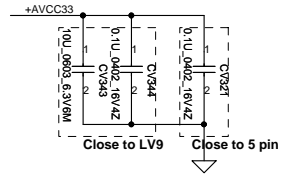
GPIO21 H2SYNC GENERICC GPIO2 GPIO8

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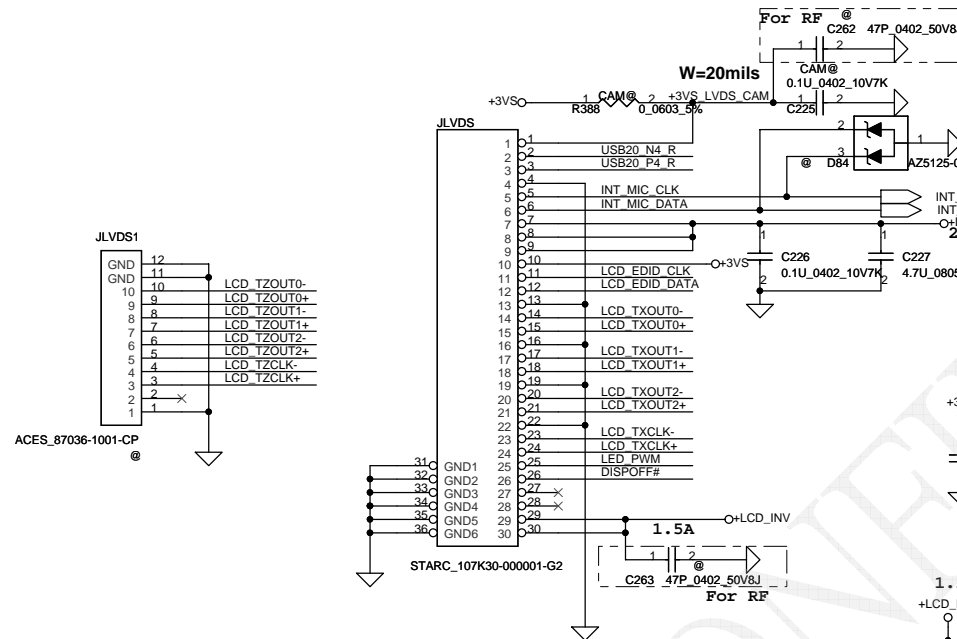
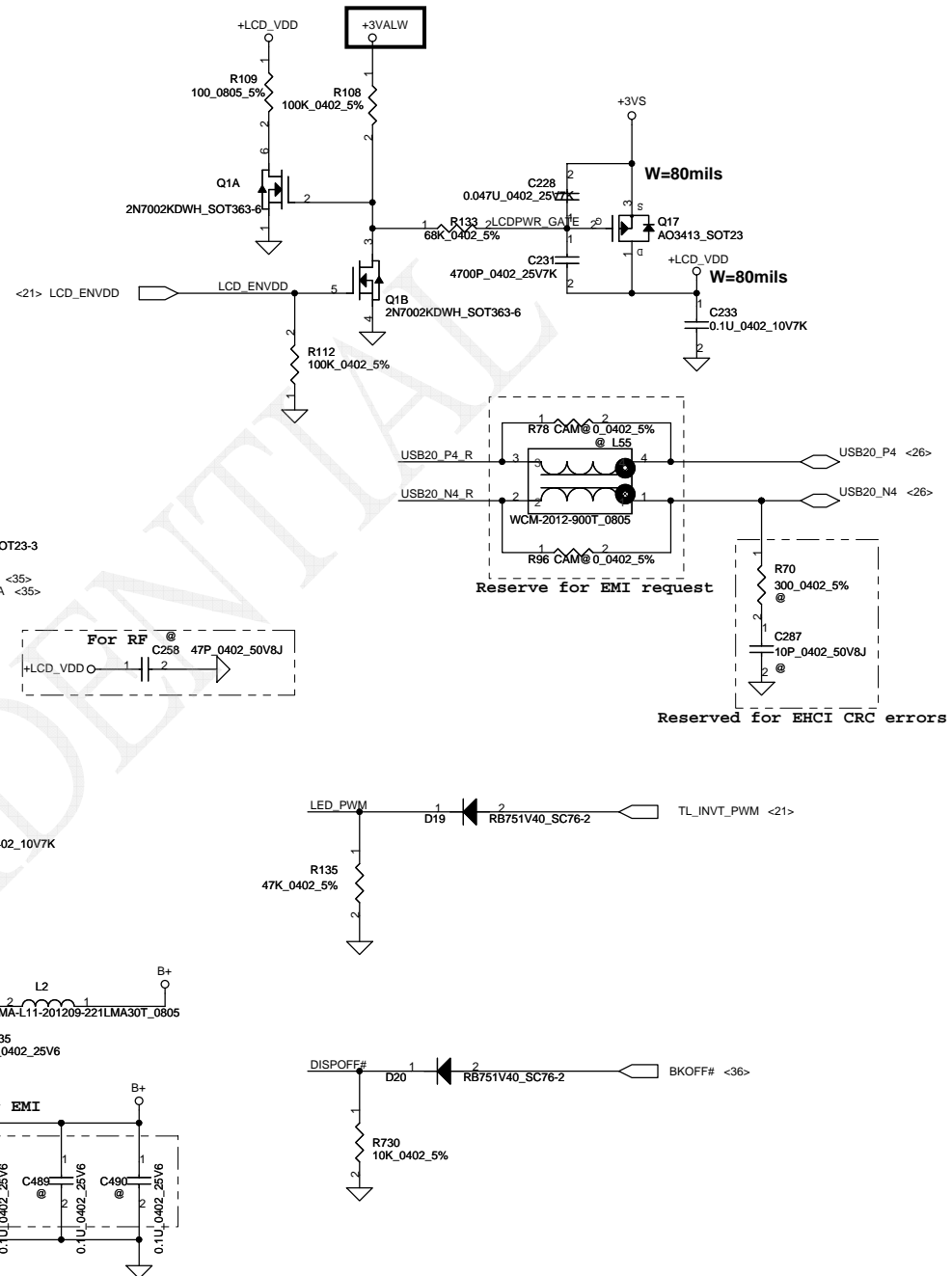
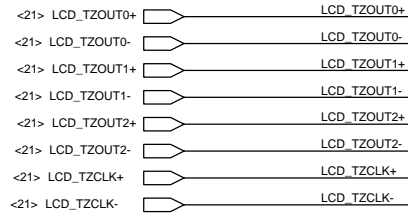
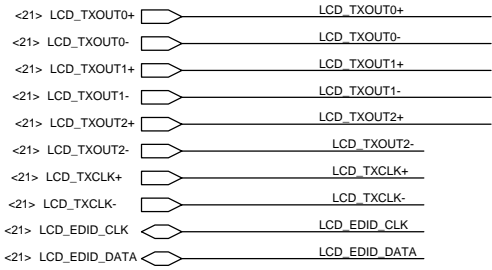


Power Consumption:

- Pin 5 (DPV33) < 20mA
- Pin 11 (DPV12) < 100mA
- Pin 15 (SWR_VCCK) < 100mA (layout trace > 60 mil)
- Pin 17 (SWR_LX) < 600mA (layout trace > 60 mil)
- Pin 18 (SWR_VDD) < 200mA (layout trace > 40 mil)
- Pin 22 (PVCC) < 50 mA
- Pin 43 (VCCK) < 50mA

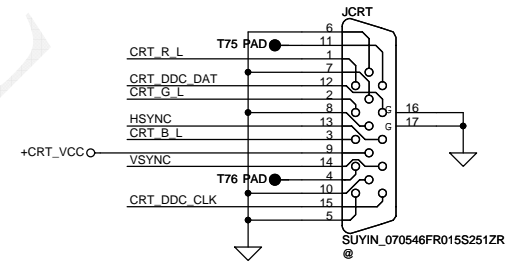
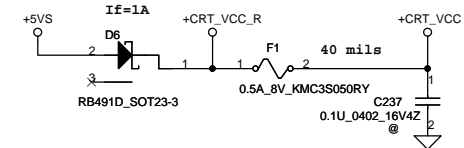


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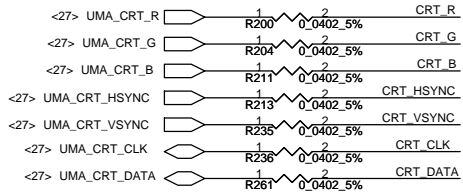


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CRT CONNECTOR

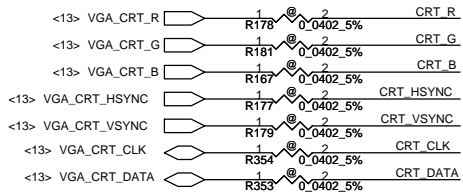


For PowerXpress

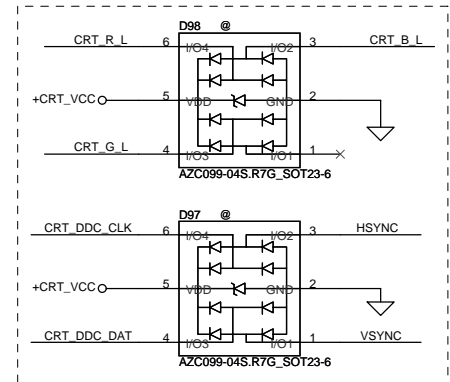
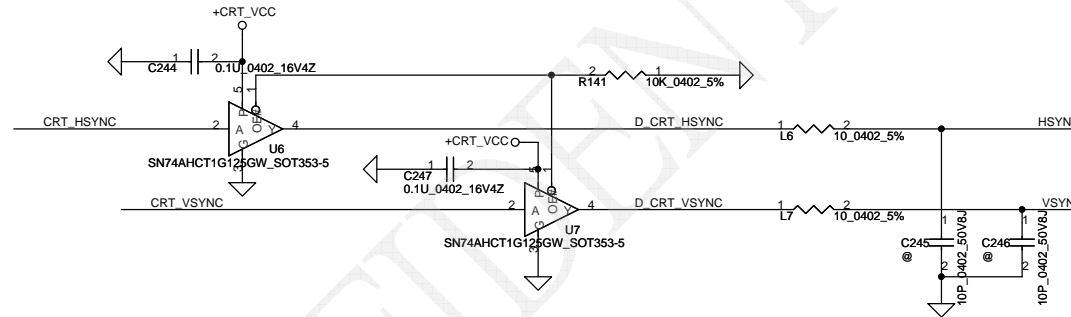
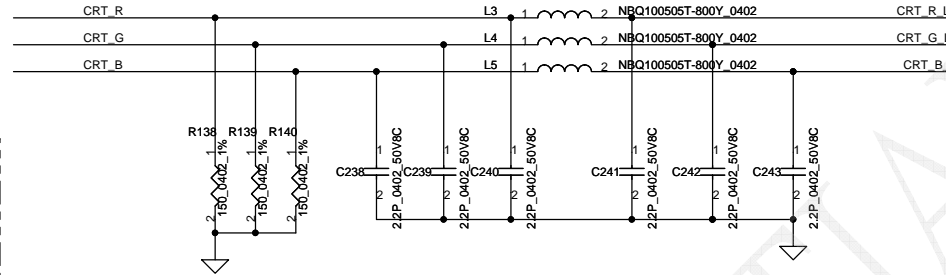


Close to CRT Connector

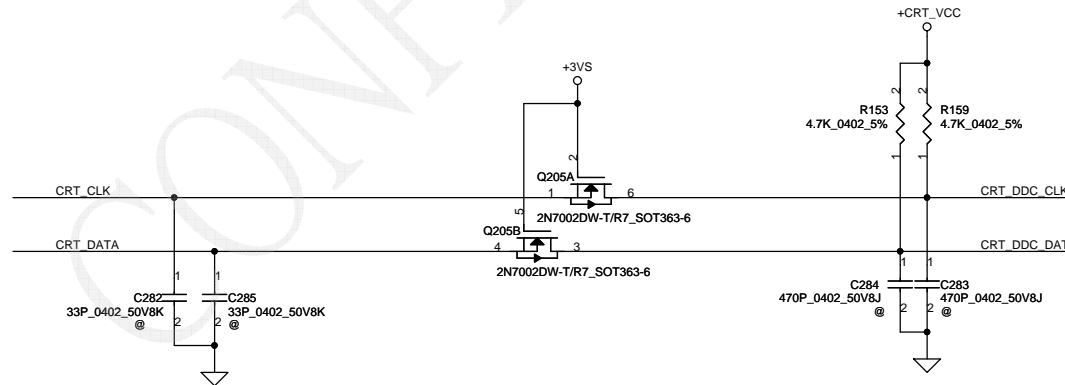
For Debug



Close to CRT Connector



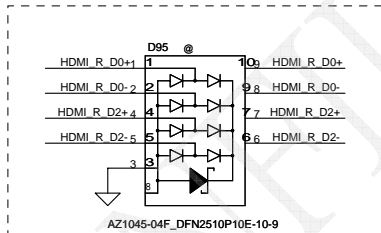
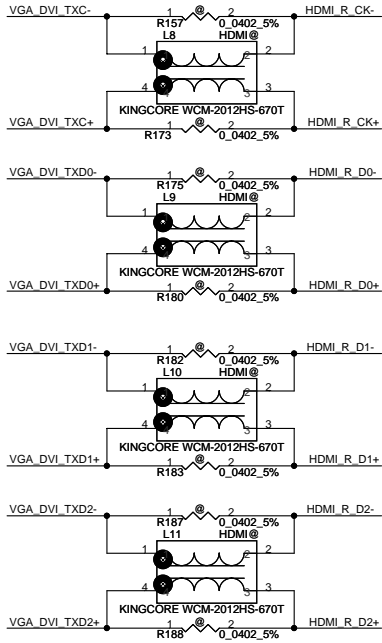
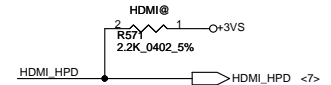
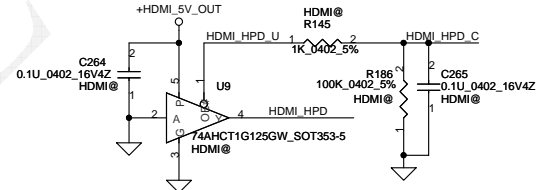
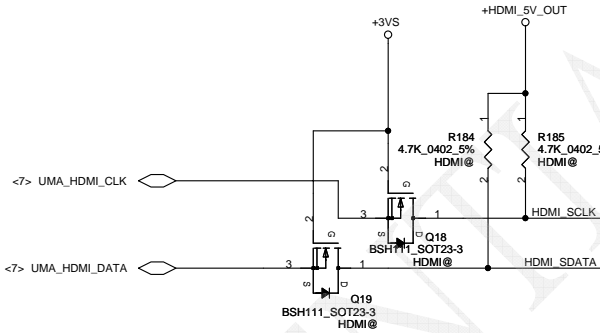
2/9: Add for ESD request



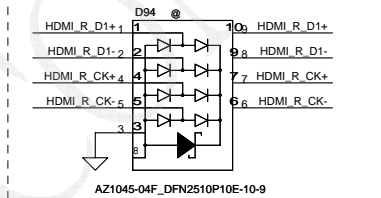
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<7> UMA_HDMI_TXC+	C310	1	2	0.1U_0402_16V7K HDMI@	VGA DVI_TXC+
<7> UMA_HDMI_TXC-	C321	1	2	0.1U_0402_16V7K HDMI@	VGA DVI_TXC-
<7> UMA_HDMI_TX0+	C326	1	2	0.1U_0402_16V7K HDMI@	VGA DVI_TXD0+
<7> UMA_HDMI_TX0-	C313	1	2	0.1U_0402_16V7K HDMI@	VGA DVI_TXD0-
<7> UMA_HDMI_TX1+	C309	1	2	0.1U_0402_16V7K HDMI@	VGA DVI_TXD1+
<7> UMA_HDMI_TX1-	C314	1	2	0.1U_0402_16V7K HDMI@	VGA DVI_TXD1-
<7> UMA_HDMI_TX2+	C318	1	2	0.1U_0402_16V7K HDMI@	VGA DVI_TXD2+
<7> UMA_HDMI_TX2-	C322	1	2	0.1U_0402_16V7K HDMI@	VGA DVI_TXD2-

Change R184 and R185 from 2K to 4.7K for HDMI detect issue on preMP

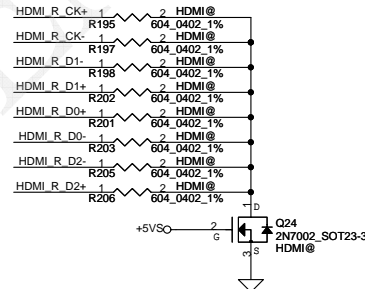


AZ1045-04F_DFN2510P10E-10-9



AZ1045-04F_DFN2510P10E-10-9

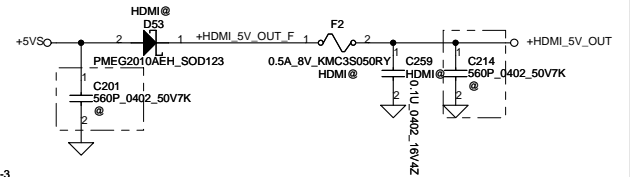
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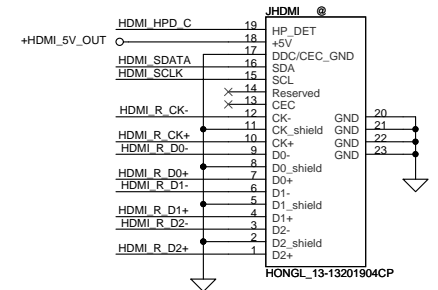
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2/9: Add for ESD request

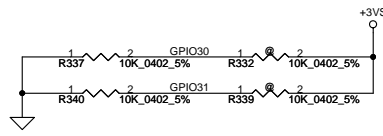
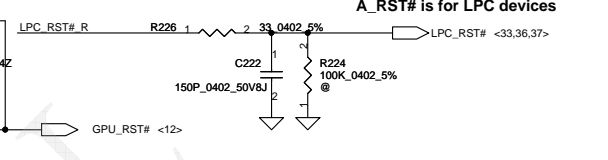
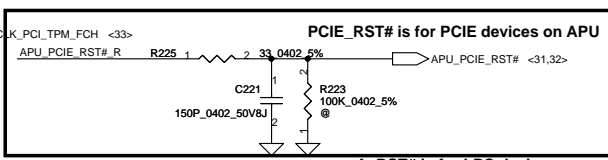
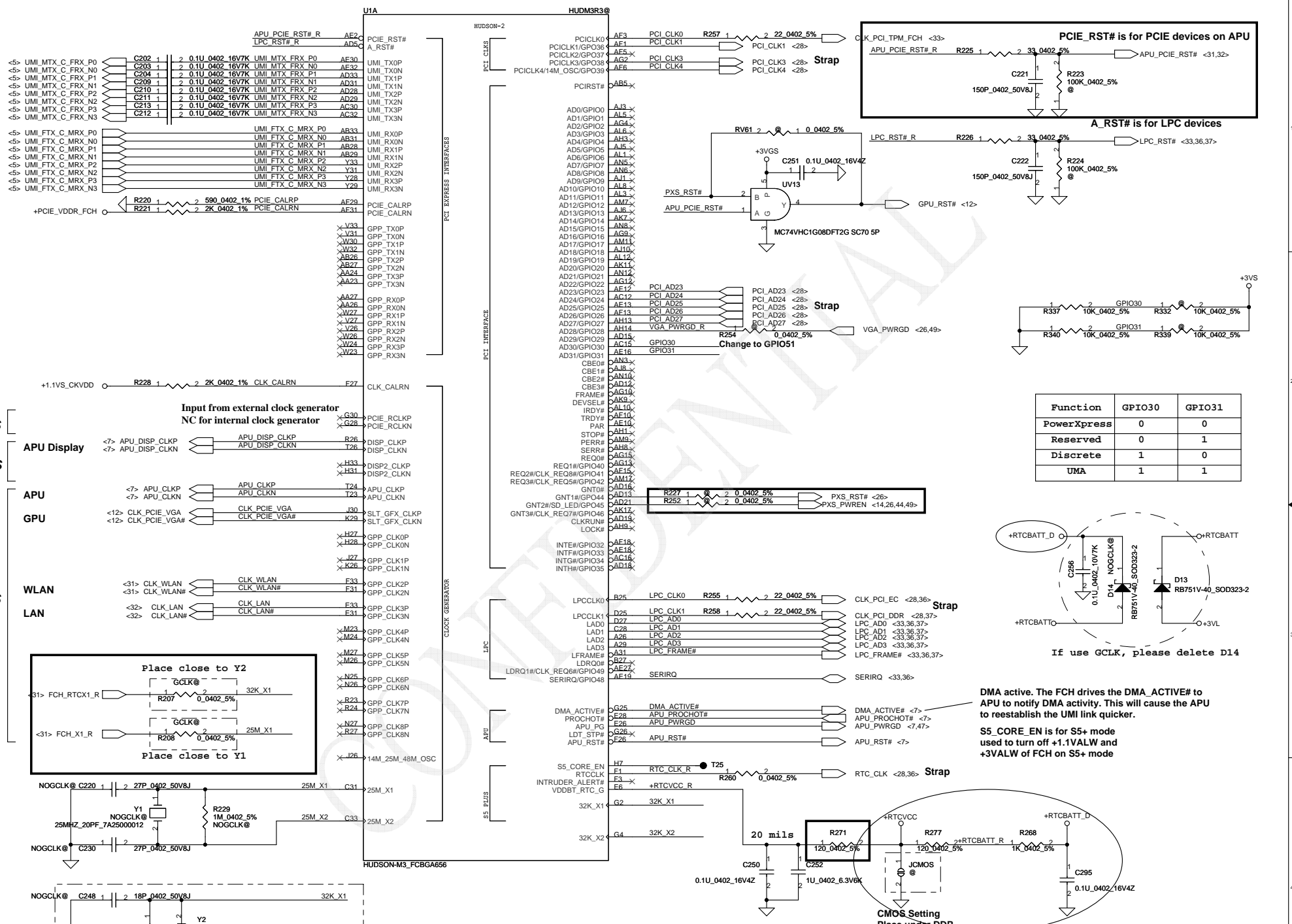
Add C201 and C214 for EMI request on PVT



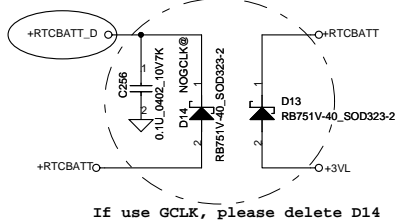
HDMI Connector



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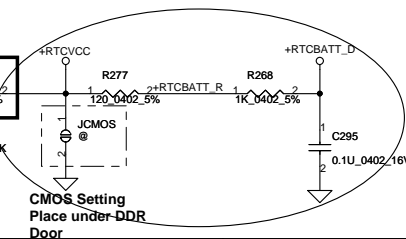
Function	GPIO30	GPIO31
PowerXpress	0	0
Reserved	0	1
Discrete	1	0
UMA	1	1



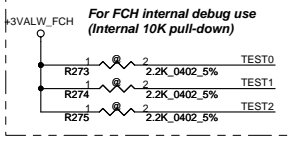
If use GCLK, please delete D14

DMA active. The FCH drives the DMA_ACTIVE# to APU to notify DMA activity. This will cause the APU to reestablish the UMI link quicker.

S5_CORE_EN is for S5+ mode used to turn off +1.1VALW and +3VALW of FCH on S5+ mode

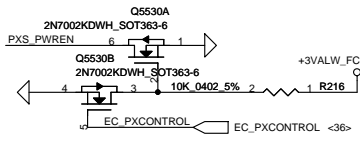
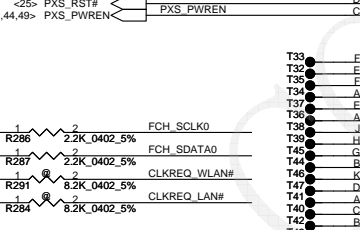
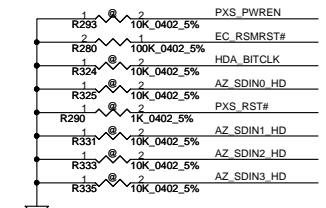
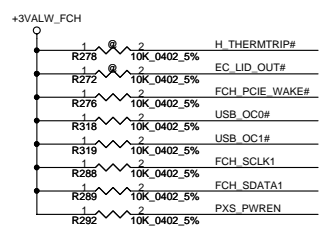


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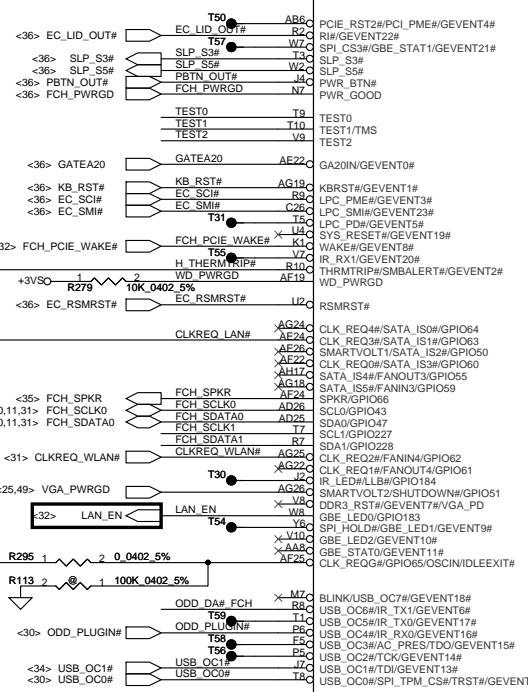


VGA_PD: Support CRT power saving
 L: MLDAC power on
 H: MLDAC power off

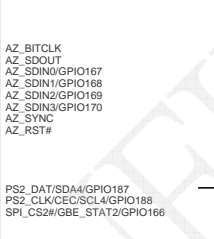
USB_OC1# is for left USB3.0 ports
 USB_OC0# is for right USB2.0 ports



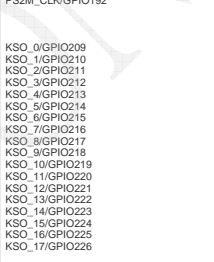
PCIE_RST2# is for PCIE devices on FCH UID



HUDSON-2

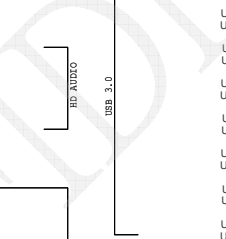
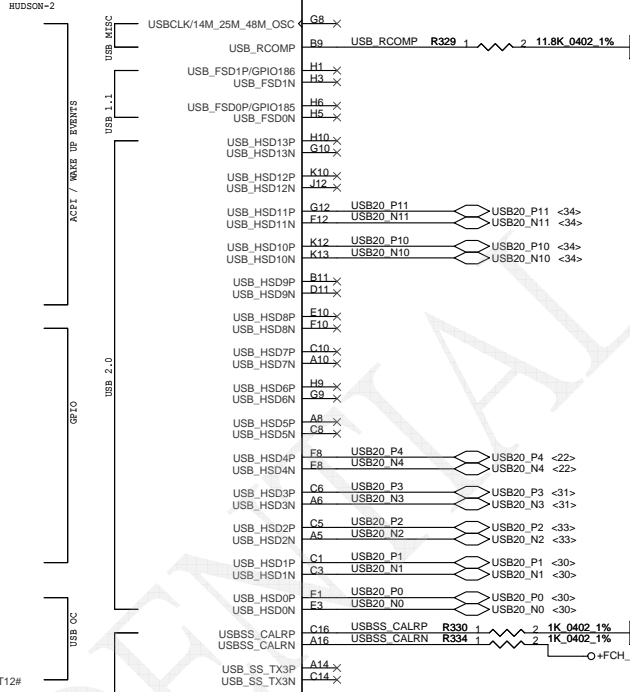


EMBEDDED CTRL

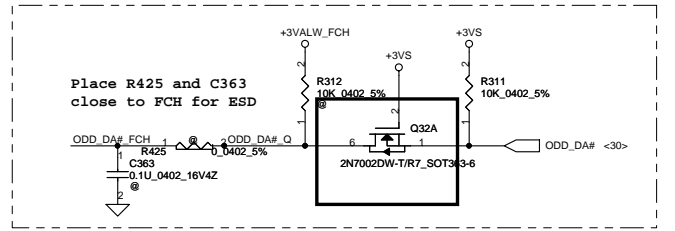
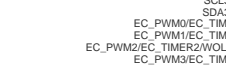


HUDSON-M3_FCBGA656

HUDM3R3@

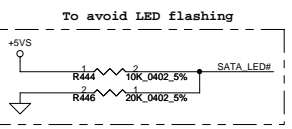
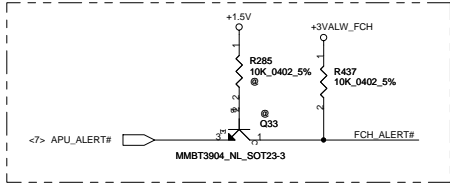


SM Bus 2-->S5 PWR domain

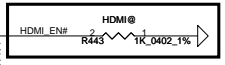
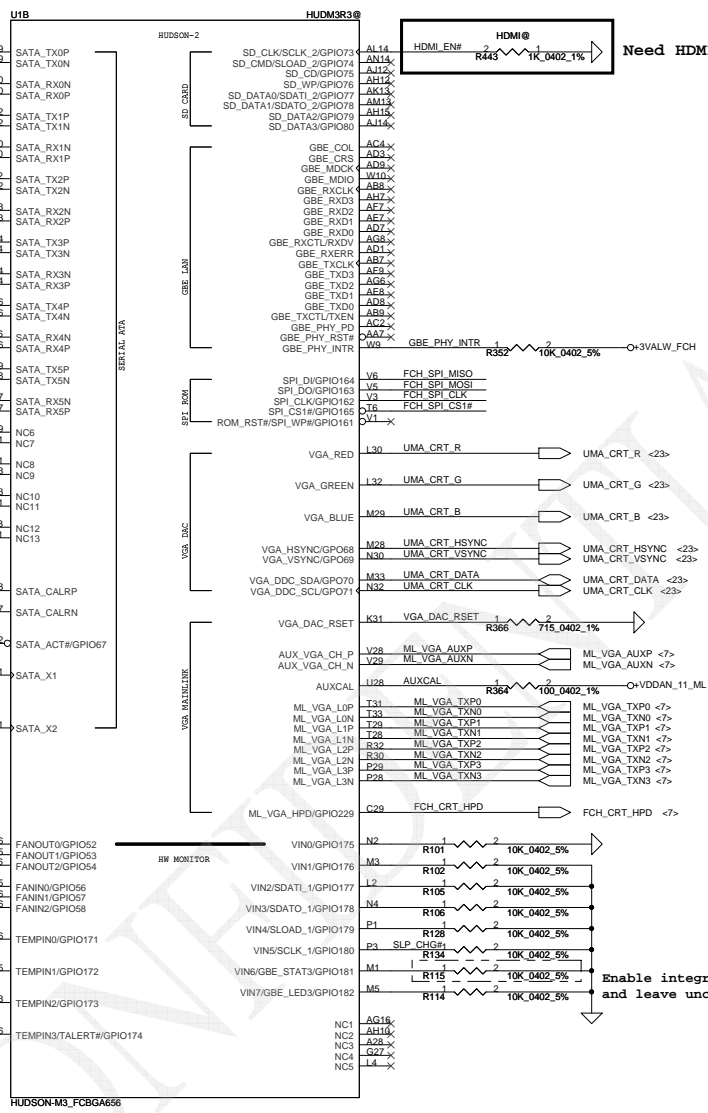
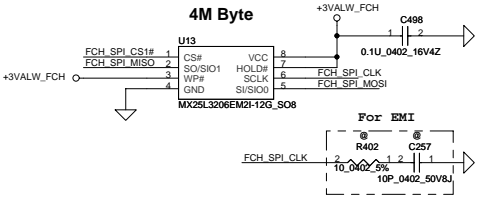
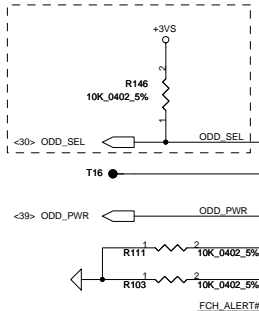


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- HDD
 - <30> SATA_FTX_DRX_P0
 - <30> SATA_FTX_DRX_N0
 - <30> SATA_FRX_C_DTX_N0
 - <30> SATA_FRX_C_DTX_P0
 - <30> SATA_FTX_DRX_P1
 - <30> SATA_FTX_DRX_N1
 - <30> SATA_FRX_C_DTX_N1
 - <30> SATA_FRX_C_DTX_P1
 - <30> SATA_FTX_DRX_P2
 - <30> SATA_FTX_DRX_N2
 - <30> SATA_FRX_C_DTX_N2
 - <30> SATA_FRX_C_DTX_P2
- 14" ODD
- 15"/17" ODD

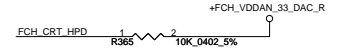
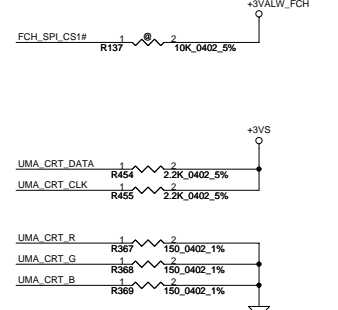


ODD_SEL	SATA port	SKU
High	Port 1	14"
Low	Port 2	15"/17"

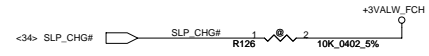


HDMI_EN#	H	L
SKU	Non-HDMI SKU	HDMI SKU

If an SPI ROM is shared between FCH and the Embedded Controller, a 10-k pull-up resistor to +3.3V_S5 is installed

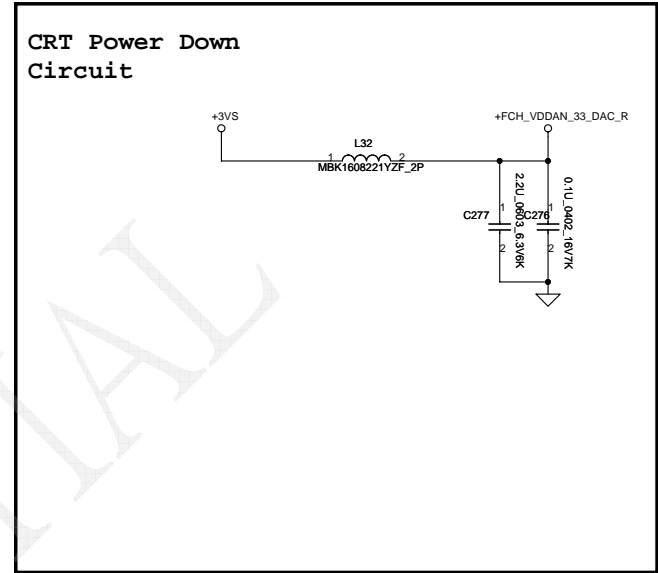
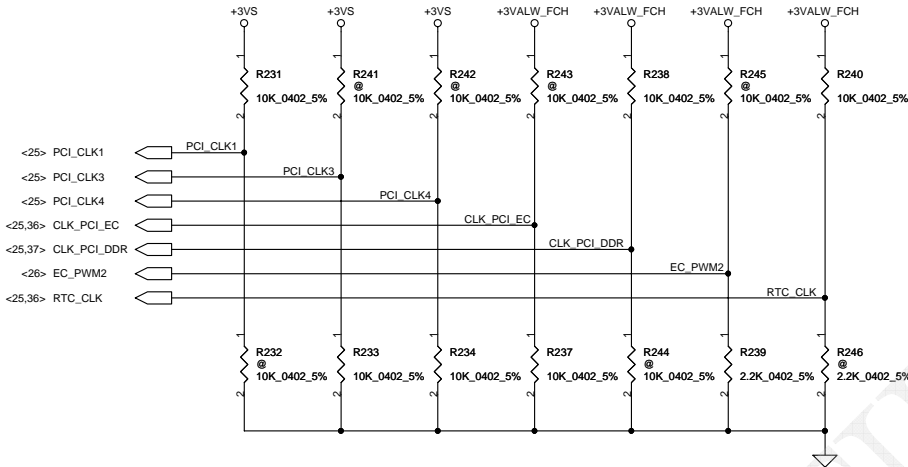


Enable integrated pull-down/up and leave unconnected



STRAP PINS

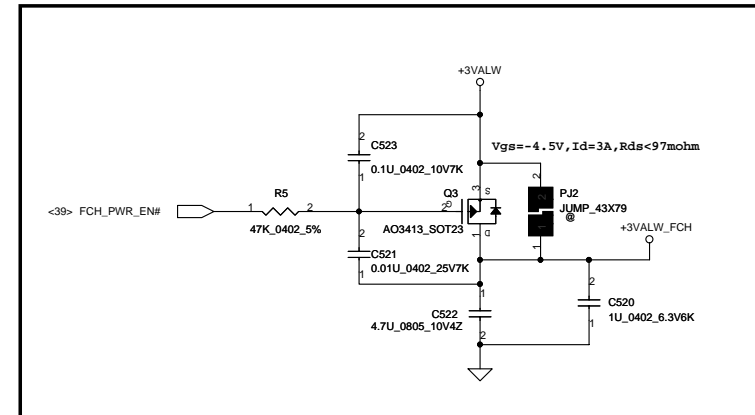
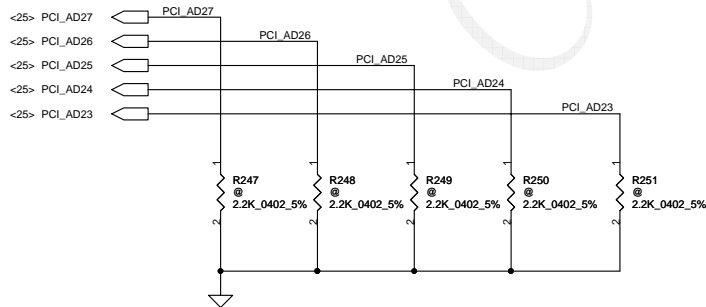
	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	ALLOW PCIE GEN2 DEFAULT	ENABLE DEBUG STRAP	NON_FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM (INTERNAL 10K PULL-UP)	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	FORCE PCIE GEN1	DISABLE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLE	SPI ROM DEFAULT	S5 PLUS MODE ENABLED



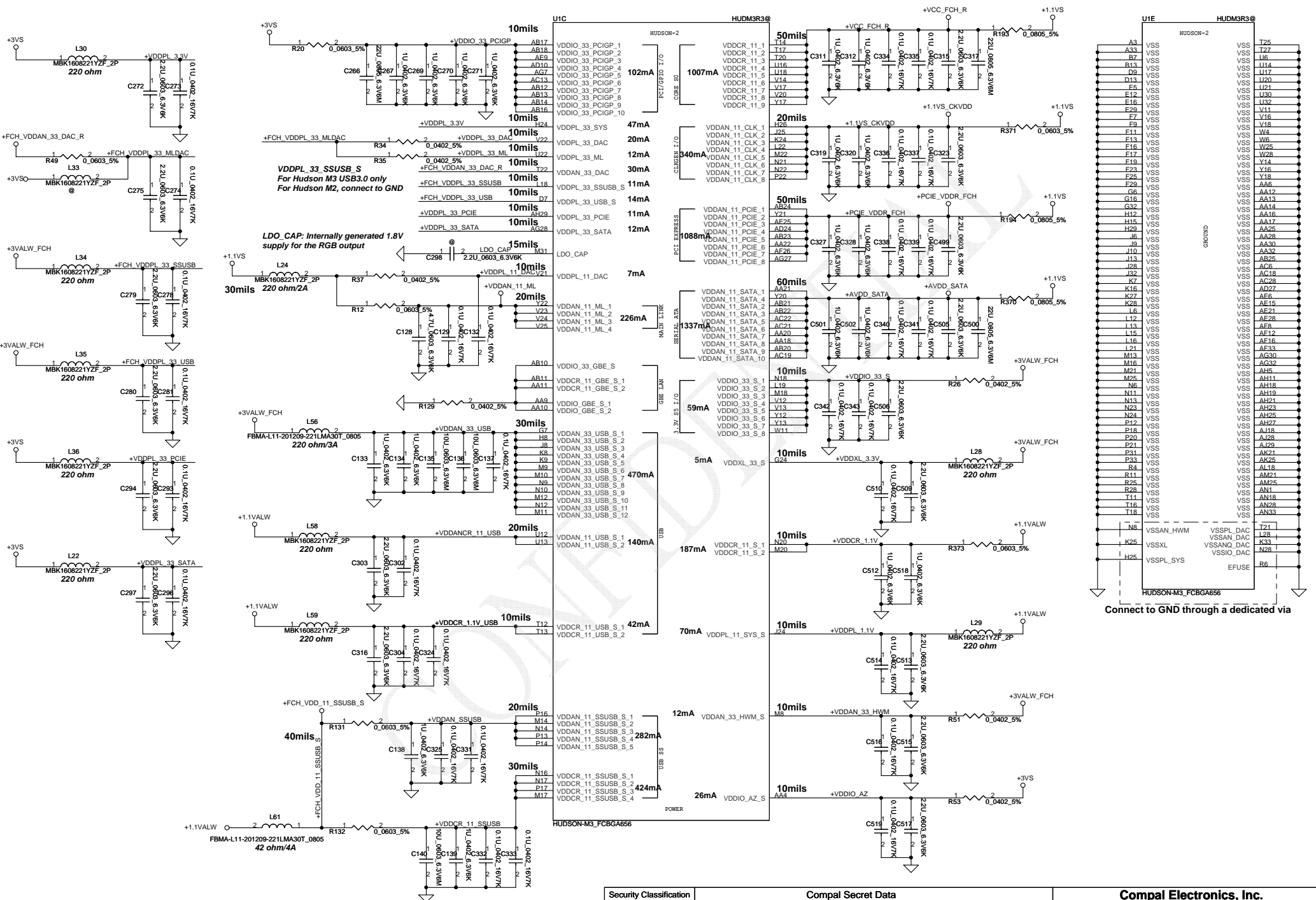
DEBUG STRAPS

FCH HAS 15K INTERNAL PU-UP FOR PCI_AD[27:23]

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT



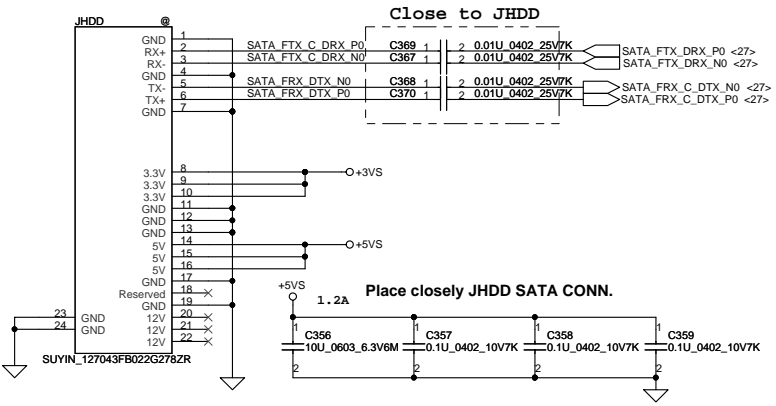
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Revision	1.0	Document Number	4019IT	Rev	A
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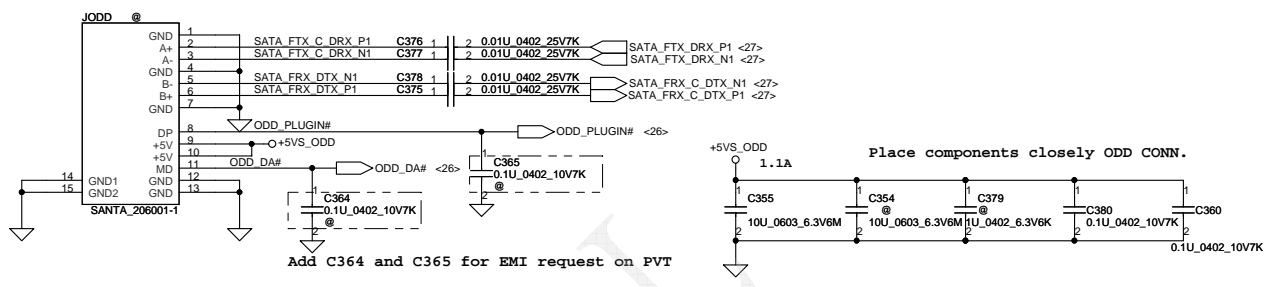
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Compal Electronics, Inc.	
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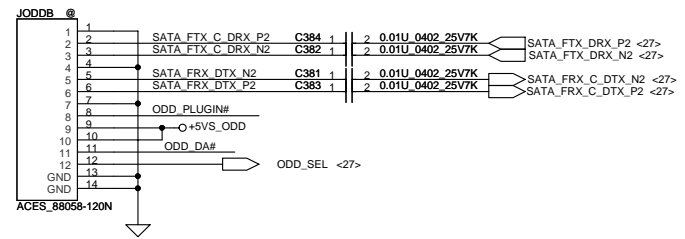
SATA HDD Conn.



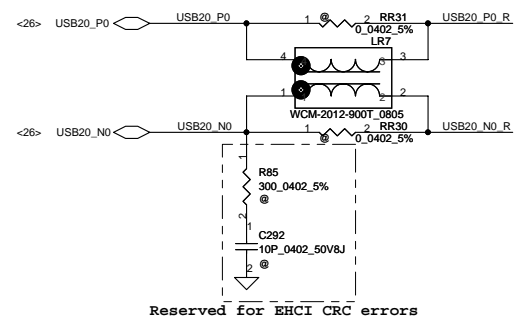
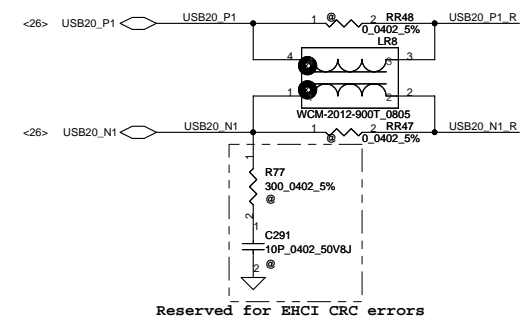
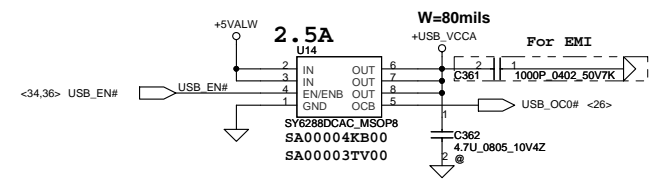
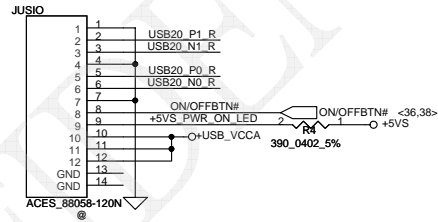
SATA ODD Conn



SATA ODD Conn (for 15"/17")

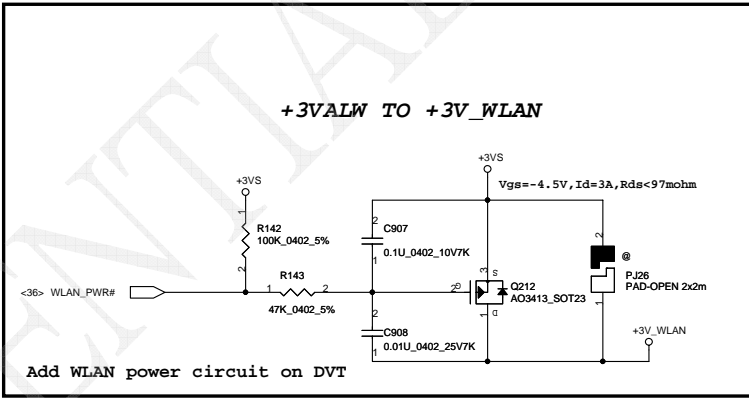
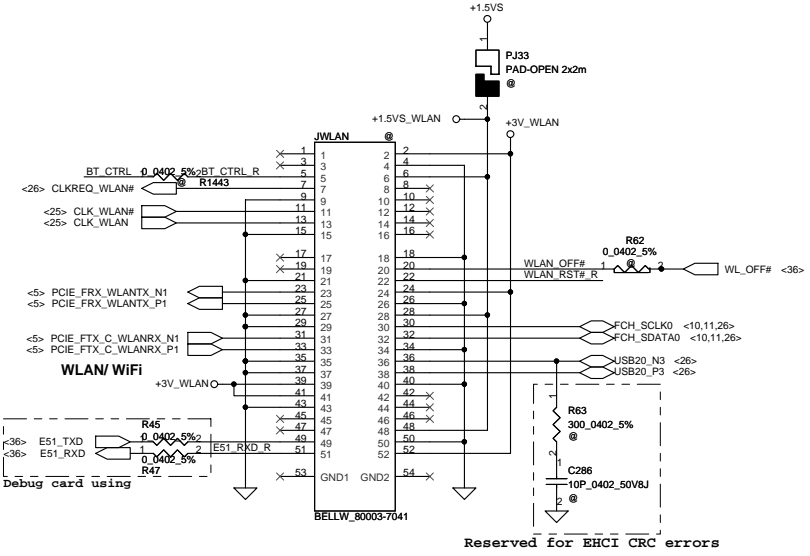
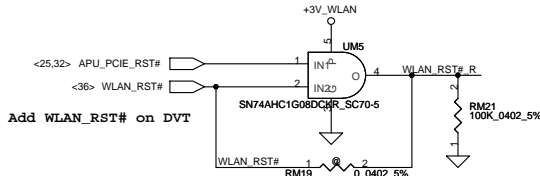
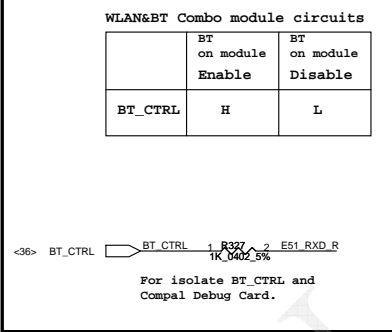
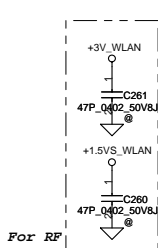
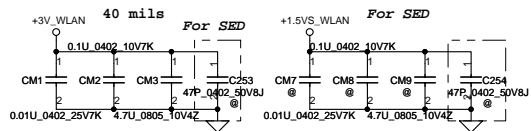


Power Button & RUSB connector

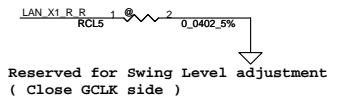
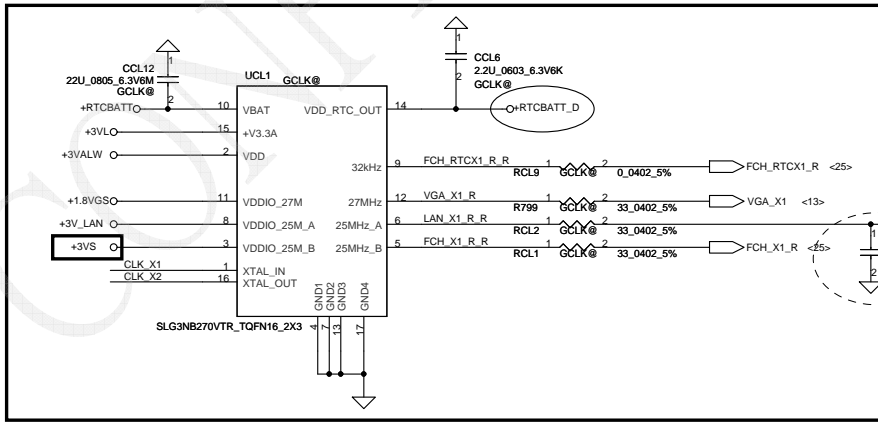
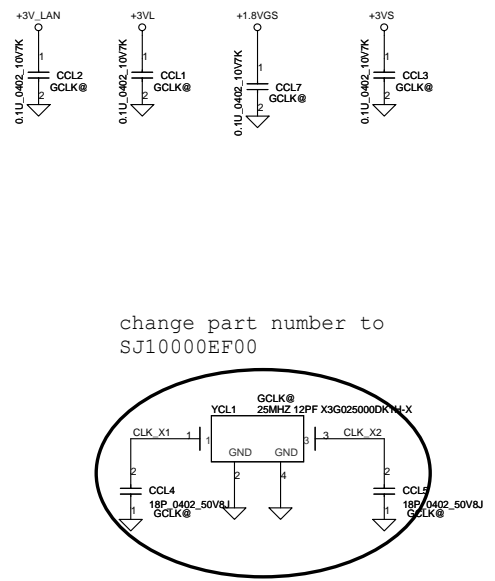


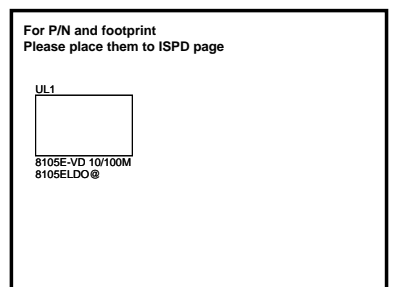
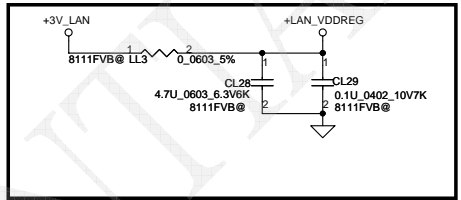
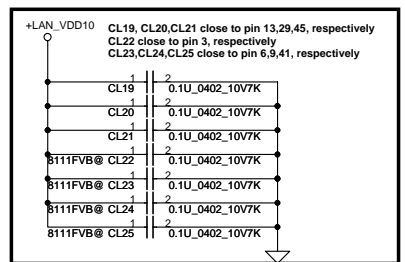
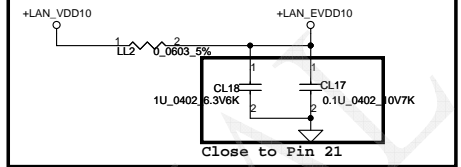
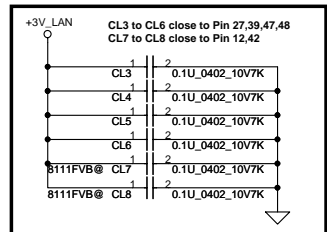
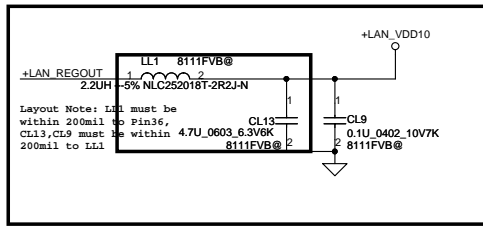
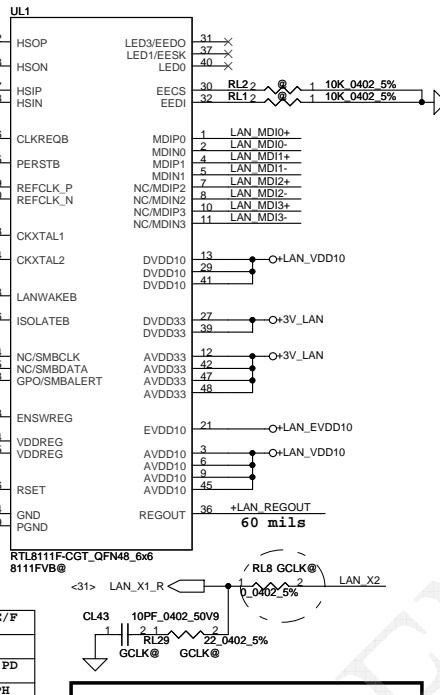
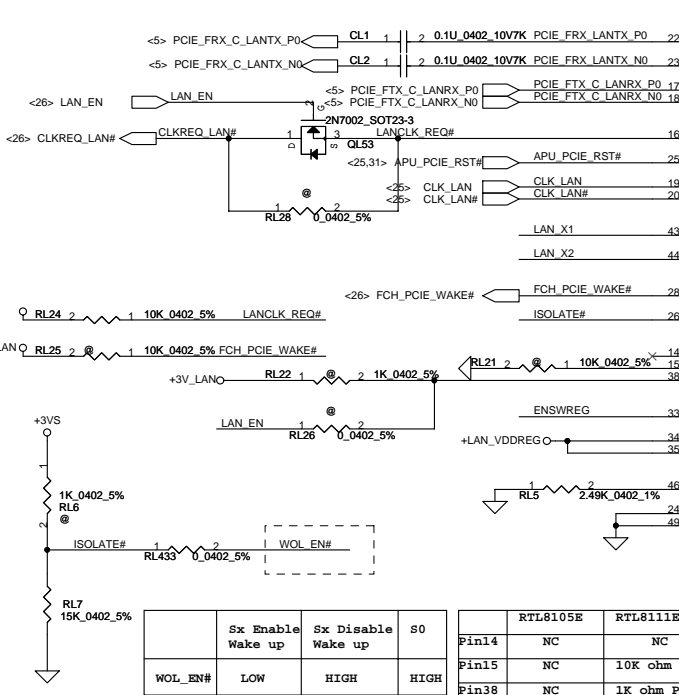
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Slot 1 Half PCIe Mini Card-WLAN



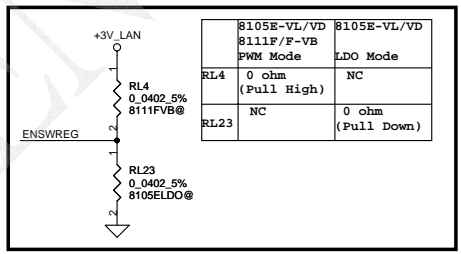
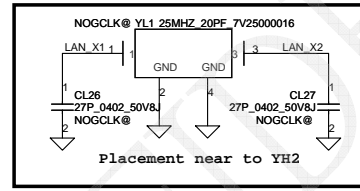
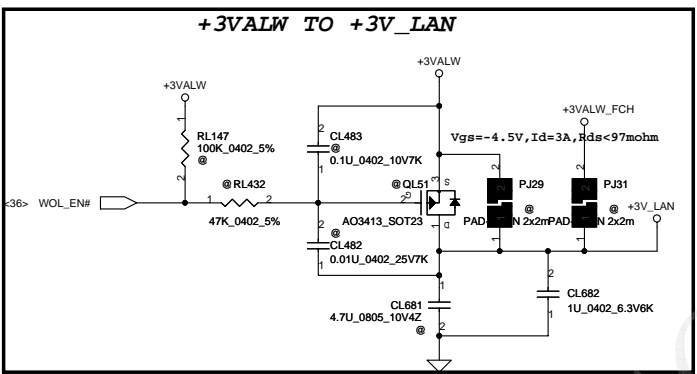
Change to GCLK to SLG3NB270V
 SA00005DP00 for 27MHz
 for VGA





Sx Enable	Sx Disable	S0
Wake up	Wake up	
LOW	HIGH	HIGH

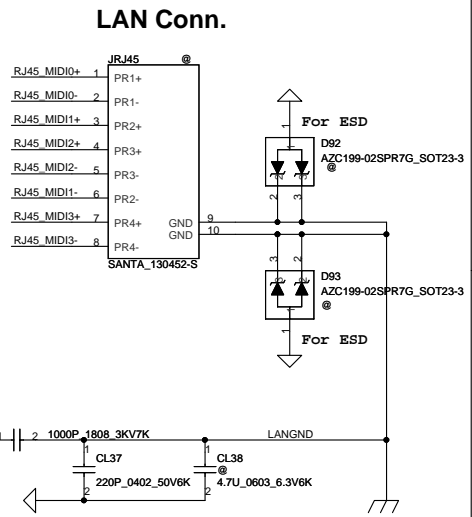
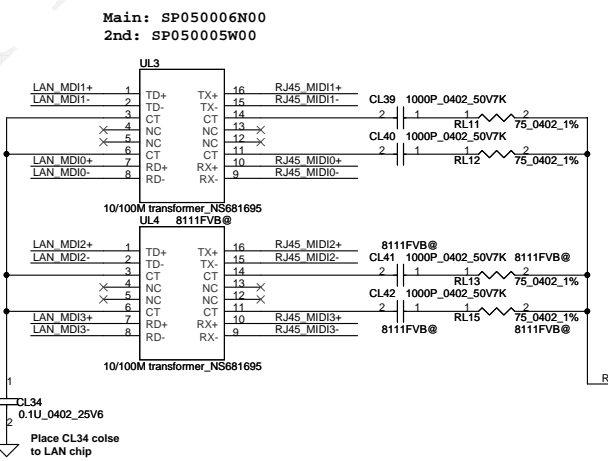
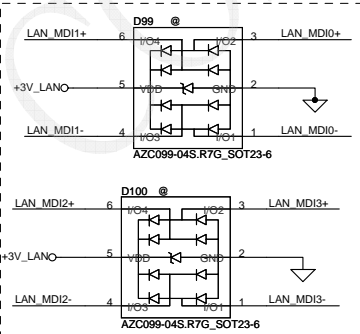
Pin14	NC	NC
Pin15	10K ohm PD	
Pin38	NC	1K ohm PH



+3V_LAN rising time (10%-90%) need > 1ms and < 100ms.

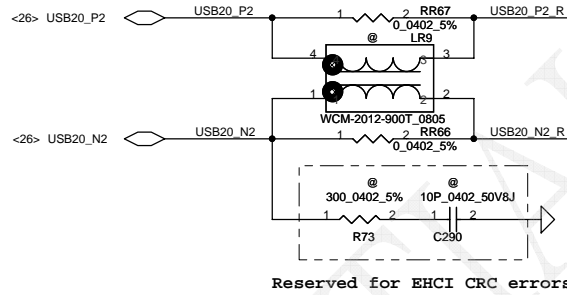
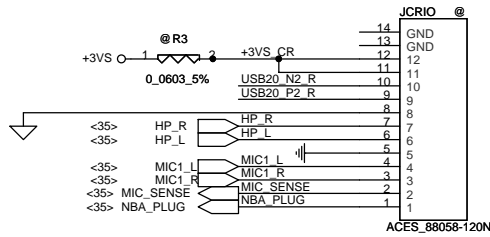
LAN	WOL	LAN_EN S0	LAN_EN Sx	ISOLATEB S0	ISOLATEB Sx
0	0	0	0	1	1
0	1	0	0	1	1
1	0	1	1	1	1
1	1	1	1	1	0*

* S3: after SUSP# assert low over 100ms
S4/S5: after SYSON assert low over 100ms

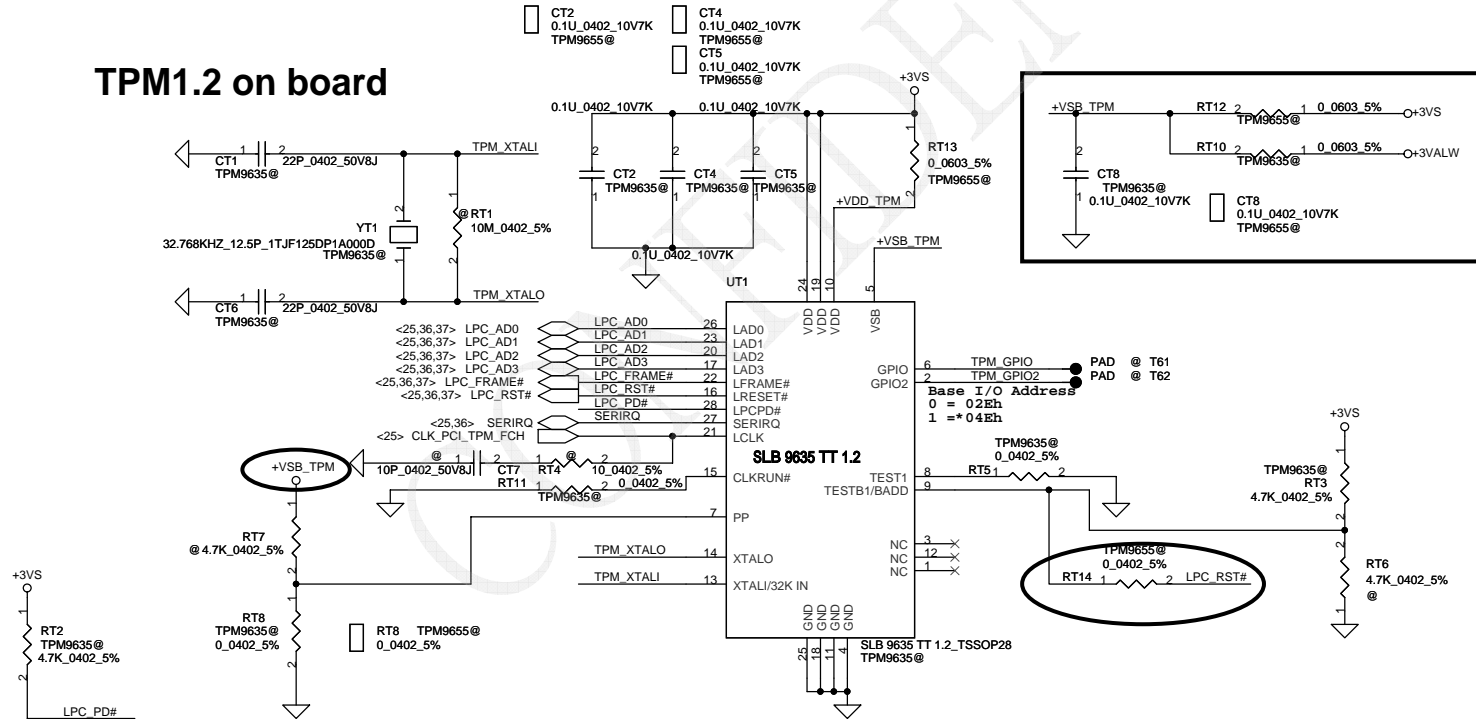


2/9: Add for ESD request

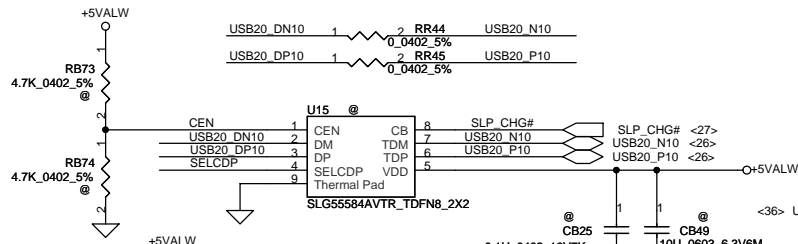
CardReader Conn.



TPM1.2 on board



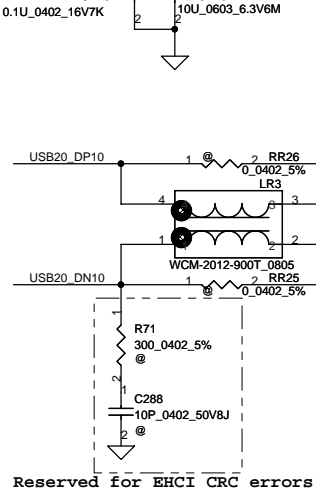
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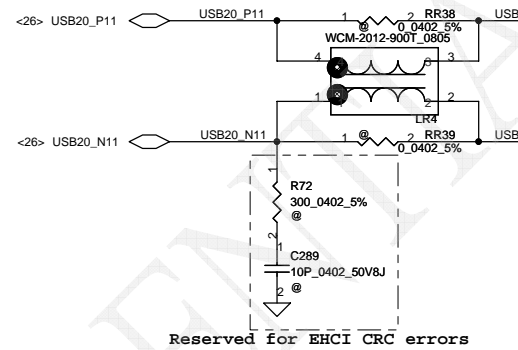
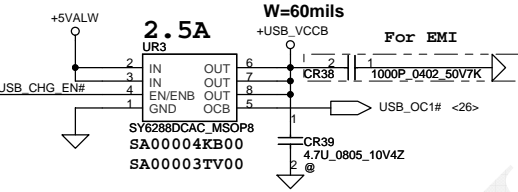
Pull-up for SLGC5584V

Pull-down for SLGC5584V

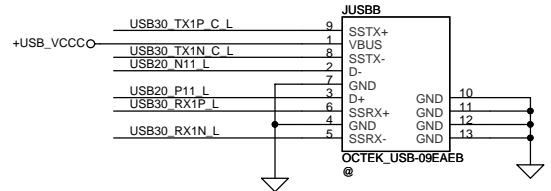
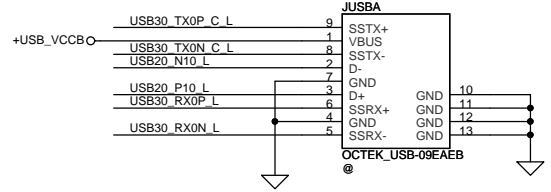
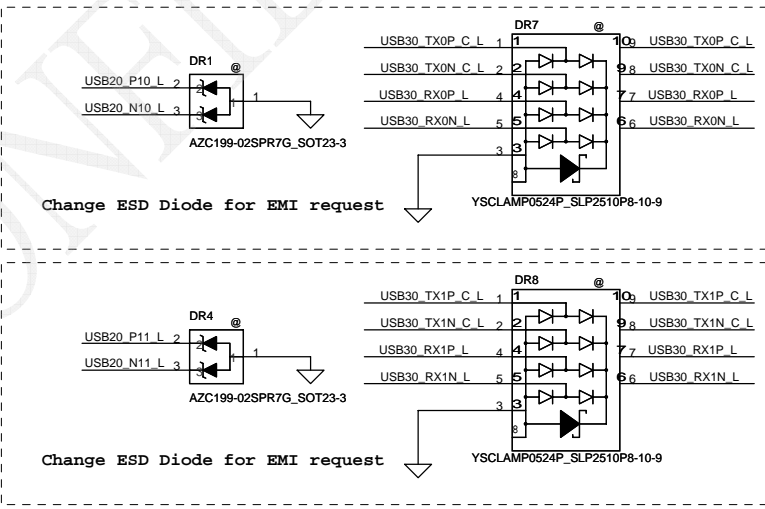
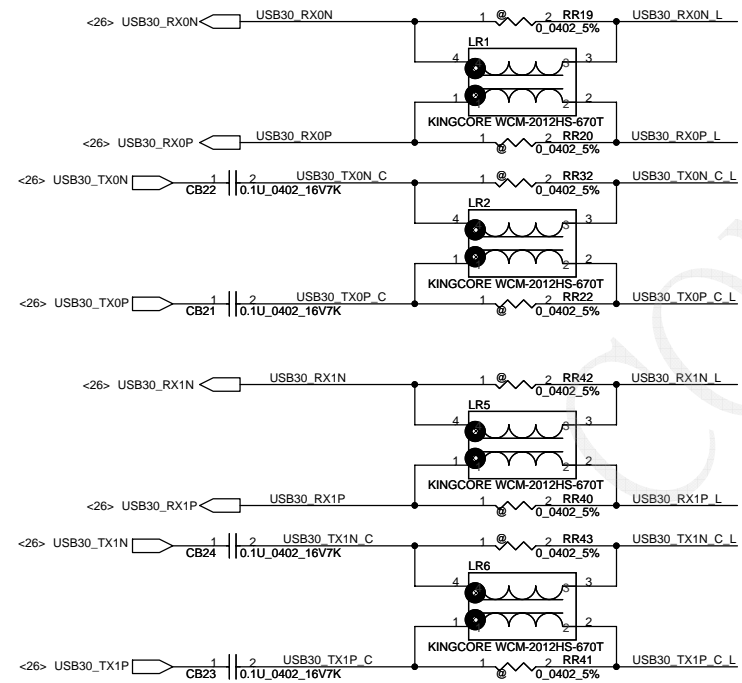
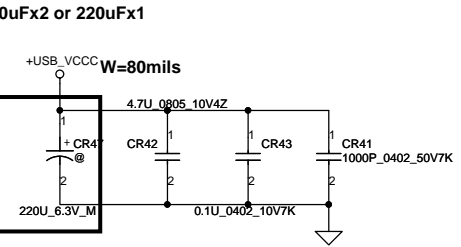
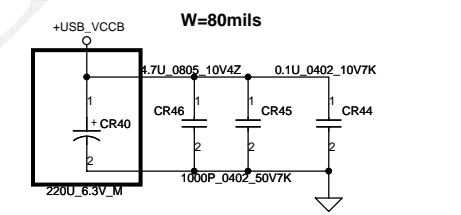
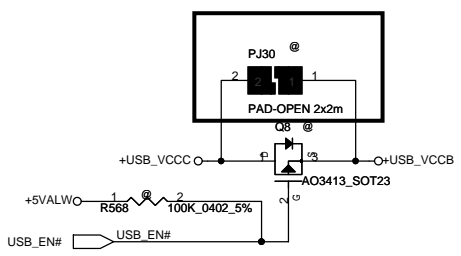
SLP_CHG#	SELCDP	Function
0	X	DCP autodetect with mouse/keyboard wakeup
1	0	S0 charging with SDP only
1	1	S0 charging with CDP or SDP only



Reserved for EHCI CRC errors

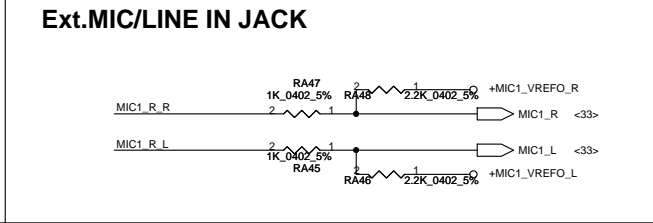
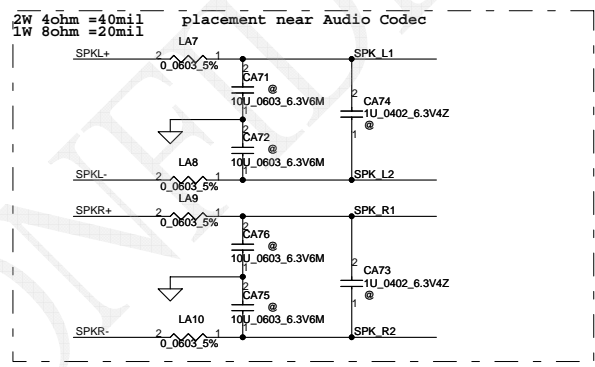
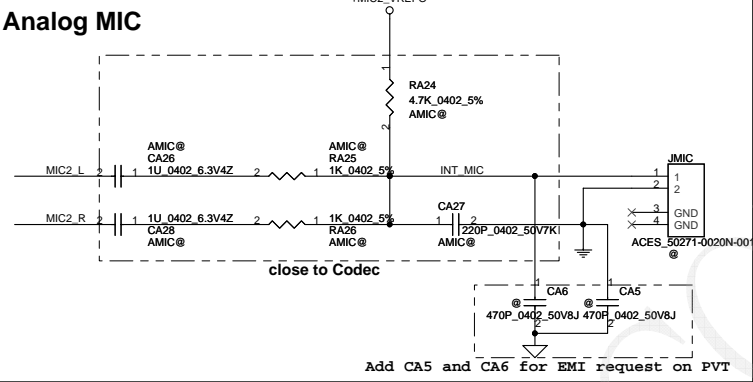
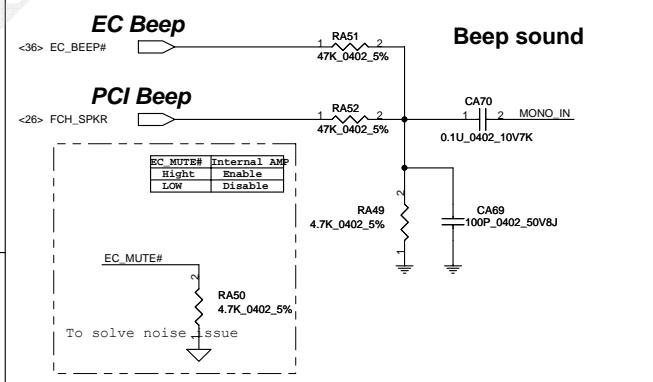
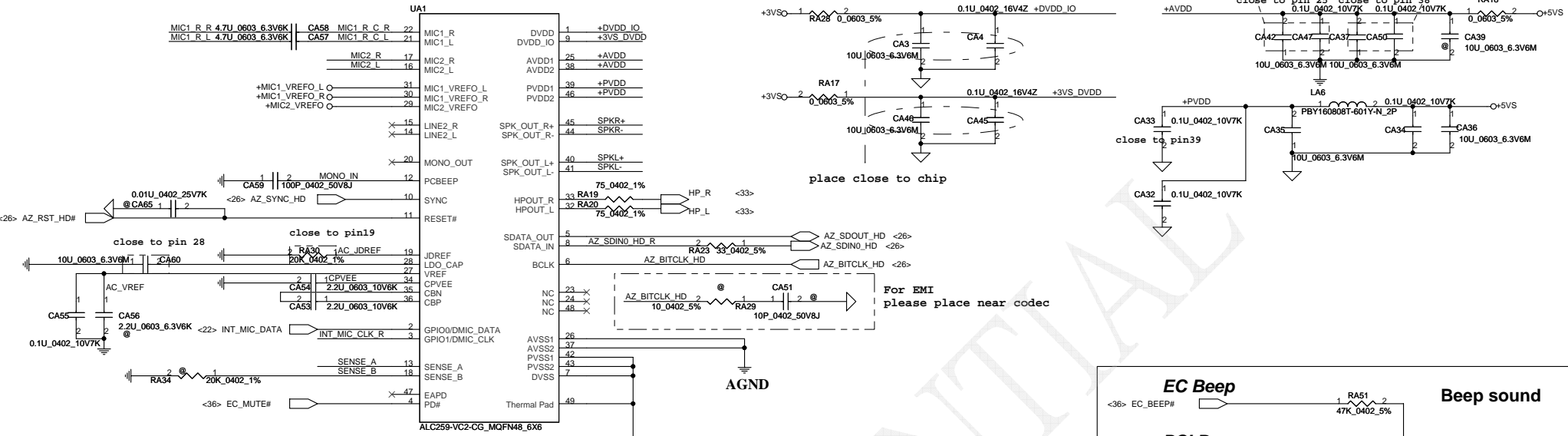


Reserved for EHCI CRC errors

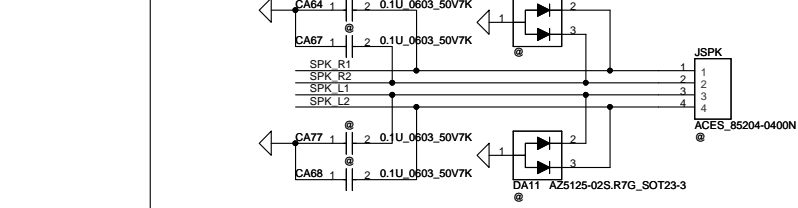
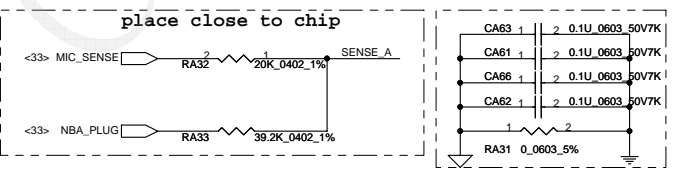


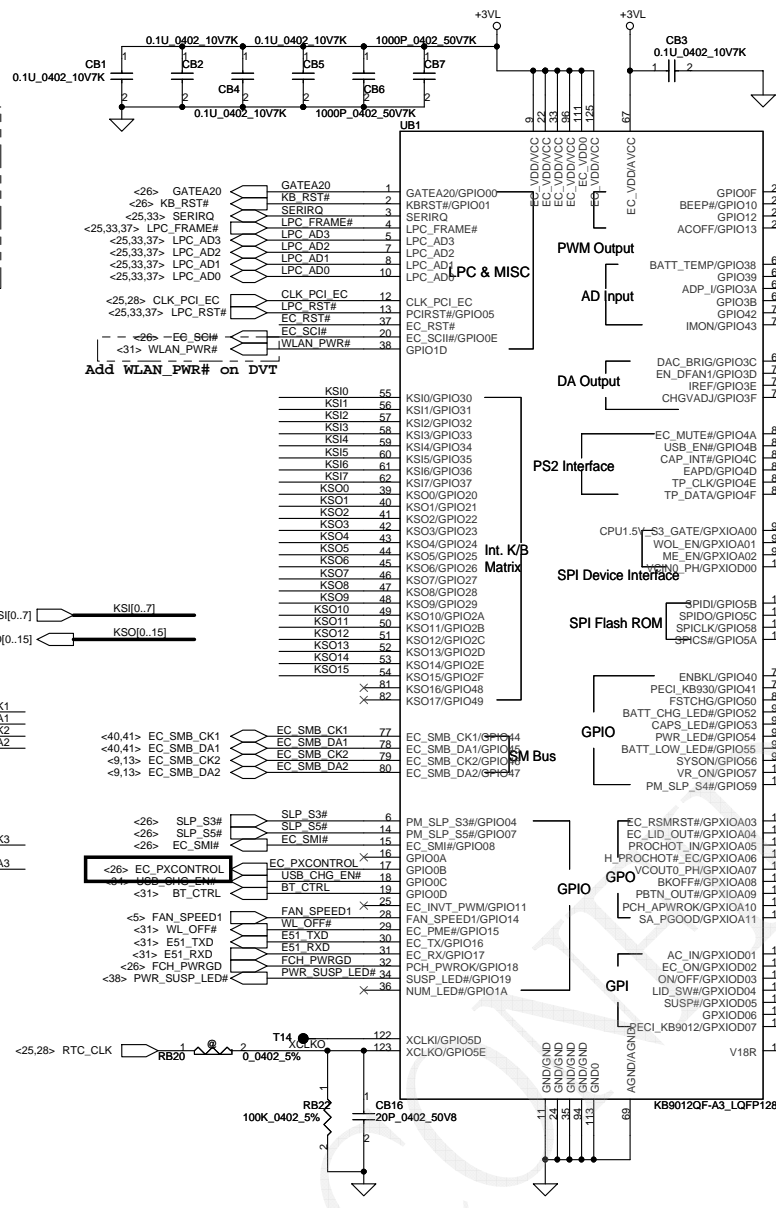
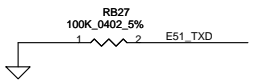
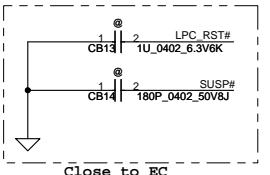
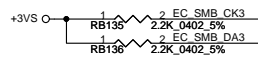
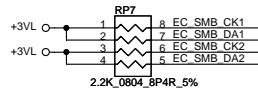
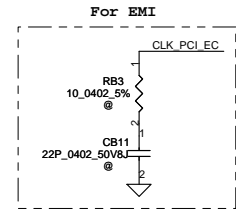
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35mA for 3.3V level



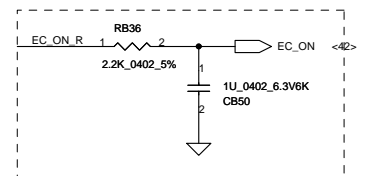
Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	(PIN 48)	
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	Analog MIC
	10K	PORT-H (PIN 20)	





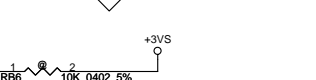
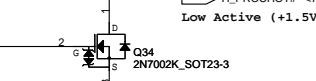
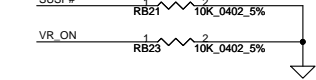
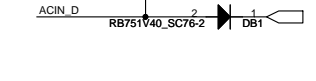
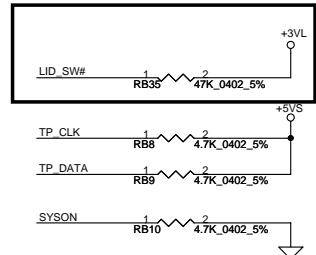
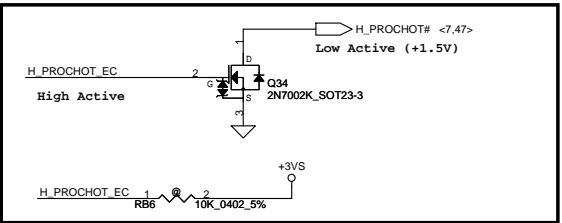
Voltage Comparator Pins FOR 9012 A3

VCIN0 pin109	>1.2V	<1.2V
VCIN1 pin102		
VCCOUT0 pin104	HIGH	LOW
VCCOUT1 pin103	LOW	HIGH

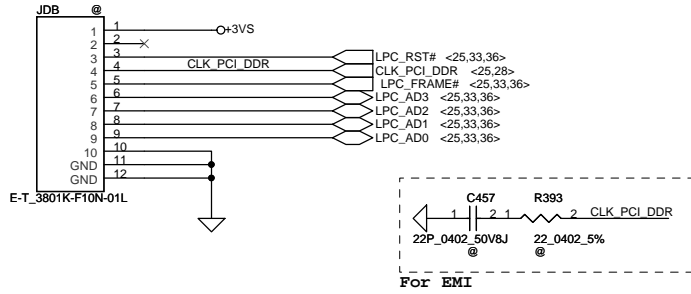


For KB9012 EC_ON Low pulse work around

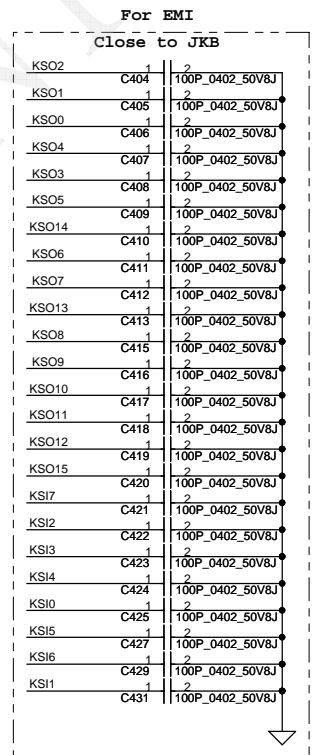
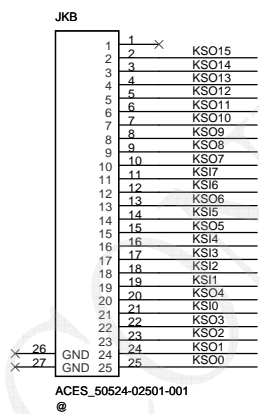
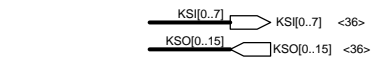
VGA_SEL	High	Low
Pin117	HIGH	LOW
Address	82h	9Ah



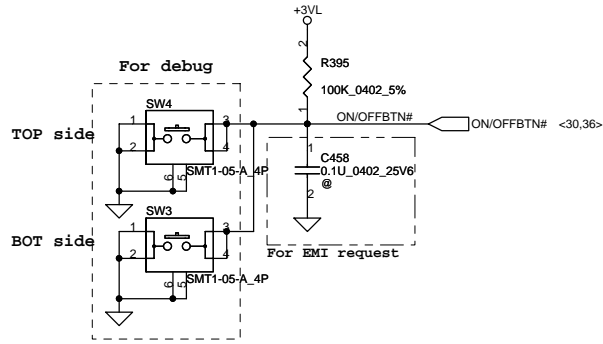
LPC Debug Port



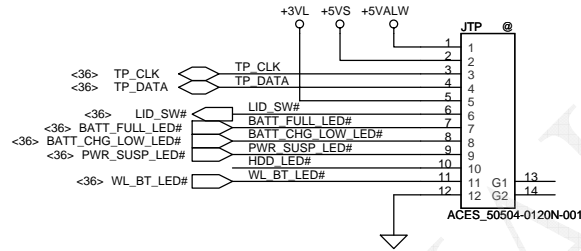
KEYBOARD CONN.



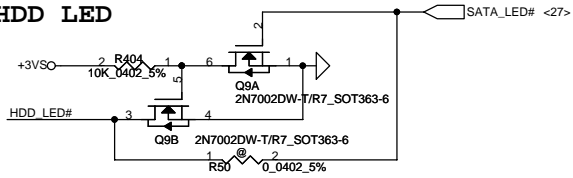
Power Button



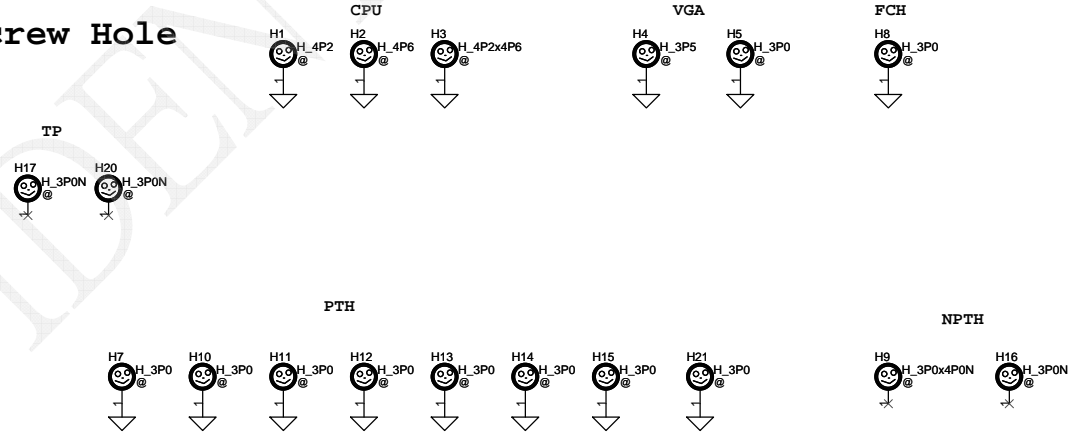
Touchpad Connector



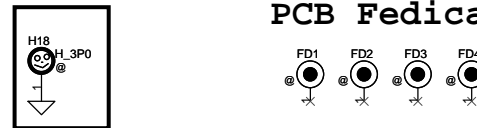
HDD LED



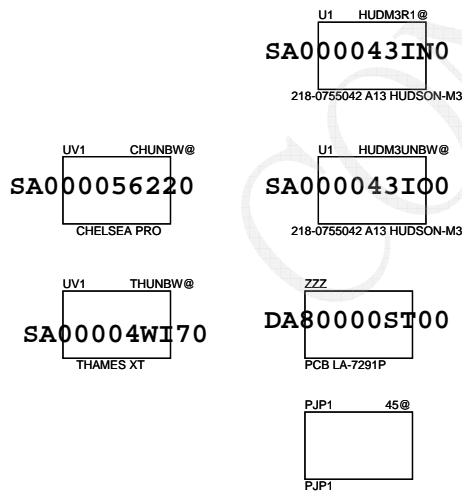
Screw Hole



PCB Federal Mark PAD

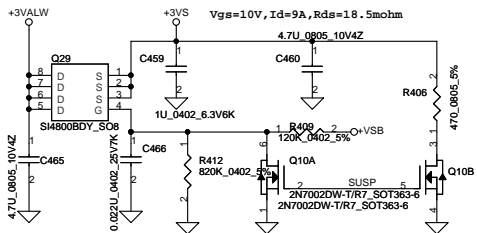


ISPD

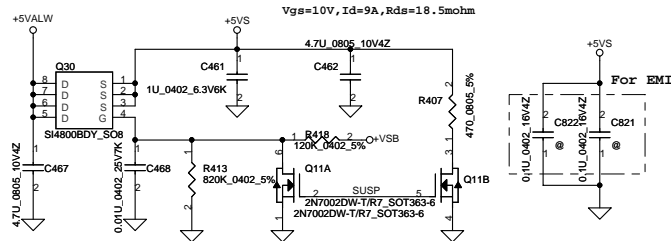


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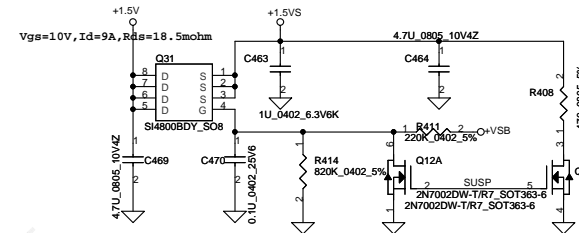
+3VALW TO +3VS



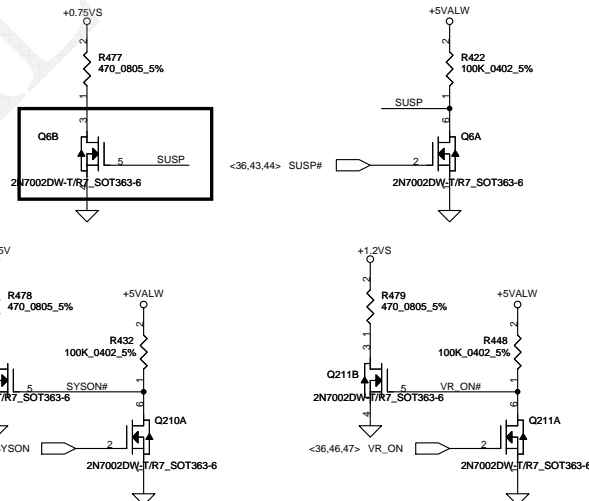
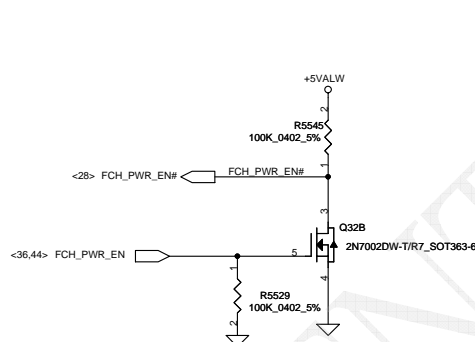
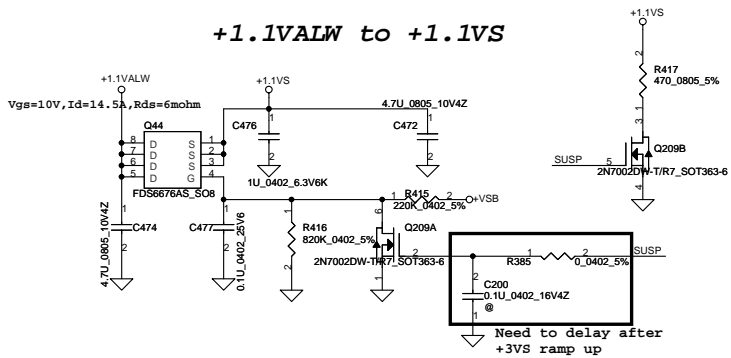
+5VALW TO +5VS



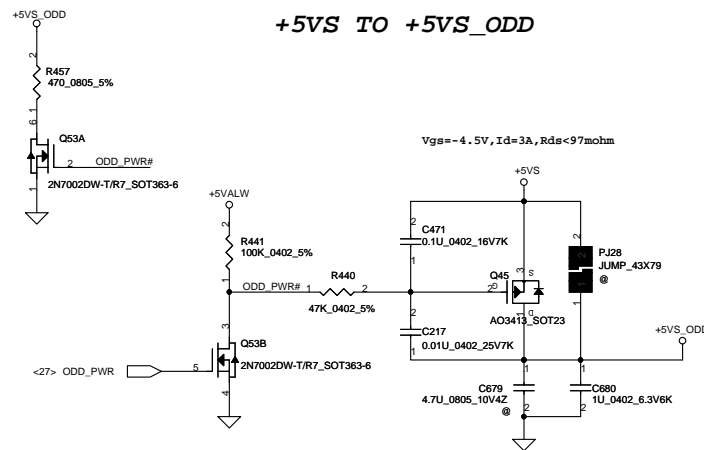
+1.5V to +1.5VS



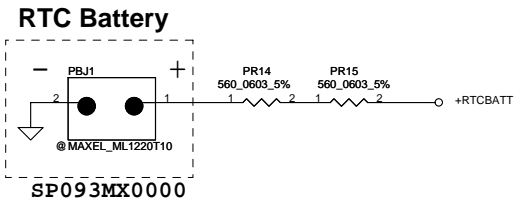
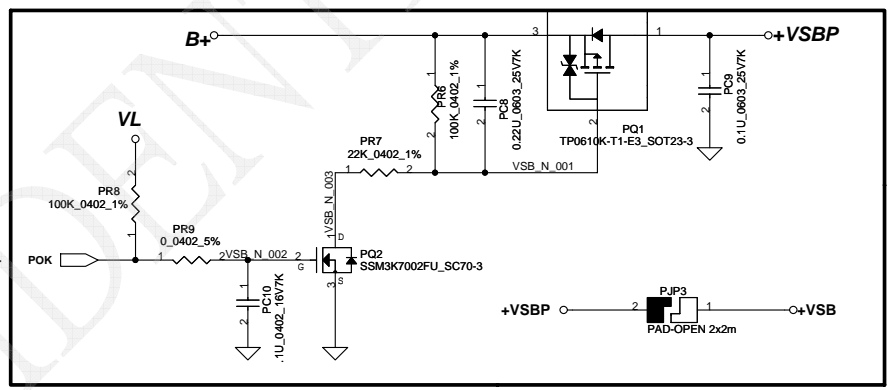
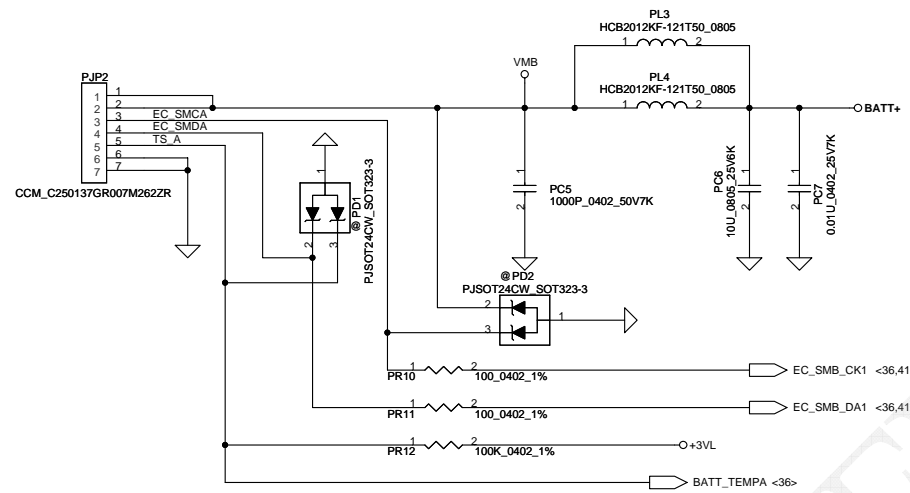
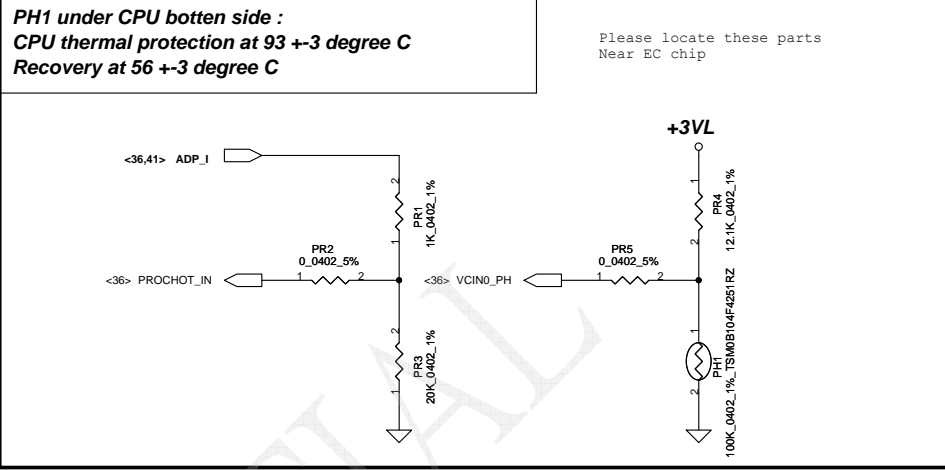
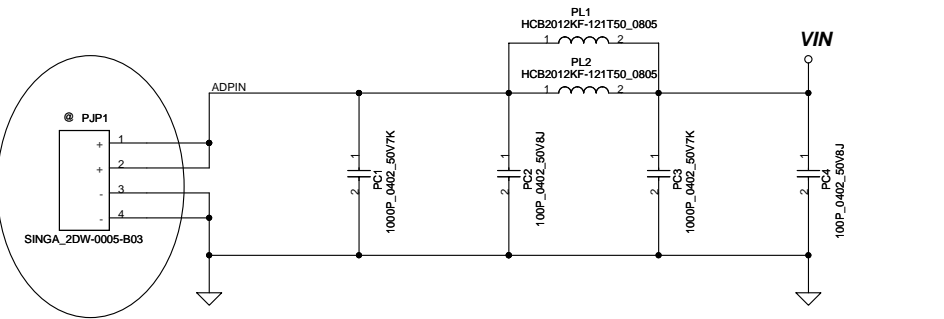
+1.1VALW to +1.1VS



+5VS TO +5VS_ODD

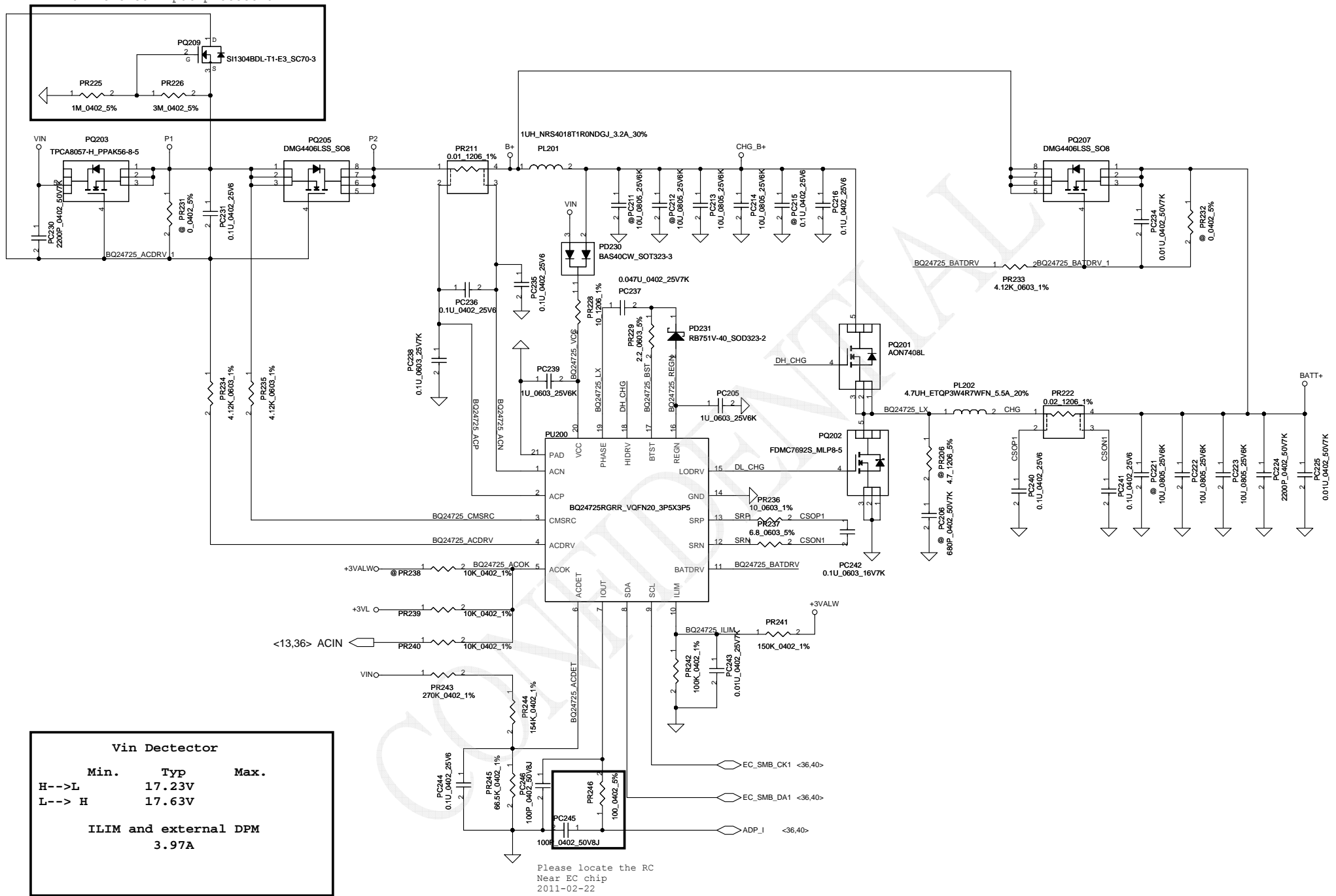


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for reverse input protection



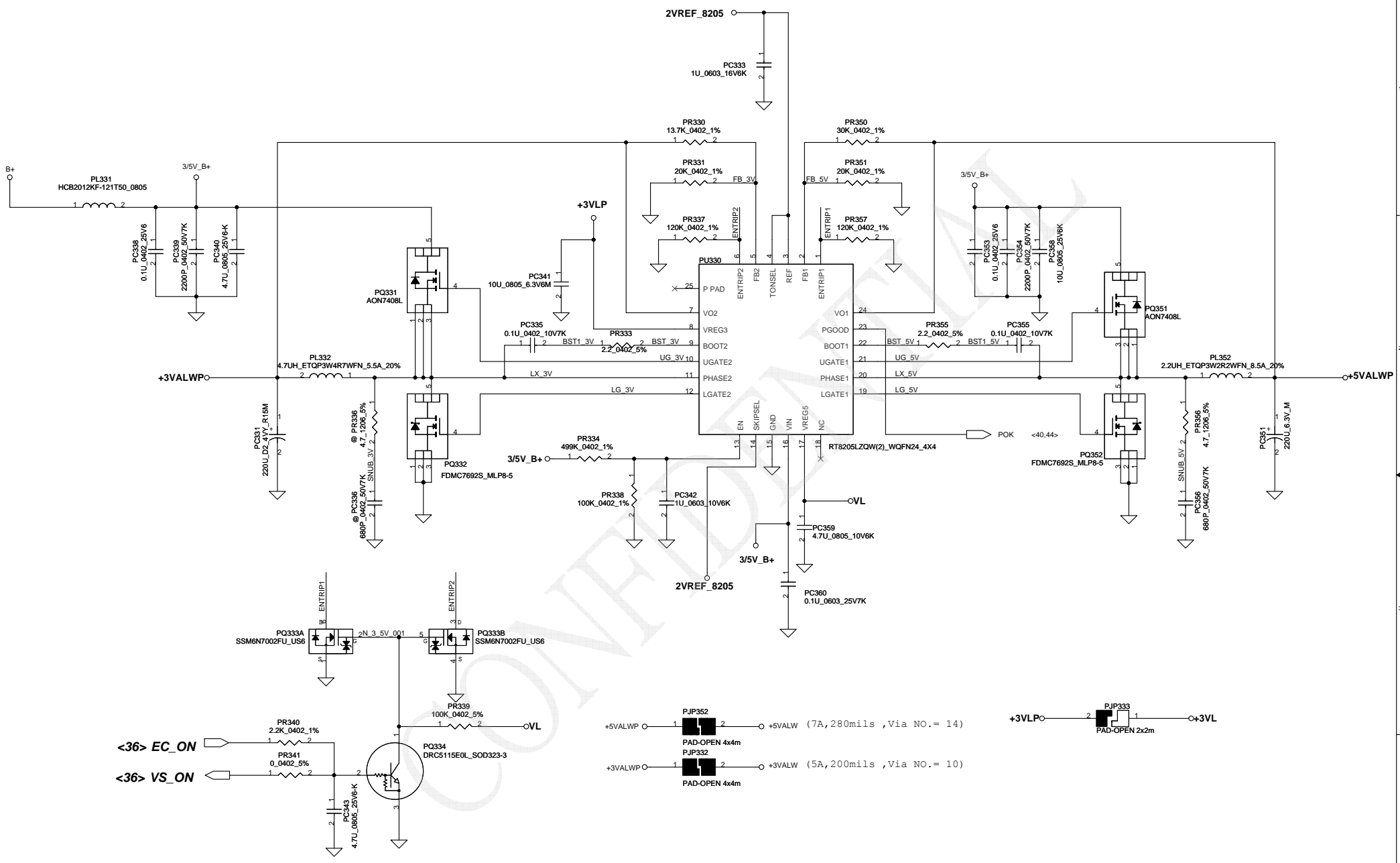
Vin Detector

	Min.	Typ	Max.
H-->L		17.23V	
L-->H		17.63V	

ILIM and external DPM
3.97A

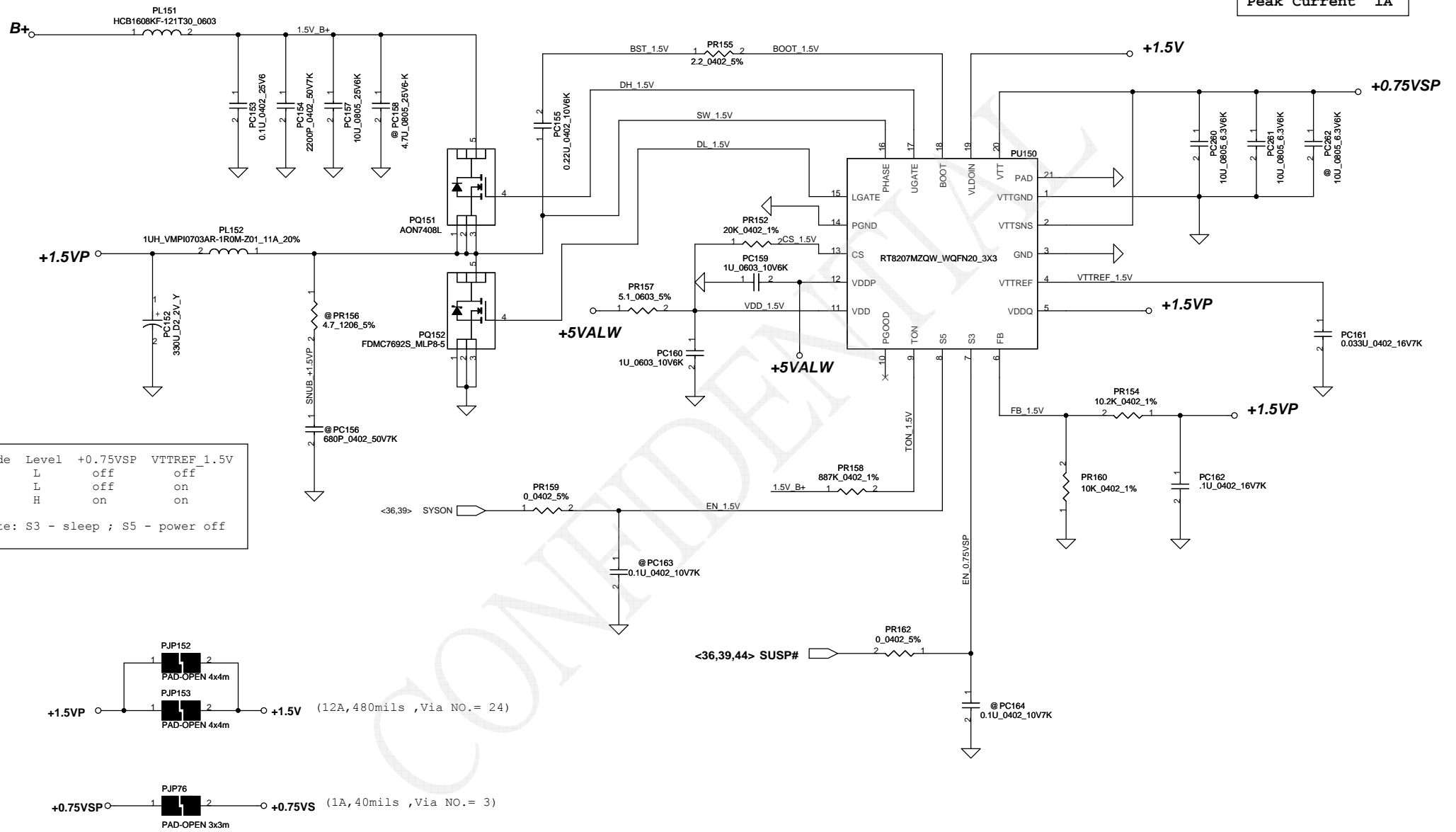
Please locate the RC
Near EC chip
2011-02-22

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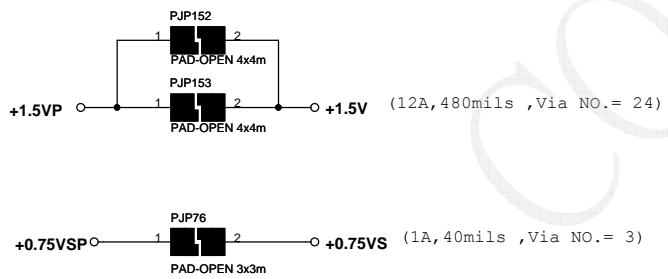


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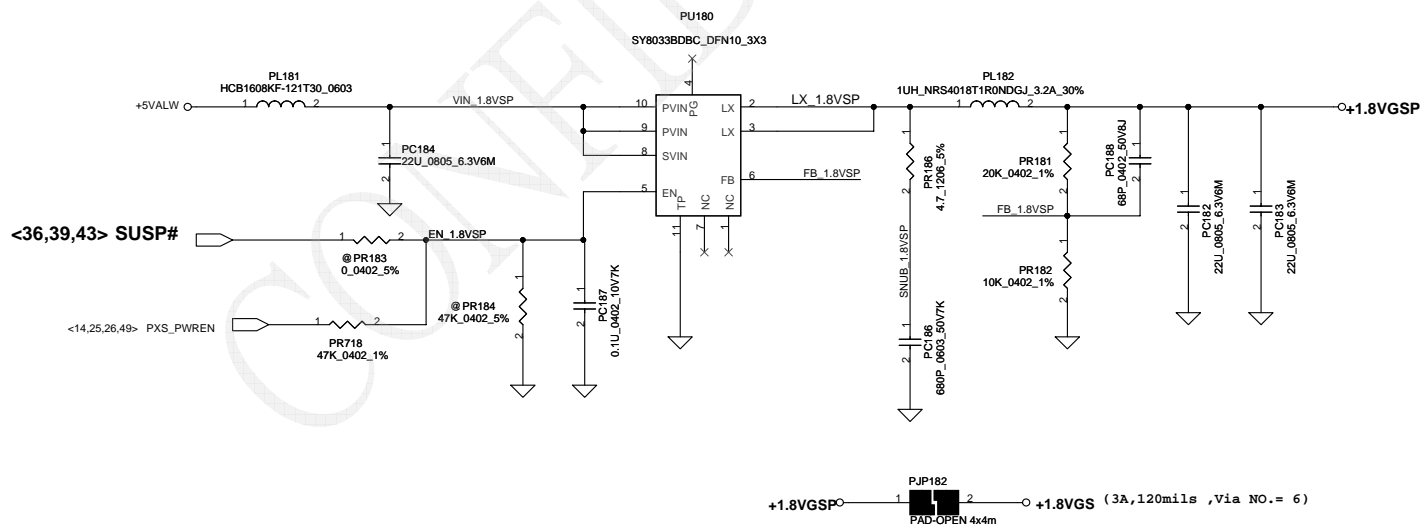
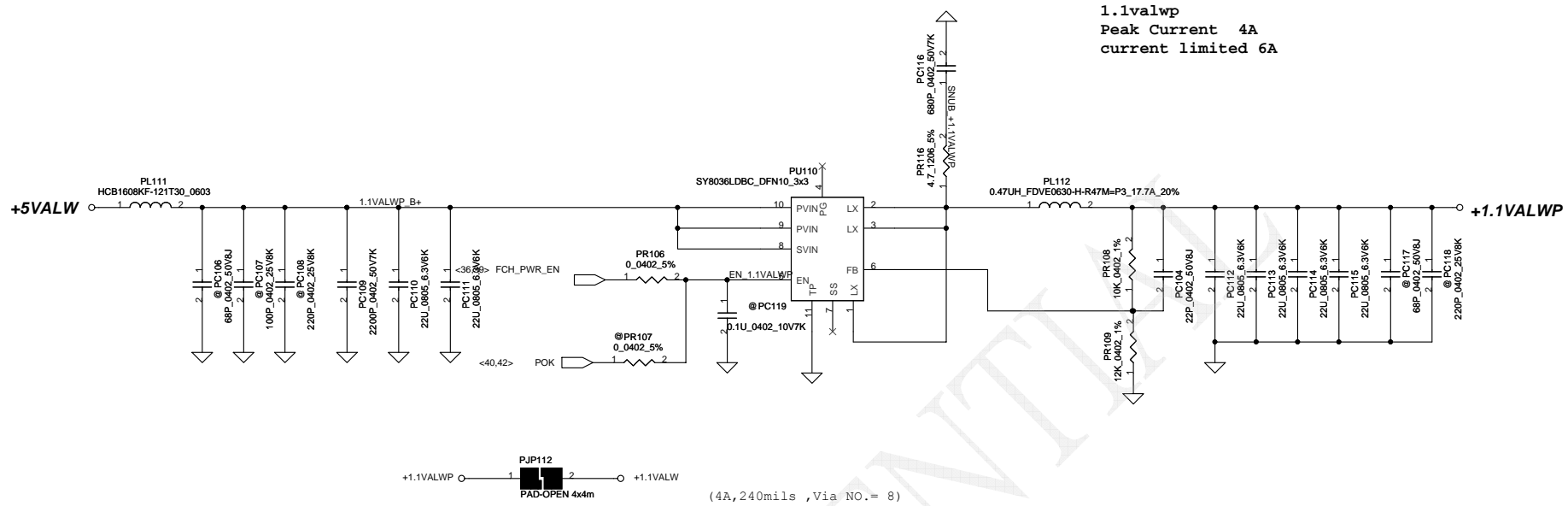
0.75Volt +/- 5%
TDC 0.7A
Peak Current 1A



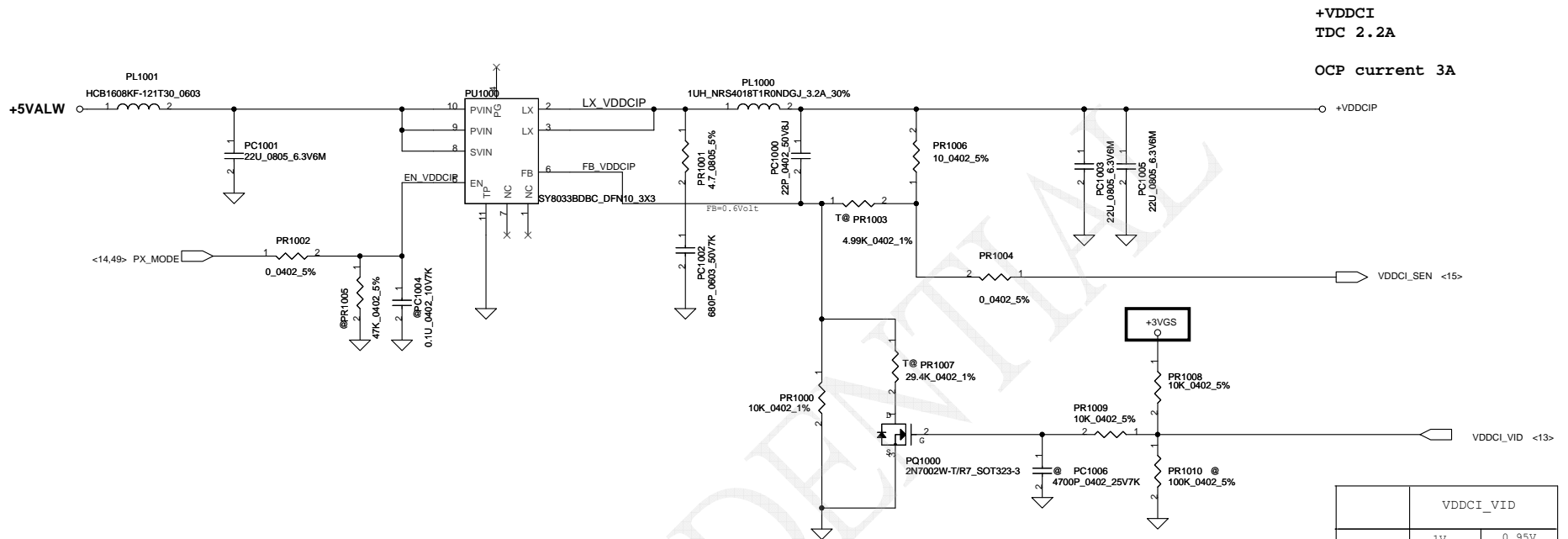
Mode Level +0.75VSP VTTREF 1.5V
S5 L off off
S3 L off on
S0 H on on
Note: S3 - sleep ; S5 - power off



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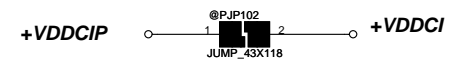


+VDDCI
TDC 2.2A
OCP current 3A

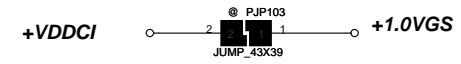
		VDDCI_VID	
High	1V	0.95V	
	PR1003 4.99K SD034499180	PR1003 5.23K SD034523180	
	PR1007 29.4K SD034294280	PR1007 86.6K SD034866280	
Low	0.9V	0.91V	
	PR1003 4.99K SD034499180	PR1003 5.23K SD034523180	
	Thames	Chelsea	

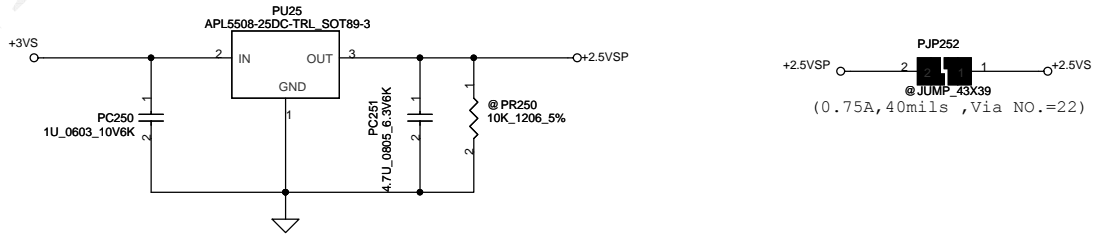
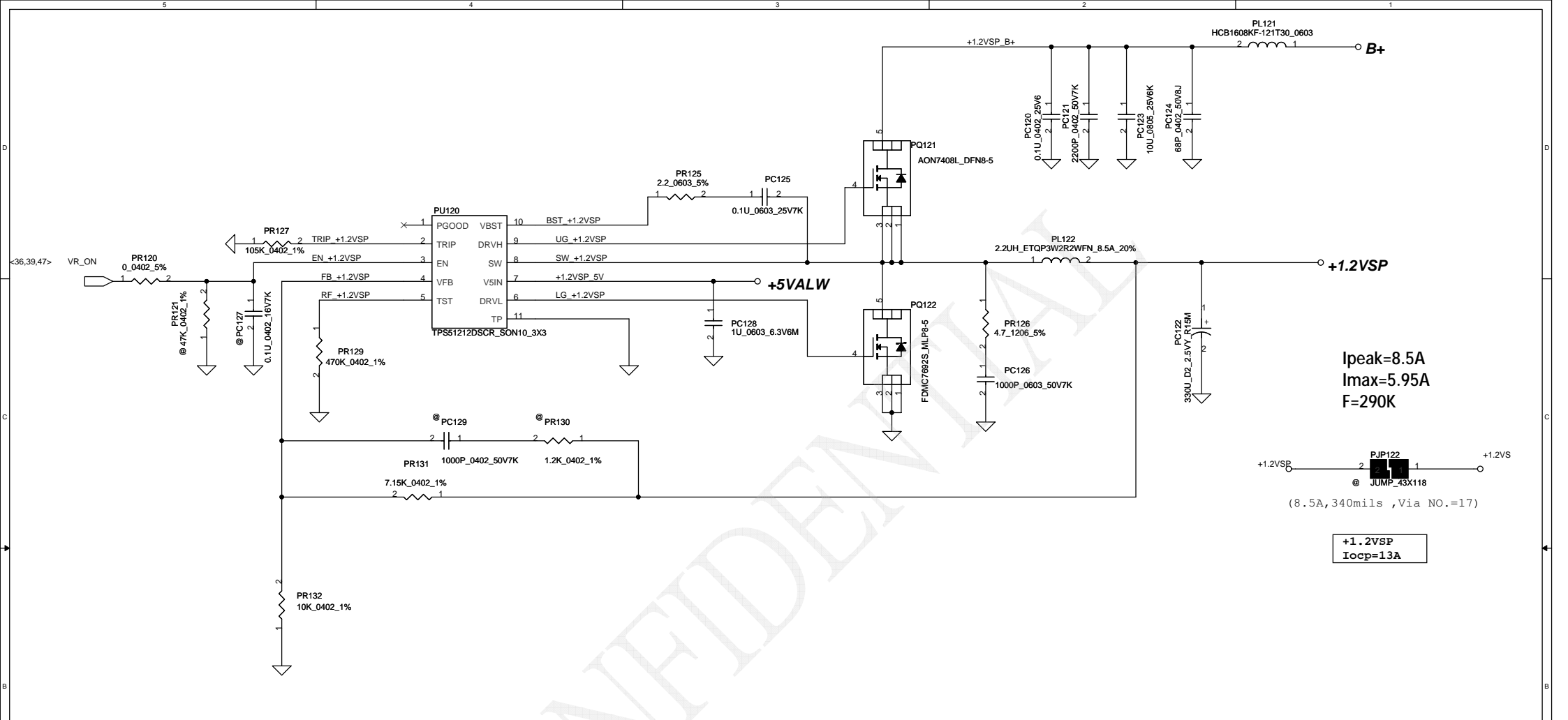
PR1003 5.23K_0402_1%
C@

PR1007 86.6K_0402_1%
C@

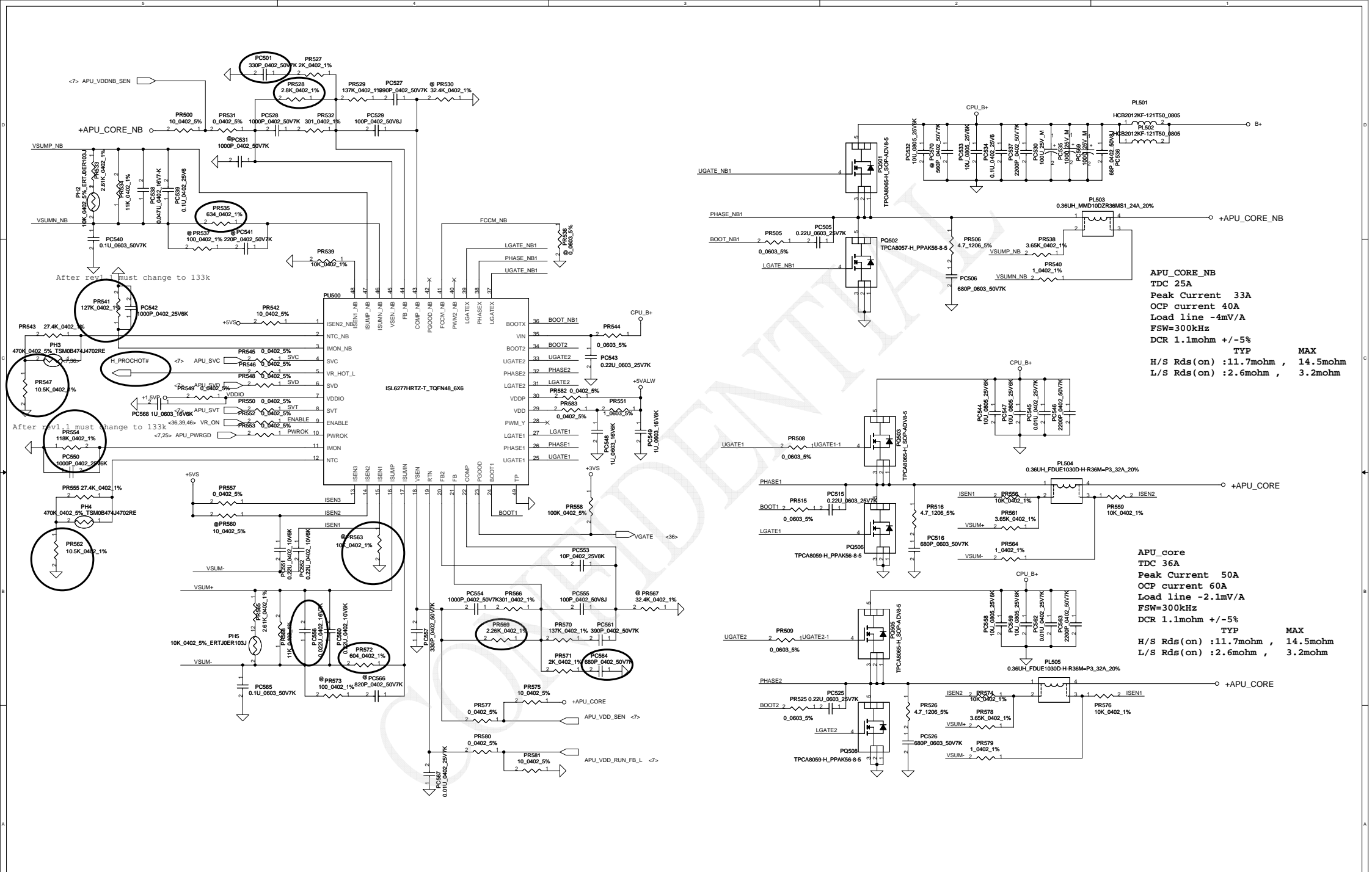


(2.2A, 100mils, Via NO. = 5)





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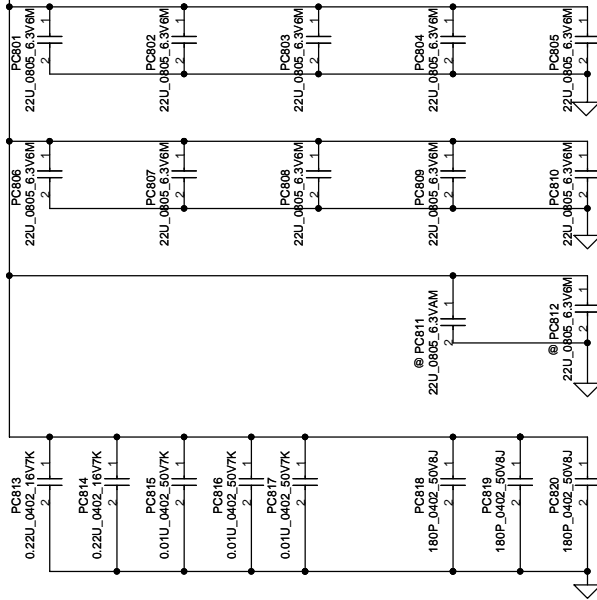
APU_CORE_NB
 TDC 25A
 Peak Current 33A
 OCP current 40A
 Load line -4mV/A
 FSW=300kHz
 DCR 1.1mohm +/-5%
 TYP
 H/S Rds(on) : 11.7mohm , 14.5mohm
 L/S Rds(on) : 2.6mohm , 3.2mohm

APU_core
 TDC 36A
 Peak Current 50A
 OCP current 60A
 Load line -2.1mV/A
 FSW=300kHz
 DCR 1.1mohm +/-5%
 TYP
 H/S Rds(on) : 11.7mohm , 14.5mohm
 L/S Rds(on) : 2.6mohm , 3.2mohm

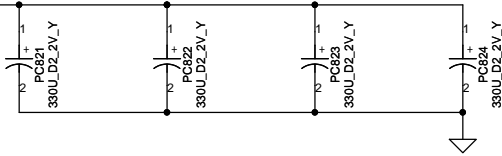
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+APU_CORE

+APU_CORE

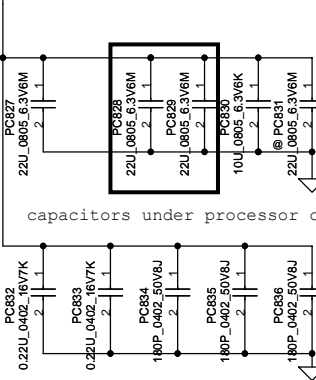


+APU_CORE Local



+APU_CORE_NB

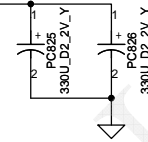
+APU_CORE_NB



capacitors under processor on bottom side of board

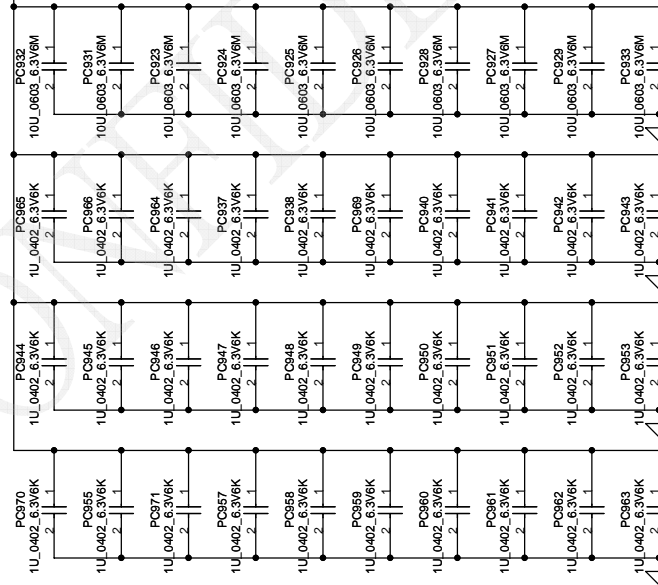
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Local

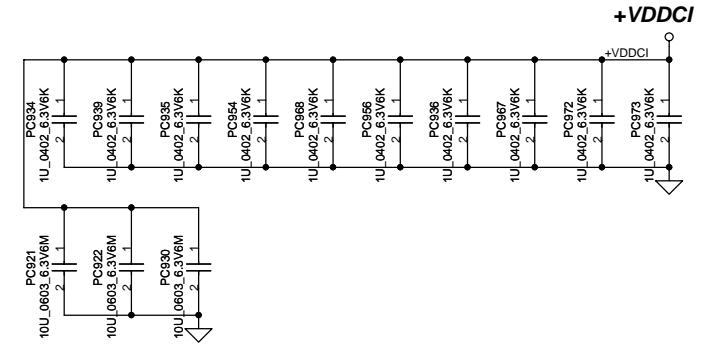


+VGA_CORE

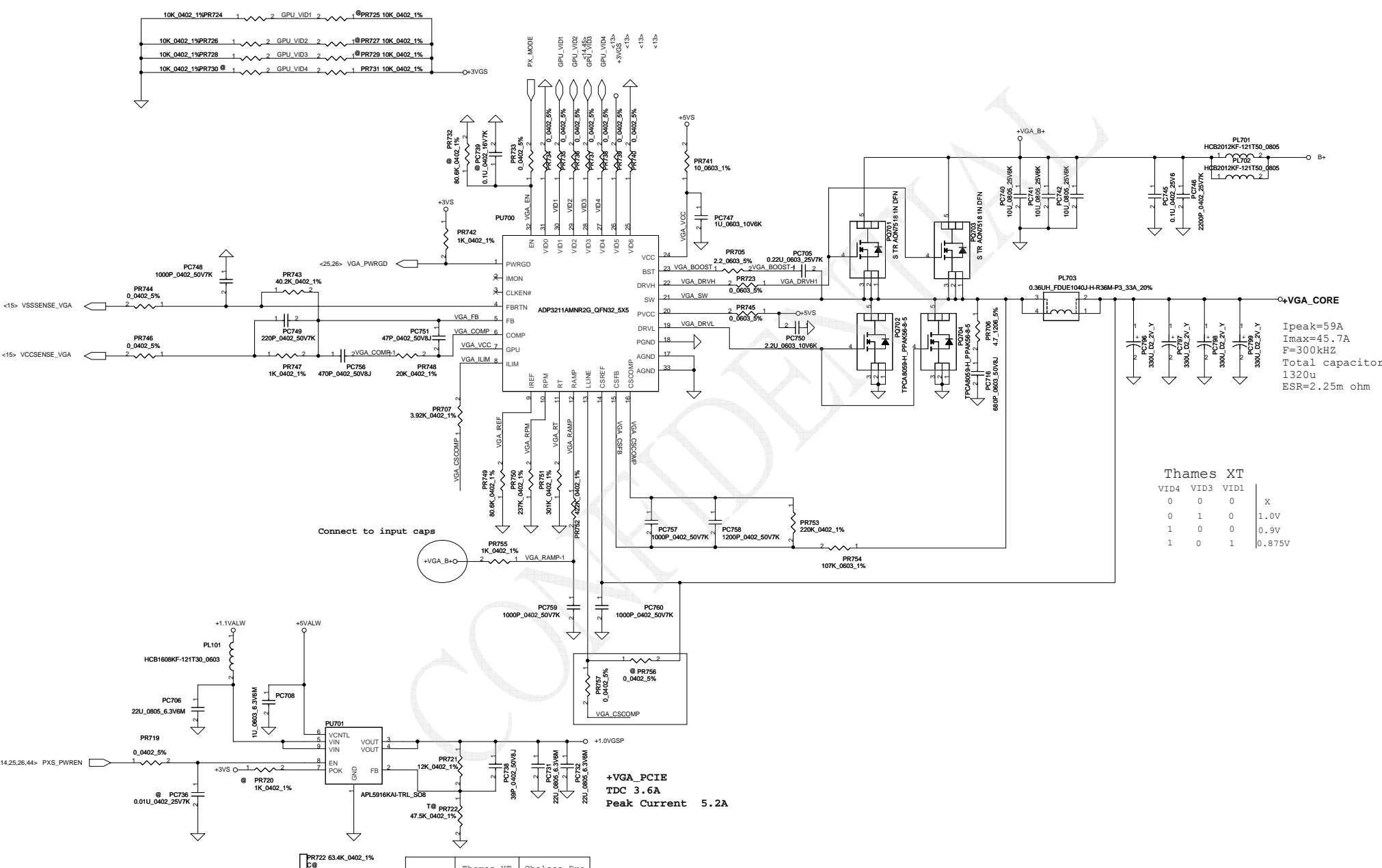
+VGA_CORE



+VDDCI



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Ipeak=59A
 Imax=45.7A
 F=300kHz
 Total capacitor
 1320u
 ESR=2.25m ohm

Thames XT

VID4	VID3	VID1	
0	0	0	X
0	1	0	1.0V
1	0	0	0.9V
1	0	1	0.875V

	Thames XT	Chelsea Pro
VGA_PCIE	1.0V	0.95V
PR722	47.5K SD034475280	63.4K SD03463K280

HW PIR (Product Improve Record)

QMLE4 LA-8863P SCHEMATIC CHANGE LIST

REVISION CHANGE: 0.1 TO 0.2

GERBER-OUT DATE: 2012/02/10

Item	Date	Page	Solution	Request
1.	1/10	P32	Add PJ31	For saving power consumption
2.	1/12	P38	Change JTP symbol to SP01001BF10	For ME request
3.	1/30	P35	Add internal MIC to MB	For customer request
4.	2/2	P14	Remove PX4.0 circuit	Support PX5.0
5.	2/2	P31	Add PJ26,PJ33, WLAN power circuit and reset pin	For customer request
6.	2/2	P33	Update JCRIO pin definition	Change int. MIC to MB
7.	2/2	P35	Remove CA64, add RA32 and RA33	Move sense resistors to MB
8.	2/3	P31	Change JWLAN symbol to SP07000TB00	For ME request
9.	2/3	P31	Add WLAN_PWR# and WLAN_RST#	For customer request
10.	2/7	P32	Change UL3 and UL4 PN to SP050005V00	For shortage

REVISION CHANGE: 0.2 TO 0.3

GERBER-OUT DATE: 2012/03/12

Item	Date	Page	Solution	Request
1.	3/1	P12	Update RTC scematic	For avoiding +3VL short to GND
2.	2/29	P22	Change R108 pull-high from +3VS to +3VALW	For LVDS sequence issue
3.	3/7	P26	Add R292 and reserve R293	To avoid PXS_PWREN floating
4.	3/7	P7	Unstuff R121~R124,R118,R119	For debug use
5.	3/7	P27	Update U13 footprint	
6.	3/7	P27/30	Connect SATA port2 to 15"ODD connector, and add GPIO54	To solve SATA EA fail issue
7.	3/8		Change RB20,RB34,R3,RV102,R425,R136,R31,R32,R33,RV284,RV287 R62,RV277 to short pad	
8.	3/12	P24	Add C201 and C214	For EMI request
9.	3/12	P30	Add C364 and C365	For EMI request
10.	3/12	P35	Add CA5, CA6, CA64, CA67, CA68 and CA77	For EMI request
11.	3/14	P8	Add C147 co-layout with C100	To avoid damage by SMT process
12.	3/14	P10	Add C148 co-layout with C218	To avoid damage by SMT process

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NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1.	2012/02/14	P40-PWR-DCIN/BATT CONN/OTP	Delete PR12,PR13	Circuit modify
2.	2012/02/14	P41-PWR-CHARGER	Change PR211 to 0.01 1206 1%,PL201 to 1UH 4*4*2 Add PC207, PC208, PC217, PC218, Delete PC232, PC233	Circuit modify
3.	2012/02/14	P43-PWR-1.5VP/+0.75VSP	Change PL152 to SH00000KS00	Circuit modify
4.	2012/02/14	P44-PWR-+1.1VALWP/+1.8VSP	Change PR718 to 47K, add PC187	HW request
5.	2012/02/14	P46-+1.2VSP/+2.5VSP PR127 to SD034105380	Change PL122 to 2.2uH(SH00000MR00),	Circuit modify
6.	2012/02/14	P37-PWR +CPU CORE	Change PQ502 to TPCA8057	Circuit modify
7.	2012/03/06	P40-PWR-DCIN/BATT CONN/OTP	Add PR12(100KΩ)	Circuit modify

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