HD66790

720-channel Source Driver for 262,144-color, 64-grayscale Display on Amorphous Silicon, Low-temperature Poly-silicon TFT Panels

REJxxxxxxx-xxxxZ
Rev.1.00
May.26.2004

Description

The HD66790 is a 720-channel, 262,144-color source driver LSI for graphics display on a TFT LCD, incorporating a timing controller to adjust the timing of LCD signals.

The HD66790 supports the 18-bit RGB interface mode (via VSYNC, HSYNC, DOTCLK, ENABLE, and PD17-0) and the 6-bit RGB interface mode (via VSYNC, HSYNC, DOTCLK, ENABLE, and PD17-12) for moving picture display. As a system interface to a microcomputer, the HD66790 supports a serial interface, enabling high quality display and low power consumption drive via instruction.

The HD66790 allows for precise power management by software, which makes this LSI an ideal for medium or small-sized portable products supporting WWW browsers, such as digital cellular phones or PDAs, where long battery life is a major concern.

Features

- Incorporates an 720-channel LCD source driver circuit
- Data bits: 6-bit (grayscale) x RGB dots
- Moving picture display interface: 18-bit RGB Interface (via VSYNC, HSYNC, DOTCLK, ENABLE, PD17-0), 6-bit RGB Interface (via VSYNC, HSYNC, DOTCLK, ENABLE, PD17-12)
- Multicolor display: 262,144 colors simultaneously available
- Incorporates a timing controller to adjust the output timing of LCD signals
- System interface: Serial Peripheral Interface (SPI)
- Reversible source driver shift direction
- Incorporates a level shifter for LCD signals
- High-speed operation: fDOTCLK = 25MHz (Max.)
- TFT display capacitor structure: Cst structure (C storage on Common)
- Generates supply voltages to the TFT display common electrode
- Vcom AC drive
- Operating power supply voltage range

  Input supply voltages
  - Logic supply voltage: Vcc = 2.5V ~ 3.6V
  - Analog supply voltage: Vci = 2.5V ~ 3.6V
  - Interface supply voltage: IOVcc = 1.65V ~ 3.6V

  LCD drive supply voltages
  - Source driver supply voltage: DDVDH = 4.0V ~ 5.5V
  - Gate driver supply voltages: VGH–VGL = 10V ~ 37.5V
    VGH–AGND = 6.0V ~ 20.0V
    VGL–AGND = -4.0V ~ -17.5V
    VcomH-VcomL = 4.0V ~ 5.5V

  Output supply voltages
  - LCD panel output: SOUT1-4R/L = VGL ~ VGH
  - Source output: S1 ~ S720 = AGND + 0.3V ~ DDVDH – 0.3V
  - Internal step-up circuits DDVDH: VLOUT1 = Vci1 x 2
    VGH: VLOUT2 = Vci1 x 6, 7, 8
    VGL: VLOUT3 = Vci1 x -5, -6, -7
    VCL: VLOUT4 = Vci1 x -1

Table 1 Product lineup

Type No.	Organization	Package
HCD667B90BP	Laced bump arrangement	Die with BUMP

Block Diagram

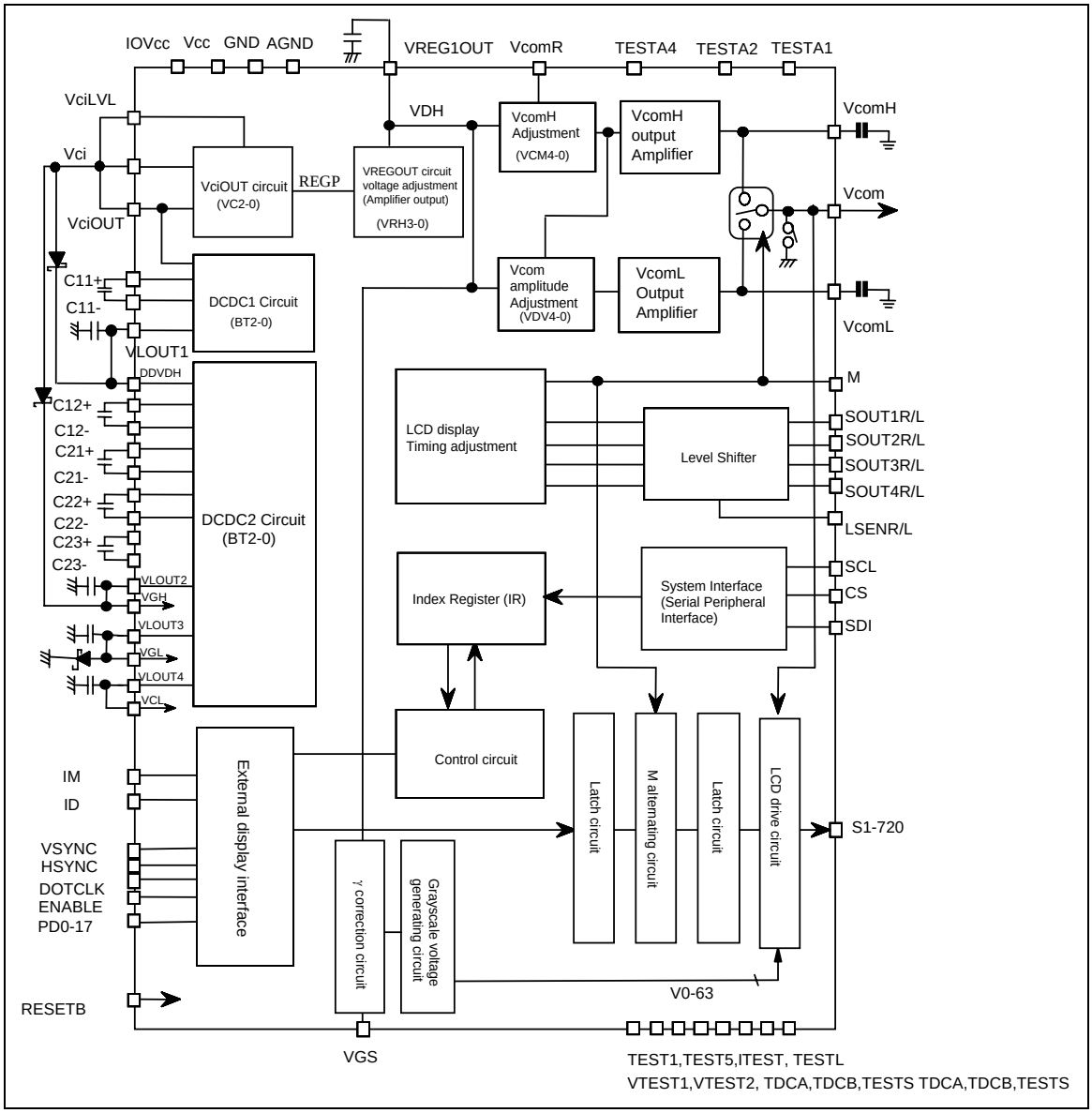

Figure 1

Block Function

(1) External Display Interface (RGB interface)

The HD66790 supports the RGB interface as an external display interface. In RGB-I/F mode, the HD66790 operates in synchronization with externally supplied signals (VSYNC, HSYNC, and DOTCLK), and takes in data according to data enable signal (ENABLE). See "RGB interface timing" for details.

The correspondence between input and output data is as follows.

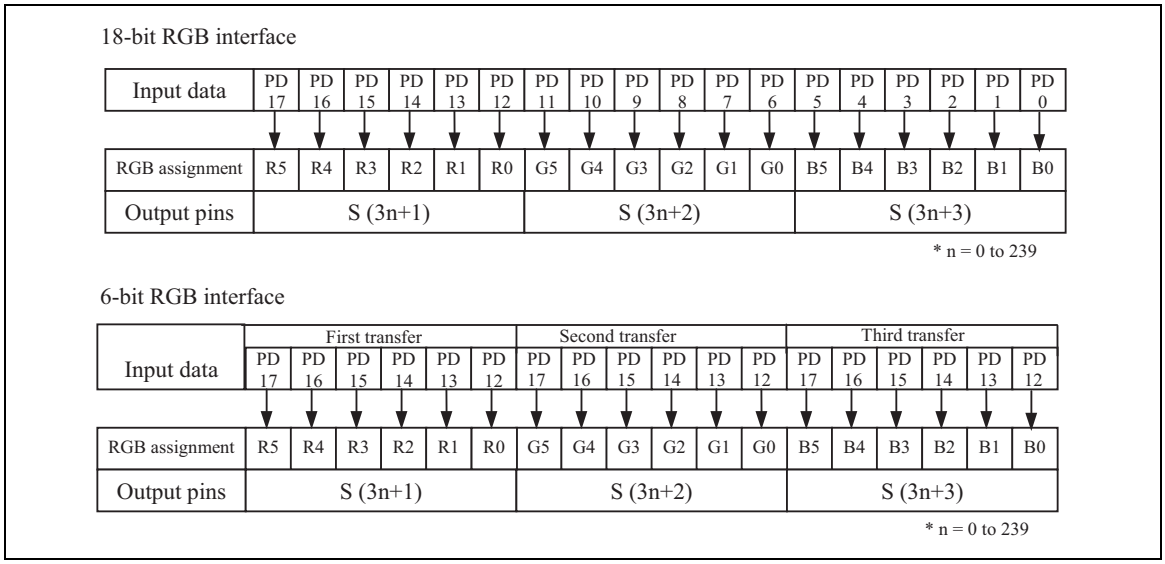

Figure 2

(2) Control circuit

The control circuit generates internal control signals from various signals.

(3) Grayscale Voltage Generating Circuit

The grayscale voltage generating circuit generates 64 grayscale voltage levels each for positive and negative polarities by dividing externally input voltages with resistors to display in 262,144 colors. See "Configuration of Grayscale Amplifier" for details.

(4) Timing Generator

The timing generator generates timing signals for LCD operation.

(5) LCD Driver Circuit

The LCD driver circuit consists of a 720 source-output (S1~S720) driver, latching display pattern data in units of lines and generates drive waveforms. The shift direction of source outputs can be switched between either from (S1, S2, S3) to (S718, S719, S720) or from (S718, S719, S720) to (S1, S2, S3), whichever suitable for the module.

(6) VCOM amplitude generator

The VCOM amplitude generator generates an amplitude signal VcomS to generate Vcom, which is supplied to the TFT LCD panel's common electrode. The AC voltage Vcom alternates between arbitrarily set two levels (VcomR and GND) in sync with an alternating cycle signal.

(7) Level shifter

The level shifter generates gate line driving supply voltages from logic supply voltages by changing the amplitude from Vcc-GND to VGH-VGL.

(8) System interface clock synchronizing serial circuit

The system interface clock synchronizing serial circuit enables setting modes of the HD66790 by setting registers.

(9) Vci internal reference voltage generating circuit

The Vci internal reference voltage generating circuit generates an internal reference voltage REGP from Vci for generating VciOUT and VREG1OUT levels. See "Instruction" for details.

(10) VciOUT output circuit

The VciOUT output circuit outputs the VciOUT level, which is input to the step-up circuit 1 (DCDC1) from Vci1 pin. See " Instruction" for details.

(11) Step-up circuit 1 (DCDC1)

The step-up circuit 1 steps up the VciOUT twice to output as VLOUT1. VLOUT1 then generates the supply voltage DDVDH. See "Instruction" for details.

(12) Step-up circuit 2 (DCDC2)

The step-up circuit 2 generates the respective VLOUT2, 3, 4 levels by using both VciOUT and VDDVH. VLOUT2 and VLOUT3 are connected to VGH and VGL pins, respectively. See "Instruction " for details.

(13) VREG1 regulator

The VREG1 regulator multiplies the REGP level by a constant number and then output into the VREG1. See “Instruction” for details.

(14) Level sift circuit

The level sifter changes the amplitude of signal from Vcc-GND. See “Electrical characteristics” for details.

Pin Arrangement

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●Chip size: 18.90 mm×2.30 mm
●Chip thickness: 550μm(typ.)
●Pad coordinates: PAD center
●Coordinates origin: Chip center

●Au bump size
(1) 54μm×100μm
Input side: No.1~No.198

(2) 26μm×90μm
Staggered output side: No.251~No.886

(3) 90μm×26μm
Staggered output side: No.205~No.246,
No.891~No.932

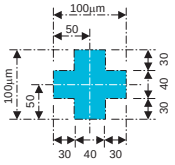
(4) 100μm×100μm
DUMMY pins: No.199, No.938

(5) 90μm×26μm
DUMMY pins: No.200~No.204, No.247, No.248
DUMMY pins: No.889, No.890, No.933~No.937

(6) 26μm×90μm
DUMMY pins: No.249, No.250, No.887, No.888

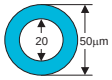
●Au bump pitch: See PAD coordinates
●Au bump height:15μm(typ.)
●No. in the figure corresponds No. in the PAD coordinates

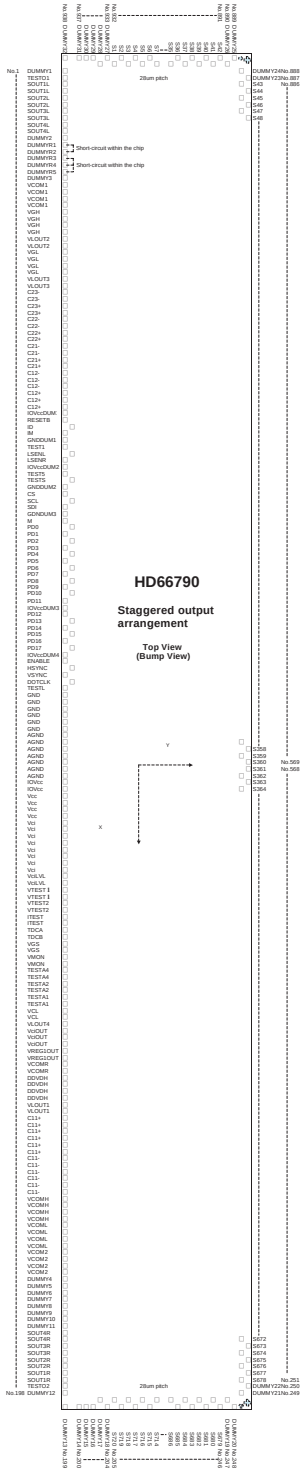
●Alignment mark
(1) arrangement: 2 places
Coordinates (X, Y) = (±9244.5, 944.4)



(2-a) Coordinates (X, Y) = (-9294.4, 802.5)

(2-b) Coordinates (X, Y) = (9294.4, 802.5)





PAD Coordinate

No.	Pad Name	X	Y
1	DUMMY1	-9037.6	-990.7
2	TESTO1	-8952.0	-990.7
3	SOUT1L	-8853.6	-990.7
4	SOUT1L	-8768.0	-990.7
5	SOUT2L	-8682.4	-990.7
6	SOUT2L	-8596.8	-990.7
7	SOUT3L	-8511.2	-990.7
8	SOUT3L	-8425.5	-990.7
9	SOUT4L	-8339.9	-990.7
10	SOUT4L	-8254.3	-990.7
11	DUMMY2	-8155.9	-990.7
12	DUMMYR1	-8070.3	-990.7
13	DUMMYR2	-7984.7	-990.7
14	DUMMYR3	-7899.1	-990.7
15	DUMMYR4	-7813.5	-990.7
16	DUMMYR5	-7727.9	-990.7
17	DUMMY3	-7642.3	-990.7
18	VCOM1	-7543.8	-990.7
19	VCOM1	-7458.2	-990.7
20	VCOM1	-7372.6	-990.7
21	VCOM1	-7287.0	-990.7
22	VGH	-7162.2	-990.7
23	VGH	-7076.6	-990.7
24	VGH	-6991.0	-990.7
25	VGH	-6905.4	-990.7
26	VLOUT2	-6803.2	-990.7
27	VLOUT2	-6717.6	-990.7
28	VGL	-6592.7	-990.7
29	VGL	-6507.1	-990.7
30	VGL	-6421.5	-990.7
31	VGL	-6335.9	-990.7
32	VLOUT3	-6224.7	-990.7
33	VLOUT3	-6139.1	-990.7
34	C23-	-6027.8	-990.7
35	C23-	-5942.2	-990.7
36	C23+	-5856.6	-990.7
37	C23+	-5771.0	-990.7
38	C22-	-5685.4	-990.7
39	C22-	-5599.8	-990.7
40	C22+	-5514.2	-990.7
41	C22+	-5428.6	-990.7
42	C21-	-5343.0	-990.7
43	C21-	-5257.4	-990.7
44	C21+	-5171.7	-990.7
45	C21+	-5086.1	-990.7
46	C12-	-5000.5	-990.7
47	C12-	-4914.9	-990.7
48	C12-	-4829.3	-990.7
49	C12+	-4710.3	-990.7
50	C12+	-4624.7	-990.7
51	C12+	-4539.1	-990.7
52	IOVCCDUM1	-4336.2	-990.7
53	RESETB	-4218.6	-990.7
54	ID	-4159.8	-850.7
55	IM	-4100.9	-990.7
56	GNDDUM1	-3983.3	-990.7
57	TEST1	-3865.7	-990.7
58	LSENL	-3806.9	-850.7
59	LSENR	-3748.1	-990.7
60	IOVCCDUM2	-3630.5	-990.7
61	TEST5	-3512.8	-990.7
62	TESTS	-3454.0	-850.7
63	GNDDUM2	-3336.4	-990.7
64	CS	-3218.8	-990.7
65	SCL	-3160.0	-850.7
66	SDI	-3101.1	-990.7
67	GNDDUM3	-2983.5	-990.7
68	M	-2865.9	-990.7
69	PD0	-2807.1	-850.7
70	PD1	-2748.3	-990.7
71	PD2	-2689.5	-850.7
72	PD3	-2630.6	-990.7
73	PD4	-2571.8	-850.7
74	PD5	-2513.0	-990.7
75	PD6	-2454.2	-850.7
76	PD7	-2395.4	-990.7
77	PD8	-2336.6	-850.7
78	PD9	-2277.8	-990.7
79	PD10	-2219.0	-850.7
80	PD11	-2160.2	-990.7
81	IOVCCDUM3	-2042.5	-990.7
82	PD12	-1924.9	-990.7
83	PD13	-1866.1	-850.7
84	PD14	-1807.3	-990.7
85	PD15	-1748.5	-850.7
86	PD16	-1689.7	-990.7
87	PD17	-1630.8	-850.7
88	IOVCCDUM4	-1513.2	-990.7
89	ENABLE	-1395.6	-990.7
90	HSYNC	-1336.8	-850.7
91	VSYNC	-1278.0	-990.7
92	DOTCLK	-1219.2	-850.7
93	TESTL	-1160.3	-990.7
94	GND	-986.7	-990.7
95	GND	-901.1	-990.7
96	GND	-815.5	-990.7
97	GND	-704.5	-990.7
98	GND	-618.9	-990.7
99	GND	-533.3	-990.7
100	AGND	-422.5	-990.7
101	AGND	-336.9	-990.7
102	AGND	-251.3	-990.7
103	AGND	-165.6	-990.7
104	AGND	-80.0	-990.7
105	AGND	5.6	-990.7
106	AGND	91.2	-990.7
107	IOVCC	210.0	-990.7
108	IOVCC	295.6	-990.7
109	VCC	422.4	-990.7
110	VCC	508.0	-990.7
111	VCC	634.8	-990.7
112	VCC	720.4	-990.7
113	VCI	848.5	-990.7
114	VCI	934.1	-990.7
115	VCI	1019.8	-990.7
116	VCI	1105.4	-990.7
117	VCI	1225.8	-990.7
118	VCI	1311.4	-990.7
119	VCI	1397.0	-990.7

120	VCI	1482.6	-990.7
121	VCILVL	1626.4	-990.7
122	VCILVL	1712.0	-990.7
123	VTEST1	1838.8	-990.7
124	VTEST1	1924.4	-990.7
125	VTEST2	2010.0	-990.7
126	VTEST2	2095.7	-990.7
127	ITEST	2181.3	-990.7
128	ITEST	2266.9	-990.7
129	TDCA	2393.7	-990.7
130	TDCB	2479.3	-990.7
131	VGS	2606.1	-990.7
132	VGS	2691.7	-990.7
133	VMON	2777.3	-990.7
134	VMON	2862.9	-990.7
135	TESTA4	2981.9	-990.7
136	TESTA4	3102.3	-990.7
137	TESTA2	3230.5	-990.7
138	TESTA2	3316.1	-990.7
139	TESTA1	3401.7	-990.7
140	TESTA1	3487.3	-990.7
141	VCL	3606.3	-990.7
142	VCL	3691.9	-990.7
143	VLOUT4	3803.2	-990.7
144	VCIOUT	3947.0	-990.7
145	VCIOUT	4032.6	-990.7
146	VCIOUT	4118.2	-990.7
147	VREG1OUT	4245.0	-990.7
148	VREG1OUT	4330.6	-990.7
149	VCOMR	4416.2	-990.7
150	VCOMR	4501.8	-990.7
151	DDVDH	4630.0	-990.7
152	DDVDH	4715.6	-990.7
153	DDVDH	4836.0	-990.7
154	DDVDH	4921.6	-990.7
155	VLOUT1	5040.7	-990.7
156	VLOUT1	5159.4	-990.7
157	C11+	5278.2	-990.7
158	C11+	5363.8	-990.7
159	C11+	5449.4	-990.7
160	C11+	5535.1	-990.7
161	C11+	5620.7	-990.7
162	C11+	5706.3	-990.7
163	C11-	5791.9	-990.7
164	C11-	5877.5	-990.7
165	C11-	5963.1	-990.7
166	C11-	6048.7	-990.7
167	C11-	6134.3	-990.7
168	C11-	6219.9	-990.7
169	VCOMH	6363.8	-990.7
170	VCOMH	6449.4	-990.7
171	VCOMH	6569.8	-990.7
172	VCOMH	6655.4	-990.7
173	VCOML	6775.8	-990.7
174	VCOML	6861.4	-990.7
175	VCOML	6981.8	-990.7
176	VCOML	7067.4	-990.7
177	VCOM2	7187.8	-990.7
178	VCOM2	7273.4	-990.7
179	VCOM2	7359.0	-990.7
180	VCOM2	7444.6	-990.7
181	DUMMY4	7543.1	-990.7
182	DUMMY5	7628.7	-990.7
183	DUMMY6	7714.3	-990.7
184	DUMMY7	7799.9	-990.7
185	DUMMY8	7885.5	-990.7
186	DUMMY9	7971.1	-990.7
187	DUMMY10	8056.7	-990.7
188	DUMMY11	8142.3	-990.7
189	SOUT4R	8240.8	-990.7
190	SOUT4R	8326.4	-990.7
191	SOUT3R	8412.0	-990.7
192	SOUT3R	8497.6	-990.7
193	SOUT2R	8583.2	-990.7
194	SOUT2R	8668.8	-990.7
195	SOUT1R	8754.4	-990.7
196	SOUT1R	8840.0	-990.7
197	TESTO2	8938.4	-990.7
198	DUMMY12	9024.0	-990.7
199	DUMMY13	9290.8	-990.7
200	DUMMY14	9295.8	-758.2
201	DUMMY15	9295.8	-702.2
202	DUMMY16	9295.8	-646.2
203	DUMMY17	9160.8	-618.2
204	DUMMY18	9295.8	-590.2
205	S720	9160.8	-562.2
206	S719	9295.8	-534.2
207	S718	9160.8	-506.2
208	S717	9295.8	-478.2
209	S716	9160.8	-450.2
210	S715	9295.8	-422.2
211	S714	9160.8	-394.2
212	S713	9295.8	-366.2
213	S712	9160.8	-338.2
214	S711	9295.8	-310.2
215	S710	9160.8	-282.2
216	S709	9295.8	-254.2
217	S708	9160.8	-226.2
218	S707	9295.8	-198.2
219	S706	9160.8	-170.2
220	S705	9295.8	-142.2
221	S704	9160.8	-114.2
222	S703	9295.8	-86.2
223	S702	9160.8	-58.2
224	S701	9295.8	-30.2
225	S700	9160.8	-2.2
226	S699	9295.8	25.8
227	S698	9160.8	53.8
228	S697	9295.8	81.8
229	S696	9160.8	109.8
230	S695	9295.8	137.8
231	S694	9160.8	165.8
232	S693	9295.8	193.8
233	S692	9160.8	221.8
234	S691	9295.8	249.8
235	S690	9160.8	277.8
236	S689	9295.8	305.8
237	S688	9160.8	333.8
238	S687	9295.8	361.8
239	S686	9160.8	389.8
240	S685	9295.8	417.8
241	S684	9160.8	445.8
242	S683	9295.8	473.8
243	S682	9160.8	501.8
244	S681	9295.8	529.8
245	S680	9160.8	557.8

246	S679	9295.8	585.8
247	DUMMY19	9160.8	613.8
248	DUMMY20	9295.8	641.8
249	DUMMY21	8960.0	860.7
250	DUMMY22	8932.0	995.7
251	S678	8904.0	860.7
252	S677	8876.0	995.7
253	S676	8848.0	860.7
254	S675	8820.0	995.7
255	S674	8792.0	860.7
256	S673	8764.0	995.7
257	S672	8736.0	860.7
258	S671	8708.0	995.7
259	S670	8680.0	860.7
260	S669	8652.0	995.7
261	S668	8624.0	860.7
262	S667	8596.0	995.7
263	S666	8568.0	860.7
264	S665	8540.0	995.7
265	S664	8512.0	860.7
266	S663	8484.0	995.7
267	S662	8456.0	860.7
268	S661	8428.0	995.7
269	S660	8400.0	860.7
270	S659	8372.0	995.7
271	S658	8344.0	860.7
272	S657	8316.0	995.7
273	S656	8288.0	860.7
274	S655	8260.0	995.7
275	S654	8232.0	860.7
276	S653	8204.0	995.7
277	S652	8176.0	860.7
278	S651	8148.0	995.7
279	S650	8120.0	860.7
280	S649	8092.0	995.7
281	S648	8064.0	860.7
282	S647	8036.0	995.7
283	S646	8008.0	860.7
284	S645	7980.0	995.7
285	S644	7952.0	860.7
286	S643	7924.0	995.7
287	S642	7896.0	860.7
288	S641	7868.0	995.7
289	S640	7840.0	860.7
290	S639	7812.0	995.7
291	S638	7784.0	860.7
292	S637	7756.0	995.7
293	S636	7728.0	860.7
294	S635	7700.0	995.7
295	S634	7672.0	860.7
296	S633	7644.0	995.7
297	S632	7616.0	860.7
298	S631	7588.0	995.7
299	S630	7560.0	860.7
300	S629	7532.0	995.7
301	S628	7504.0	860.7
302	S627	7476.0	995.7
303	S626	7448.0	860.7
304	S625	7420.0	995.7
305	S624	7392.0	860.7
306	S623	7364.0	995.7
307	S622	7336.0	860.7
308	S621	7308.0	995.7
309	S620	7280.0	860.7
310	S619	7252.0	995.7
311	S618	7224.0	860.7
312	S617	7196.0	995.7
313	S616	7168.0	860.7
314	S615	7140.0	995.7
315	S614	7112.0	860.7
316	S613	7084.0	995.7
317	S612	7056.0	860.7
318	S611	7028.0	995.7
319	S610	7000.0	860.7
320	S609	6972.0	995.7
321	S608	6944.0	860.7
322	S607	6916.0	995.7
323	S606	6888.0	860.7
324	S605	6860.0	995.7
325	S604	6832.0	860.7
326	S603	6804.0	995.7
327	S602	6776.0	860.7
328	S601	6748.0	995.7
329	S600	6720.0	860.7
330	S599	6692.0	995.7
331	S598	6664.0	860.7
332	S597	6636.0	995.7
333	S596	6608.0	860.7
334	S595	6580.0	995.7
335	S594	6552.0	860.7
336	S593	6524.0	995.7
337	S592	6496.0	860.7
338	S591	6468.0	995.7
339	S590	6440.0	860.7
340	S589	6412.0	995.7
341	S588	6384.0	860.7
342	S587	6356.0	995.7
343	S586	6328.0	860.7
344	S585	6300.0	995.7
345	S584	6272.0	860.7
346	S583	6244.0	995.7
347	S582	6216.0	860.7
348	S581	6188.0	995.7
349	S580	6160.0	860.7
350	S579	6132.0	995.7
351	S578	6104.0	860.7
352	S577	6076.0	995.7
353	S576	6048.0	860.7
354	S575	6020.0	995.7
355	S574	5992.0	860.7
356	S573	5964.0	995.7
357	S572	5936.0	860.7
358	S571	5908.0	995.7
359	S570	5880.0	860.7
360	S569	5852.0	995.7
361	S568	5824.0	860.7
362	S567	5796.0	995.7
363	S566	5768.0	860.7
364	S565	5740.0	995.7
365	S564	5712.0	860.7
366	S563	5684.0	995.7
367	S562	5656.0	860.7
368	S561	5628.0	995.7
369	S560	5600.0	860.7
370	S559	5572.0	995.7
371	S558	5544.0	860.7

372	S557	5516.0	995.7
373	S556	5488.0	860.7
374	S555	5460.0	995.7
375	S554	5432.0	860.7
376	S553	5404.0	995.7
377	S552	5376.0	860.7
378	S551	5348.0	995.7
379	S550	5320.0	860.7
380	S549	5292.0	995.7
381	S548	5264.0	860.7
382	S547	5236.0	995.7
383	S546	5208.0	860.7
384	S545	5180.0	995.7
385	S544	5152.0	860.7
386	S543	5124.0	995.7
387	S542	5096.0	860.7
388	S541	5068.0	995.7
389	S540	5040.0	860.7
390	S539	5012.0	995.7
391	S538	4984.0	860.7
392	S537	4956.0	995.7
393	S536	4928.0	860.7
394	S535	4900.0	995.7
395	S534	4872.0	860.7
396	S533	4844.0	995.7
397	S532	4816.0	860.7
398	S531	4788.0	995.7
399	S530	4760.0	860.7
400	S529	4732.0	995.7
401	S528	4704.0	860.7
402	S527	4676.0	995.7
403	S526	4648.0	860.7
404	S525	4620.0	995.7
405	S524	4592.0	860.7
406	S523	4564.0	995.7
407	S522	4536.0	860.7
408	S521	4508.0	995.7
409	S520	4480.0	860.7
410	S519	4452.0	995.7
411	S518	4424.0	860.7
412	S517	4396.0	995.7
413	S516	4368.0	860.7

414	S515	4340.0	995.7
415	S514	4312.0	860.7
416	S513	4284.0	995.7
417	S512	4256.0	860.7
418	S511	4228.0	995.7
419	S510	4200.0	860.7
420	S509	4172.0	995.7
421	S508	4144.0	860.7
422	S507	4116.0	995.7
423	S506	4088.0	860.7
424	S505	4060.0	995.7
425	S504	4032.0	860.7
426	S503	4004.0	995.7
427	S502	3976.0	860.7
428	S501	3948.0	995.7
429	S500	3920.0	860.7
430	S499	3892.0	995.7
431	S498	3864.0	860.7
432	S497	3836.0	995.7
433	S496	3808.0	860.7
434	S495	3780.0	995.7
435	S494	3752.0	860.7
436	S493	3724.0	995.7
437	S492	3696.0	860.7
438	S491	3668.0	995.7
439	S490	3640.0	860.7
440	S489	3612.0	995.7
441	S488	3584.0	860.7
442	S487	3556.0	995.7
443	S486	3528.0	860.7
444	S485	3500.0	995.7
445	S484	3472.0	860.7
446	S483	3444.0	995.7
447	S482	3416.0	860.7
448	S481	3388.0	995.7
449	S480	3360.0	860.7
450	S479	3332.0	995.7
451	S478	3304.0	860.7
452	S477	3276.0	995.7
453	S476	3248.0	860.7
454	S475	3220.0	995.7
455	S474	3192.0	860.7

456	S473	3164.0	995.7
457	S472	3136.0	860.7
458	S471	3108.0	995.7
459	S470	3080.0	860.7
460	S469	3052.0	995.7
461	S468	3024.0	860.7
462	S467	2996.0	995.7
463	S466	2968.0	860.7
464	S465	2940.0	995.7
465	S464	2912.0	860.7
466	S463	2884.0	995.7
467	S462	2856.0	860.7
468	S461	2828.0	995.7
469	S460	2800.0	860.7
470	S459	2772.0	995.7
471	S458	2744.0	860.7
472	S457	2716.0	995.7
473	S456	2688.0	860.7
474	S455	2660.0	995.7
475	S454	2632.0	860.7
476	S453	2604.0	995.7
477	S452	2576.0	860.7
478	S451	2548.0	995.7
479	S450	2520.0	860.7
480	S449	2492.0	995.7
481	S448	2464.0	860.7
482	S447	2436.0	995.7
483	S446	2408.0	860.7
484	S445	2380.0	995.7
485	S444	2352.0	860.7
486	S443	2324.0	995.7
487	S442	2296.0	860.7
488	S441	2268.0	995.7
489	S440	2240.0	860.7
490	S439	2212.0	995.7
491	S438	2184.0	860.7
492	S437	2156.0	995.7
493	S436	2128.0	860.7
494	S435	2100.0	995.7
495	S434	2072.0	860.7
496	S433	2044.0	995.7
497	S432	2016.0	860.7

498	S431	1988.0	995.7
499	S430	1960.0	860.7
500	S429	1932.0	995.7
501	S428	1904.0	860.7
502	S427	1876.0	995.7
503	S426	1848.0	860.7
504	S425	1820.0	995.7
505	S424	1792.0	860.7
506	S423	1764.0	995.7
507	S422	1736.0	860.7
508	S421	1708.0	995.7
509	S420	1680.0	860.7
510	S419	1652.0	995.7
511	S418	1624.0	860.7
512	S417	1596.0	995.7
513	S416	1568.0	860.7
514	S415	1540.0	995.7
515	S414	1512.0	860.7
516	S413	1484.0	995.7
517	S412	1456.0	860.7
518	S411	1428.0	995.7
519	S410	1400.0	860.7
520	S409	1372.0	995.7
521	S408	1344.0	860.7
522	S407	1316.0	995.7
523	S406	1288.0	860.7
524	S405	1260.0	995.7
525	S404	1232.0	860.7
526	S403	1204.0	995.7
527	S402	1176.0	860.7
528	S401	1148.0	995.7
529	S400	1120.0	860.7
530	S399	1092.0	995.7
531	S398	1064.0	860.7
532	S397	1036.0	995.7
533	S396	1008.0	860.7
534	S395	980.0	995.7
535	S394	952.0	860.7
536	S393	924.0	995.7
537	S392	896.0	860.7
538	S391	868.0	995.7
539	S390	840.0	860.7

540	S389	812.0	995.7
541	S388	784.0	860.7
542	S387	756.0	995.7
543	S386	728.0	860.7
544	S385	700.0	995.7
545	S384	672.0	860.7
546	S383	644.0	995.7
547	S382	616.0	860.7
548	S381	588.0	995.7
549	S380	560.0	860.7
550	S379	532.0	995.7
551	S378	504.0	860.7
552	S377	476.0	995.7
553	S376	448.0	860.7
554	S375	420.0	995.7
555	S374	392.0	860.7
556	S373	364.0	995.7
557	S372	336.0	860.7
558	S371	308.0	995.7
559	S370	280.0	860.7
560	S369	252.0	995.7
561	S368	224.0	860.7
562	S367	196.0	995.7
563	S366	168.0	860.7
564	S365	140.0	995.7
565	S364	112.0	860.7
566	S363	84.0	995.7
567	S362	56.0	860.7
568	S361	28.0	995.7
569	S360	-28.0	995.7
570	S359	-56.0	860.7
571	S358	-84.0	995.7
572	S357	-112.0	860.7
573	S356	-140.0	995.7
574	S355	-168.0	860.7
575	S354	-196.0	995.7
576	S353	-224.0	860.7
577	S352	-252.0	995.7
578	S351	-280.0	860.7
579	S350	-308.0	995.7
580	S349	-336.0	860.7
581	S348	-364.0	995.7

582	S347	-392.0	860.7
583	S346	-420.0	995.7
584	S345	-448.0	860.7
585	S344	-476.0	995.7
586	S343	-504.0	860.7
587	S342	-532.0	995.7
588	S341	-560.0	860.7
589	S340	-588.0	995.7
590	S339	-616.0	860.7
591	S338	-644.0	995.7
592	S337	-672.0	860.7
593	S336	-700.0	995.7
594	S335	-728.0	860.7
595	S334	-756.0	995.7
596	S333	-784.0	860.7
597	S332	-812.0	995.7
598	S331	-840.0	860.7
599	S330	-868.0	995.7
600	S329	-896.0	860.7
601	S328	-924.0	995.7
602	S327	-952.0	860.7
603	S326	-980.0	995.7
604	S325	-1008.0	860.7
605	S324	-1036.0	995.7
606	S323	-1064.0	860.7
607	S322	-1092.0	995.7
608	S321	-1120.0	860.7
609	S320	-1148.0	995.7
610	S319	-1176.0	860.7
611	S318	-1204.0	995.7
612	S317	-1232.0	860.7
613	S316	-1260.0	995.7
614	S315	-1288.0	860.7
615	S314	-1316.0	995.7
616	S313	-1344.0	860.7
617	S312	-1372.0	995.7
618	S311	-1400.0	860.7
619	S310	-1428.0	995.7
620	S309	-1456.0	860.7
621	S308	-1484.0	995.7
622	S307	-1512.0	860.7
623	S306	-1540.0	995.7

624	S305	-1568.0	860.7
625	S304	-1596.0	995.7
626	S303	-1624.0	860.7
627	S302	-1652.0	995.7
628	S301	-1680.0	860.7
629	S300	-1708.0	995.7
630	S299	-1736.0	860.7
631	S298	-1764.0	995.7
632	S297	-1792.0	860.7
633	S296	-1820.0	995.7
634	S295	-1848.0	860.7
635	S294	-1876.0	995.7
636	S293	-1904.0	860.7
637	S292	-1932.0	995.7
638	S291	-1960.0	860.7
639	S290	-1988.0	995.7
640	S289	-2016.0	860.7
641	S288	-2044.0	995.7
642	S287	-2072.0	860.7
643	S286	-2100.0	995.7
644	S285	-2128.0	860.7
645	S284	-2156.0	995.7
646	S283	-2184.0	860.7
647	S282	-2212.0	995.7
648	S281	-2240.0	860.7
649	S280	-2268.0	995.7
650	S279	-2296.0	860.7
651	S278	-2324.0	995.7
652	S277	-2352.0	860.7
653	S276	-2380.0	995.7
654	S275	-2408.0	860.7
655	S274	-2436.0	995.7
656	S273	-2464.0	860.7
657	S272	-2492.0	995.7
658	S271	-2520.0	860.7
659	S270	-2548.0	995.7
660	S269	-2576.0	860.7
661	S268	-2604.0	995.7
662	S267	-2632.0	860.7
663	S266	-2660.0	995.7
664	S265	-2688.0	860.7
665	S264	-2716.0	995.7

666	S263	-2744.0	860.7
667	S262	-2772.0	995.7
668	S261	-2800.0	860.7
669	S260	-2828.0	995.7
670	S259	-2856.0	860.7
671	S258	-2884.0	995.7
672	S257	-2912.0	860.7
673	S256	-2940.0	995.7
674	S255	-2968.0	860.7
675	S254	-2996.0	995.7
676	S253	-3024.0	860.7
677	S252	-3052.0	995.7
678	S251	-3080.0	860.7
679	S250	-3108.0	995.7
680	S249	-3136.0	860.7
681	S248	-3164.0	995.7
682	S247	-3192.0	860.7
683	S246	-3220.0	995.7
684	S245	-3248.0	860.7
685	S244	-3276.0	995.7
686	S243	-3304.0	860.7
687	S242	-3332.0	995.7
688	S241	-3360.0	860.7
689	S240	-3388.0	995.7
690	S239	-3416.0	860.7
691	S238	-3444.0	995.7
692	S237	-3472.0	860.7
693	S236	-3500.0	995.7
694	S235	-3528.0	860.7
695	S234	-3556.0	995.7
696	S233	-3584.0	860.7
697	S232	-3612.0	995.7
698	S231	-3640.0	860.7
699	S230	-3668.0	995.7
700	S229	-3696.0	860.7
701	S228	-3724.0	995.7
702	S227	-3752.0	860.7
703	S226	-3780.0	995.7
704	S225	-3808.0	860.7
705	S224	-3836.0	995.7
706	S223	-3864.0	860.7
707	S222	-3892.0	995.7

708	S221	-3920.0	860.7
709	S220	-3948.0	995.7
710	S219	-3976.0	860.7
711	S218	-4004.0	995.7
712	S217	-4032.0	860.7
713	S216	-4060.0	995.7
714	S215	-4088.0	860.7
715	S214	-4116.0	995.7
716	S213	-4144.0	860.7
717	S212	-4172.0	995.7
718	S211	-4200.0	860.7
719	S210	-4228.0	995.7
720	S209	-4256.0	860.7
721	S208	-4284.0	995.7
722	S207	-4312.0	860.7
723	S206	-4340.0	995.7
724	S205	-4368.0	860.7
725	S204	-4396.0	995.7
726	S203	-4424.0	860.7
727	S202	-4452.0	995.7
728	S201	-4480.0	860.7
729	S200	-4508.0	995.7
730	S199	-4536.0	860.7
731	S198	-4564.0	995.7
732	S197	-4592.0	860.7
733	S196	-4620.0	995.7
734	S195	-4648.0	860.7
735	S194	-4676.0	995.7
736	S193	-4704.0	860.7
737	S192	-4732.0	995.7
738	S191	-4760.0	860.7
739	S190	-4788.0	995.7
740	S189	-4816.0	860.7
741	S188	-4844.0	995.7
742	S187	-4872.0	860.7
743	S186	-4900.0	995.7
744	S185	-4928.0	860.7
745	S184	-4956.0	995.7
746	S183	-4984.0	860.7
747	S182	-5012.0	995.7
748	S181	-5040.0	860.7
749	S180	-5068.0	995.7

750	S179	-5096.0	860.7
751	S178	-5124.0	995.7
752	S177	-5152.0	860.7
753	S176	-5180.0	995.7
754	S175	-5208.0	860.7
755	S174	-5236.0	995.7
756	S173	-5264.0	860.7
757	S172	-5292.0	995.7
758	S171	-5320.0	860.7
759	S170	-5348.0	995.7
760	S169	-5376.0	860.7
761	S168	-5404.0	995.7
762	S167	-5432.0	860.7
763	S166	-5460.0	995.7
764	S165	-5488.0	860.7
765	S164	-5516.0	995.7
766	S163	-5544.0	860.7
767	S162	-5572.0	995.7
768	S161	-5600.0	860.7
769	S160	-5628.0	995.7
770	S159	-5656.0	860.7
771	S158	-5684.0	995.7
772	S157	-5712.0	860.7
773	S156	-5740.0	995.7
774	S155	-5768.0	860.7
775	S154	-5796.0	995.7
776	S153	-5824.0	860.7
777	S152	-5852.0	995.7
778	S151	-5880.0	860.7
779	S150	-5908.0	995.7
780	S149	-5936.0	860.7
781	S148	-5964.0	995.7
782	S147	-5992.0	860.7
783	S146	-6020.0	995.7
784	S145	-6048.0	860.7
785	S144	-6076.0	995.7
786	S143	-6104.0	860.7
787	S142	-6132.0	995.7
788	S141	-6160.0	860.7
789	S140	-6188.0	995.7
790	S139	-6216.0	860.7
791	S138	-6244.0	995.7

792	S137	-6272.0	860.7
793	S136	-6300.0	995.7
794	S135	-6328.0	860.7
795	S134	-6356.0	995.7
796	S133	-6384.0	860.7
797	S132	-6412.0	995.7
798	S131	-6440.0	860.7
799	S130	-6468.0	995.7
800	S129	-6496.0	860.7
801	S128	-6524.0	995.7
802	S127	-6552.0	860.7
803	S126	-6580.0	995.7
804	S125	-6608.0	860.7
805	S124	-6636.0	995.7
806	S123	-6664.0	860.7
807	S122	-6692.0	995.7
808	S121	-6720.0	860.7
809	S120	-6748.0	995.7
810	S119	-6776.0	860.7
811	S118	-6804.0	995.7
812	S117	-6832.0	860.7
813	S116	-6860.0	995.7
814	S115	-6888.0	860.7
815	S114	-6916.0	995.7
816	S113	-6944.0	860.7
817	S112	-6972.0	995.7
818	S111	-7000.0	860.7
819	S110	-7028.0	995.7
820	S109	-7056.0	860.7
821	S108	-7084.0	995.7
822	S107	-7112.0	860.7
823	S106	-7140.0	995.7
824	S105	-7168.0	860.7
825	S104	-7196.0	995.7
826	S103	-7224.0	860.7
827	S102	-7252.0	995.7
828	S101	-7280.0	860.7
829	S100	-7308.0	995.7
830	S99	-7336.0	860.7
831	S98	-7364.0	995.7
832	S97	-7392.0	860.7
833	S96	-7420.0	995.7

834	S95	-7448.0	860.7
835	S94	-7476.0	995.7
836	S93	-7504.0	860.7
837	S92	-7532.0	995.7
838	S91	-7560.0	860.7
839	S90	-7588.0	995.7
840	S89	-7616.0	860.7
841	S88	-7644.0	995.7
842	S87	-7672.0	860.7
843	S86	-7700.0	995.7
844	S85	-7728.0	860.7
845	S84	-7756.0	995.7
846	S83	-7784.0	860.7
847	S82	-7812.0	995.7
848	S81	-7840.0	860.7
849	S80	-7868.0	995.7
850	S79	-7896.0	860.7
851	S78	-7924.0	995.7
852	S77	-7952.0	860.7
853	S76	-7980.0	995.7
854	S75	-8008.0	860.7
855	S74	-8036.0	995.7
856	S73	-8064.0	860.7
857	S72	-8092.0	995.7
858	S71	-8120.0	860.7
859	S70	-8148.0	995.7
860	S69	-8176.0	860.7
861	S68	-8204.0	995.7
862	S67	-8232.0	860.7
863	S66	-8260.0	995.7
864	S65	-8288.0	860.7
865	S64	-8316.0	995.7
866	S63	-8344.0	860.7
867	S62	-8372.0	995.7
868	S61	-8400.0	860.7
869	S60	-8428.0	995.7
870	S59	-8456.0	860.7
871	S58	-8484.0	995.7
872	S57	-8512.0	860.7
873	S56	-8540.0	995.7
874	S55	-8568.0	860.7
875	S54	-8596.0	995.7

876	S53	-8624.0	860.7
877	S52	-8652.0	995.7
878	S51	-8680.0	860.7
879	S50	-8708.0	995.7
880	S49	-8736.0	860.7
881	S48	-8764.0	995.7
882	S47	-8792.0	860.7
883	S46	-8820.0	995.7
884	S45	-8848.0	860.7
885	S44	-8876.0	995.7
886	S43	-8904.0	860.7
887	DUMMY23	-8932.0	995.7
888	DUMMY24	-8960.0	860.7
889	DUMMY25	-9295.8	641.8
890	DUMMY26	-9160.8	613.8
891	S42	-9295.8	585.8
892	S41	-9160.8	557.8
893	S40	-9295.8	529.8
894	S39	-9160.8	501.8
895	S38	-9295.8	473.8
896	S37	-9160.8	445.8
897	S36	-9295.8	417.8
898	S35	-9160.8	389.8
899	S34	-9295.8	361.8
900	S33	-9160.8	333.8
901	S32	-9295.8	305.8
902	S31	-9160.8	277.8
903	S30	-9295.8	249.8
904	S29	-9160.8	221.8
905	S28	-9295.8	193.8
906	S27	-9160.8	165.8
907	S26	-9295.8	137.8
908	S25	-9160.8	109.8
909	S24	-9295.8	81.8
910	S23	-9160.8	53.8
911	S22	-9295.8	25.8
912	S21	-9160.8	-2.2
913	S20	-9295.8	-30.2
914	S19	-9160.8	-58.2
915	S18	-9295.8	-86.2
916	S17	-9160.8	-114.2
917	S16	-9295.8	-142.2
918	S15	-9160.8	-170.2
919	S14	-9295.8	-198.2
920	S13	-9160.8	-226.2
921	S12	-9295.8	-254.2
922	S11	-9160.8	-282.2
923	S10	-9295.8	-310.2
924	S9	-9160.8	-338.2
925	S8	-9295.8	-366.2
926	S7	-9160.8	-394.2
927	S6	-9295.8	-422.2
928	S5	-9160.8	-450.2
929	S4	-9295.8	-478.2
930	S3	-9160.8	-506.2
931	S2	-9295.8	-534.2
932	S1	-9160.8	-562.2
933	DUMMY27	-9295.8	-590.2
934	DUMMY28	-9160.8	-618.2
935	DUMMY29	-9295.8	-646.2
936	DUMMY30	-9295.8	-702.2
937	DUMMY31	-9295.8	-758.2
938	DUMMY32	-9290.8	-990.7

BUMP Arrangement

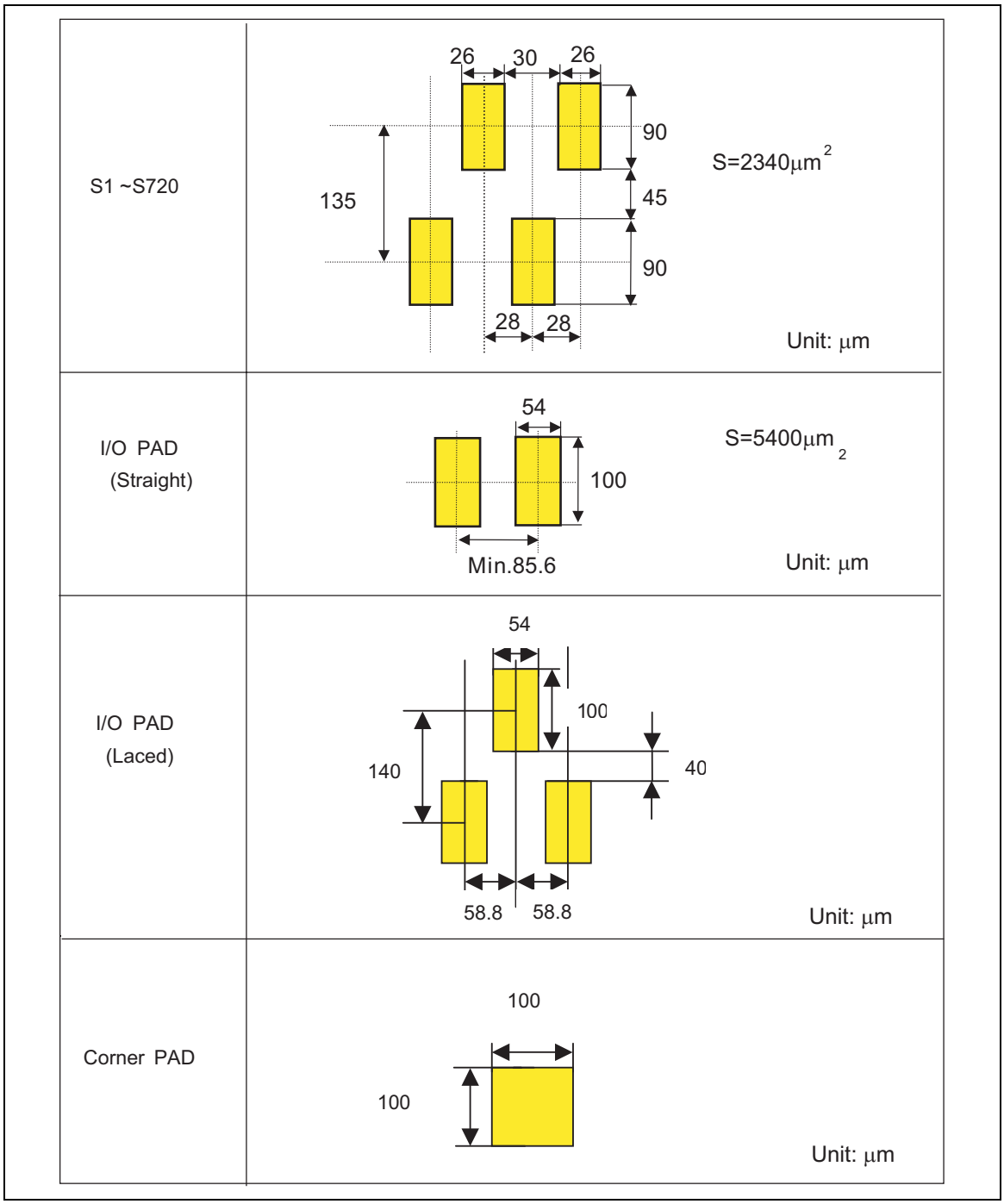
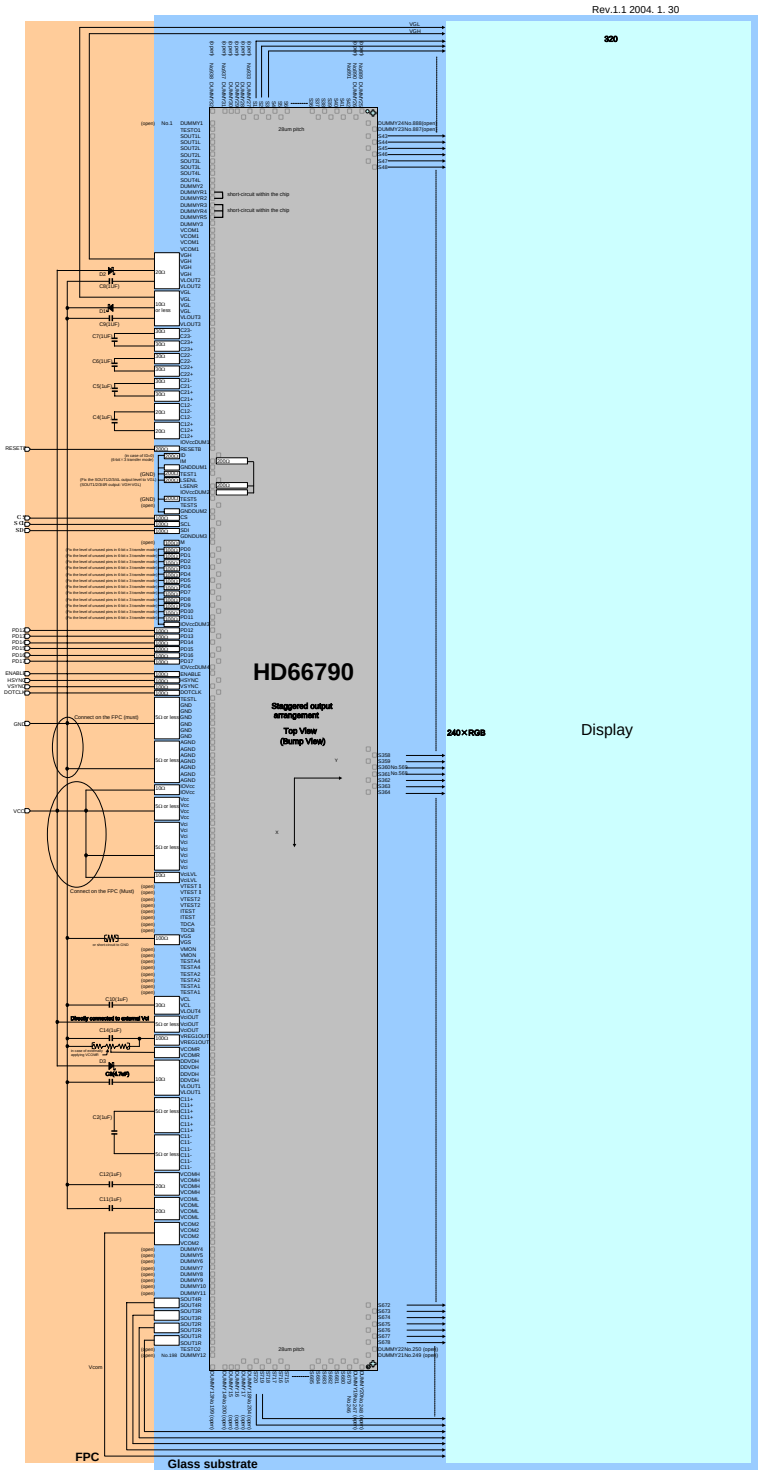


Figure 3

Wiring example



Pin function

Table 2 Power supply pins

Signals	I/O	Connected to	Function	Unused pins
Vcc	S	Power supply	Logic supply voltage	
IOVcc	S	Power supply	Interface supply voltage.	
GND	S	Power supply	Logic ground.	
Vci	S	Power supply	Analog supply voltage.	
AGND	S	Power supply	Analog ground.	

Table 3 DCDC converter pins

Signals	I/O	Connected to	Function	Unused pins
VciOUT	O	Vci1 or Vci	Outputs a reference voltage for the step-up circuits using Vci-GND as a reference level. The voltage level is set with VC2-0 bits. Connect a stabilizing capacitor when using. When not in use, leave it open.	
VciLVL	I	Power supply (Vci)	A reference supply voltage setting the maximum electrical potential of the ladder resistors used for generating the reference supply voltage. Use the Vci level in normal operation.	
VLOUT1	O	DDVDH	A supply voltage of twice the VciOUT level, output from the step-up circuit 1. Connect a stabilizing capacitor when in use.	
DDVDH	I	VLOUT1 or power supply	A supply voltage for source driver and Vcom drive. Connect to VLOUT1 when using the internal step-up circuit. When not using the internal step-up circuit, connect to an external power supply.	
VLOUT2	O	Stabilizing capacitor	A supply voltage of either 6/7/8 times the VciOUT level, output from the step-up circuit 2, when DDVDH=VciOUT x 2. The step-up factor is set with BT2-0 bits. Connect a stabilizing capacitor when using the VGH output.	
VGH	I	VLOUT2 or power supply	A supply voltage to drive the gate driver circuit incorporated in the TFT LCD panel.	
VLOUT3	O	Stabilizing capacitor	A supply voltage of either –5/-6/-7 times the VciOUT level, output from the step-up circuit 2, when DDVDH=VciOUT x 2. The step-up factor is set with BT2-0 bits. Connect a stabilizing capacitor when using the VGL output.	
VGL	I	VLOUT3 or power supply	A supply voltage to drive the gate driver circuit incorporated in the TFT LCD panel.	
VLOUT4	O	Stabilizing capacitor	A supply voltage of -1 times the VciOUT level, output from the step-up circuit 2. Connect a stabilizing capacitor when in use.	
VCL	I	VLOUT4 or power supply	A VcomL drive supply voltage.	
C11+, C11-	I/O	Step-up capacitor	Pins to connect a stabilizing capacitor for the step-up circuit 1.	Open
C12+, C12-	I/O	Step-up capacitor	Pins to connect a stabilizing capacitor for the step-up circuit 2.	Open
C21+, C21-	I/O	Step-up capacitor	Pins to connect a stabilizing capacitor for the step-up circuit 2.	Open
C22+, C22-	I/O	Step-up capacitor	Pins to connect a stabilizing capacitor for the step-up circuit 2.	Open
C23+, C23-	I/O	Step-up capacitor	Pins to connect a stabilizing capacitor for the step-up circuit 2.	Open

Table 4 Common electrode output and control pins

Signals	I/O	Connected to	Function	Unused pins
VREG1OUT	O	Stabilizing capacitor	A voltage level generated from the internal reference voltage REGP. The REGP is generated internally by multiplying the Vci-GND level by a factor 1.27 ~ 1.92 and has the same electrical potential as VciOUT. The step-up factor is set with VRH bits. VREG1OUT serves as (1) source driver grayscale reference level VDH, (2) VcomH reference level, (3) Vcom width reference level. Connect a stabilizing capacitor in use. When not in use, leave it open.	Open
VCOM1, VCOM2	O	TFT panel common electrode	Output the Vcom level to the TFT panel common electrode. Both VCOM1 and VCOM2 output the same signal. VCOM1 and VCOM2 are arranged on the left and right sides of the chip respectively for convenience of arrangement. Use either one of them.	
VcomH	O	Stabilizing capacitor	The Vcom high level. The output voltage level is adjusted with VCM bits.	
VcomL	O	Stabilizing capacitor or open	The Vcom low level. The amplitude is set using VcomH as a reference by multiplying a factor with DVD bits. When VCOMG is set to 0, the output from VcomL halts. In this case, a capacitor connection is not required.	
VcomR	I	Variable resistor	Used when adjusting VcomH with variable resistors. When using VcomR, halt the VcomH internal adjusting circuit by instruction (VCM bits) and connect a variable resistor between VREG1OUT and GND. When not using VcomR (not adjusting Vcom externally), leave VcomR open, and adjust the Vcom level with VCM bits.	Open

Table 5 Source driver output and control pins

Signals	I/O	Connected to	Function	Unused pins
S1~ S720	O	LCD	Source signals to output voltages applied to the LCD. The shift direction of outputting signals from S1-720 pins is changeable by setting the SHL pin.	

Table 6 Source driver power supply pin

Signals	I/O	Connected to	Function	Unused pins
VGS	S	GND or resistor	The low side supply voltage to the source driver.	

Grayscale level monitor pins

Signals	I/O	Connected to	Function	Unused pins
VMON	I/O	OPEN	A grayscale level monitor pin. Do not use this pin. Disconnect it.	
RESETB	I	MPU or external RC circuits	A reset pin. The HD66790 is initialized with a low RESET input. Be sure to execute a power-on reset after turning on power supply.	
VSYNC	I	LCTC	A frame synchronizing signal. The effective polarity of the signal is set with the VPL bit.	
HSYNC	I	LCTC	A line synchronizing signal. The effective polarity of the signal is set with the HPL bit.	
DOTCLK	I	LCTC	A DOTCLK signal. The effective polarity of the signal is set with the DPL bit	
ENABLE	I	LCTC	A data ENABLE signal The effective polarity of the signal is set with the EPL bit.	
PD17-0	I	LCTC	A data bus to input display data in units of 18 bits (6 bits (grayscale) x 3 dots (RGB)).	GND or Vcc
IM	I	GND or Vcc	An RGB interface modes switching pin. If IM = “L”: input RGB dots at a time via 18-bit RGB interface mode. If IM = “H”: input one dot (6 bits) at a time via 6-bit inter face mode (input RGB dots by 3 transmissions).	

Register control interface pins

Signals	I/O	Connected to	Function	Unused pins
ID	I	GND or Vcc	A chip ID setting pin for Serial Peripheral Interface mode.	
CS	I	MPU	A chip select signal for Serial Peripheral Interface mode. If CS = “L”: select the HD66790 (accessible). If CS = “H”: not select the HD66790 (inaccessible)	Fix to Vcc
SCL	I	MPU	A synchronizing clock signal for Serial Peripheral Interface mode.	Fix to Vcc
SDI	I	MPU	A serial data input pins for Serial Peripheral Interface mode. Data are input on the rising edge of SCL signal.	Fix to Vcc

Gate driver control signal function setting pins

Signals	I/O	Connected to	Function	Unused pins
LSENR	I	GND or Vcc	A level shifter output ENABLE signal. If LSENR = “H”: enable the level shifter outputs from SOUT1/2/3/4R If LSENR = “L”: output the VGL level from SOUT1/2/3/4R In consideration of current consumption increase and voltage drop, set LSENL = “L” if LSENR =”H”.	-
LSENL	I	GND or Vcc	A level shifter output ENABLE signal. If LSENL = “H”: enable the level shifter outputs from SOUT1/2/3/4L. If LSENL = “L”: output the VGL level from SOUT1/2/3/4L. In consideration of current consumption increase and voltage drop, set LSENR = “L” if LSENL =”H”.	-

Gate driver control signal within level shifter

Signals	I/O	Connected to	Function	Unused pins
SOUT1R SOUT1L	O		A frame pulse signal for the LCD (the level shifter output, operating at voltage amplitude of VGH-VGL).	Open
SOUT2R SOUT2L	O		A line cycle clock signal for the LCD (the level shifter output, operating at voltage amplitude of VGH-VGL).	Open
SOUT3R SOUT3L	O		A signal for the LCD (the level shifter output, operating at voltage amplitude of VGH-VGL).	Open
SOUT4R SOUT4L	O		A signal for the LCD (the level shifter output, operating at voltage amplitude of VGH-VGL).	Open

Gate driver control signal for logic level

Signals	I/O	Connected to	Function	Unused pins
M	O		An alternating cycle clock signal (logic level output).	Open

TEST pins

Signals	I/O	Connected to	Function	Unused pins
TESTO1	O	Open	A monitor pin for S1.	
TESTO2	O	Open	A monitor pin for S720.	
TEST1	I	GND	A logic test pin.	
TEST5	I	GND	A logic test pin.	
TESTS	O	Open	A logic test pin.	
VTEST1	O	Open	An analog test pin.	
VTEST2	O	Open	An analog test pin.	
ITEST	O	Open	An analog test pin.	
TDCA	O	Open	An analog test pin.	
TDCB	O	Open	An analog test pin.	
TESTA1	O	Open	An analog test pin.	
TESTA2	O	Open	An analog test pin.	
TESTA4	O	Stabilizing capacitor	An analog test pin.	
TESTL	I	GND	An analog test pin.	

Dummy pins

Signals	I/O	Connected to	Function	Unused pins
DUMMY 1 ~ 15	-	Open	Disconnected these pins.	
DUMMYR	I/O		Dummy pads. DUMMYR can also be used for measuring COG contact resistance.	
VccDUM 1 ~ 4	O		Pins to fix the high level. Use them to fix the level of mode pins.	
GNDDUM 1 ~ 3	O		Pins to fix the low level. Use them to fix the level of mode pins.	

Patents of dummy pin which is used to fix pin to VCC or GND are pending and granted.

PATENT ISSUED: United States Patent No. 6,323,930
PATENT PENDING: Japanese Application No. 10-514484
Korean Application No. 19997002322
Taiwanese Application No.086103756
(PCT/JP96/02728(W098/12597)

Instruction

The HD66790 supports an interface to a microcomputer, enabling high-quality display and low power consumption drive by setting instruction. See “Serial Peripheral Interface (SPI)”for details on setting, timing and so on.

Index: IR

RS1	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	0	0	0	0	ID4	ID3	ID2	ID1	ID0
Default	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0

Specifies the index registor to access. Do not try to access to a register to which instruction is not assigned.

Power Color 1: R01h

RS1	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	DC 12	DC 11	DC 10	GON	0	BT2	BT1	BT0	DC 02	DC 01	DC 00	AP2	AP1	AP0	SLP
Default	-	0	0	0	0	-	1	1	1	0	0	0	0	0	0	0

SLP: Sets sleep mode. Upon setting SLP = “1”, the HD66790 is in the same state as it is when AP[2:0] = “000”, in which the operation of power circuits (DCDC step-up circuits) are halted but the operation of source amplifiers and other circuits are not affected. This does not mean the AP[2:0] bits are overwritten to “000”. The setting is enabled at the next VSYNC assert timing.

AP[2:0]: Adjusts the constant current from the constant current source in the internal operational amplifier circuit. A higher constant current will stabilize the operational amplifier circuit. Adjust the constant current taking the trade-off between the stability of the grayscale level and current consumption into account. In cases like sleep and standby modes when there needs no display on the screen, set AP[2:0] = “000” to halt operational amplifiers to reduce power consumption. If AP[2:0] is set to other than “000”, the step-up circuits 1 and 2 output the VLOUT1 and VLOUT2 level respectively.

Table 7

AP2	AP1	AP0	Constant current in operational amplifiers	
0	0	0	Halt operations of operational amplifier and step-up circuits	(Default)
0	0	1	0.5	
0	1	0	0.75	
0	1	1	1	
1	0	0	1.25	
1	0	1	1.5	
1	1	0	Setting disabled	
1	1	1	Setting disabled	

Note: The values in this table are the ratios against the constant current when AP[2:0] is set to “011”.

DC0[2:0]: Set the operating frequency of the step-up circuit 1. A higher frequency increases current consumption. Set the optimum frequency taking display quality, power consumption, and power supply startup characteristics in high temperatures into consideration. The DDVDH load fluctuation becomes smaller at a higher step-up frequency. The operating frequency of the step-up circuit 2 is set independently with the DC1[2:0] bits.

Table 8

DC 02	DC 01	DC 00	Step-up circuit 1 Step-up clock frequency	
0	0	0	DOTCLK / 32	(Default)
0	0	1	DOTCLK / 64	
0	1	0	DOTCLK / 128	
0	1	1	DOTCLK / 256	
1	0	0	DOTCLK / 512	
1	0	1	Setting disabled	
1	1	0	DOTCLK / 16	
1	1	1	Setting disabled	

BT[2:0]: Set an optimum step-up factor for the power supply voltage in use.

Table 9

VLOUT1 output: Vci1 x 2 (fixed whatever the setting of BT[2:0])

BT2	BT1	BT0	VLOUT1 output	Capacitor connection pins
*	*	*	Vci1 x 2	VLOUT1, C11±

VLOUT2, VLOUT3 outputs:

BT2	BT1	BT0	VLOUT2	VLOUT3	Capacitor connection pins	
0	0	0	DDVDH x 4 [x 8]	– (VciOUT + DDVDH x 3) [x –7]	VLOUT2, VLOUT3, C12±, C21±, C22±	
0	0	1		– (DDVDH x 3) [x –6]	VLOUT2, VLOUT3, C21±, C22±	
0	1	0		– (VciOUT + DDVDH x 2) [x –5]	VLOUT2, VLOUT3, C12±, C21±, C22±	
0	1	1	VciOUT+DDVDHx3 [x 7]	– (VciOUT + DDVDH x 3) [x –7]	VLOUT2, VLOUT3, C12±, C21±, C22±	
1	0	0		– (DDVDH x 3) [x –6]	VLOUT2, VLOUT3, C21±, C22±	
1	0	1		– (VciOUT + DDVDH x 2) [x –5]	VLOUT2, VLOUT3, C12±, C21±, C22±	
1	1	0	DDVDH x 3 [x 6]	– (DDVDH x 3) [x –6]	VLOUT2, VLOUT3, C21±, C22±	
1	1	1		– (VciOUT + DDVDH x 2) [x –5]	VLOUT2, VLOUT3, C12±, C21±	(Default)

Note 1) The step-up factors in the brackets are the ratio against VciOUT, which is obtained by short-circuiting VLOUT1 and DDVDH.

Note 2) when using the VLOUT output 1/2/3/4 pins, connect capacitors to the pins where required.

GON: Sets the Vcom output. When GON = "0", the Vcom output becomes GND.

DC1[2:0]: Set the operating frequency of the step-up circuit 2. A higher frequency increases current consumption. Set the optimum frequency taking display quality, power consumption, and power supply startup characteristics in high temperatures into consideration. The operating frequency of the step-up circuit 1 is set independently with the DC0[2:0] bits.

Table 10

DC 12	DC 11	DC 10	Step-up circuit 2 Step-up clock frequency	
0	0	0	DOTCLK / 64	(Default)
0	0	1	DOTCLK / 128	
0	1	0	DOTCLK / 256	
0	1	1	DOTCLK / 512	
1	0	0	DOTCLK / 1024	
1	0	1	DOTCLK / 2048	
1	1	0	DOTCLK / 4096	
1	1	1	Setting disabled	

Note: The HD66790 use a charge pump method (DCDC) to generate supply voltages. There are cases that DDVDH voltage fluctuation (ripple) occurs in synchronization with the divided DOTCLK frequency set with the DC0 bits when the power supply load is high. A high DDVDH voltage fluctuation will trigger the fluctuation of source voltages synchronously, which will appear as the unevenness of grayscales in the gate line direction. Also, the DDVDH voltage fluctuation is likely to occur with a high VCOM voltage load on the panel in synchronization with the VCOM operation, which also has something to do with the fluctuation of source voltage.

To restrain the DDVDH voltage fluctuation, connect multiple stabilizing capacitors of 1uF to DDVDH in parallel to secure enough capacitance for DDVDH. Also, the electrical load on the panel should be made as small as possible. The current consumption and the power supply load can be reduced by functions to halt source amplifiers (EQE, SDC, SDT bits), equalize the source and Vcom levels (EQE, SDT bits), and adjust the source amplifier bias current (TMB bit). The optimum setting of these bits depends on the characteristics of the panel.

The HD66790 starts the step-up operation in synchronization with the divided DOTCLK. The optimum division ratios for the step-up clock frequencies set with the DC0[2:0] and DC1 [2:0] bits depend on the DOTCLK frequency. The recommended range for the step-up clock DCDC1 is from 20KHz to 100KHz and that for DCDC2 is from 5KHz to 25KHz. Also be sure to set the division ratio of DCDC1 is smaller than that of DCDC2. Although the HD66790 can operate with the frequencies not within these ranges, a higher step-up clock frequency increases current consumption and lower the output voltage level. Check the display quality to set these bits optimally. In case of using a DCDC operating frequency not within the recommended range, remember the following points when executing the power supply startup sequence (see “Power Supply Setting”, p.74). In this case, because the startup of the VGH and VGL levels after setting AP[2:0] bits in the “issuing power supply setting instruction (1)” stage is delayed, the relative relationship between the electrical potential of DDVDH and that of VGH is inverted and the power supply startup will fail. To avoid this, spread the interval between the “issuing power supply setting instruction (1)” stage and the “issuing power supply setting instruction (2)”.

In general, the voltage fluctuation synchronizing with the DCDC frequency can be mitigated by raising the step-up clock frequency, i.e. by setting a smaller division ratio with DC0/DC1 bits for dividing the DOTCLK frequency. However a higher DCDC frequency that contributes to mitigating the DDVDH voltage fluctuation due to the DCDC frequency sacrifices the efficiency and is likely to cause the DDVDH output voltage drop. In case of fDOTCLK = 5MHz, the division ratio which will minimize the output impedance is from 1/128 to 1/256.

The kind of unwanted horizontal line appearing on the screen with some division ratios has something to do with the step-up cycle DCDC, which is set by dividing the DOTCLK by the division ratio. For example, when selecting the division ratio 1/64, the charge pump cycle is 64 DOTCLKs per cycle, and in synchronization with this cycle, the DDVDH ripple occur. The DDVDH ripple then fluctuate the source output voltage, which appears as the uneven grayscale on the screen in the gate line direction. Here, assume the sum of the horizontal back and front porch periods (HBP+HFP) is 32 DOTCLKs, instead of 16 DOTCLKs. In this case, the number of DOTCLK in one horizontal (1H) period becomes 272 (=240+32) DOTCLKs. Since the number of DOTCLK in 1H period (272) is not divisible by 64, the remainder will cause shifting voltage leves from one line to another line. This is the exact cause of the moving horizontal line in the gate line direction on the screen. Therefore, by setting the number of DOTCLK in the back and front porch periods so that the total number of DOTCLK in 1H period becomes 256 (the least common multiple of 32, 64, 128, 256), this problem will be eliminated when the division ratio of DCDC1 is from 1/16 to 1/256.

In case the division ratio of DCDC1 is 1/512, set the number of DOTCLK 256 per 1H period and set the number of vertical lines (effective lines+VBP+VFP) to an odd number. In this case, one charge pump cycle lasts for 2 line periods. If the number of vertical line is even, the shift in voltage levels from one line to another is just repeated in the same manner. As a result, fixed lines in the gate line direction appear on the screen every other line. However, if the number of vertical lines is odd, the remainder one vertical line generates a time lag in the above mentioned repetition, and due to different voltage levels at each vertical line in 2 frame periods, the voltage fluctuation is mitigated. As a result, the fixed line in the gate line direction on the screen becomes obscure.

The following are examples of setting. In 18-bit interface mode, set the division ratios for DCDC1 and DCDC2 1/128, 1/512 respectively if DOTCLK = 5MHz. The number of DOTCLK in 1H period should be 256 DOTCLKs. In 6-bit interface mode, the frequency of DOTCLK becomes three times higher in the same frame cycle. In this case, DOTCLK = 15MHz, and the recommended combination of division ratios for DCDC1 and DCDC2 are either 1/512, 1/2048 or 1/256, 1/1024. Even when the division ratio for DCDC1 is set 1/32 to obtain fair quality of display, it is recommended to set as high a division ratio as possible for DCDC2 (lower step-up clock frequency).

Voltage setup 1 : R01h

RS1	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	DK	0	POC	0	PON	VRH 3	VRH 2	VRH 1	VRH 0	VC2	VC1	VC0
Default	-	-	-	-	1	-	0	-	0	0	0	0	0	0	0	0

VC[2:0]: Generate the VciOUT output and the VREG1OUT input level using VciLVL as a reference. The step-up factor and the VC[2:0] bits are as follows. Set VC[2:0] to “000” when directly inputting the Vci level externally.

Table 11

VC2	VC1	VC0	VciOUT voltage (REGP)	
0	0	0	VciLVL	(Default)
0	0	1	0.92 x VciLVL	
0	1	0	0.90 x VciLVL	
0	1	1	0.87 x VciLVL	
1	0	0	0.85 x VciLVL	
1	0	1	0.83 x VciLVL	
1	1	0	0.73 x VciLVL	
1	1	1	Setting disabled	

POC: Control the power control mode.

Table 12

POC	Power control mode	
0	Power control mode. A white display is shown on full screen	(Default)
1	Normal operation mode. All I/O interfaces are operable.	

Note 1) See “Power control” for details.
Note 2) The setting of POC is enabled at the next VSYNC assert timing.

PON: Controls ON and OFF of VLOUT3 output.

Table 13

PON	VLOUT3	
0	OFF	(Default)
1	ON	

DK: Controls DDVDH.

Table 14

DK	Function	
0	Startup DDVDH simultaneously with VGH. Startup the step-up circuit 1 (VLOUT1 output) according to the setting in the register (AP[2:0]) bits.	
1	Halt the step-up circuit 1 (VLOUT1).	(Default)

VRH[3:0]: Sets the amplifiying factor of REGP, the VciOUT voltage amplified by the factor set with the VC[2:0] bits, to generate VREG1OUT. The factor ranges from 1.27 to 1.92.

Table 15

VRH3	VRH2	VRH1	VRH0	VREG1OUT voltage
0	0	0	0	1.27 x REGP (Defarult)
0	0	0	1	1.32 x REGP
0	0	1	0	1.37 x REGP
0	0	1	1	1.42 x REGP
0	1	0	0	1.47 x REGP
0	1	0	1	1.52 x REGP
0	1	1	0	1.57 x REGP
0	1	1	1	Halt
1	0	0	0	1.62 x REGP
1	0	0	1	1.67 x REGP
1	0	1	0	1.72 x REGP
1	0	1	1	1.77 x REGP
1	1	0	0	1.82 x REGP
1	1	0	1	1.87 x REGP
1	1	1	0	1.92 x REGP
1	1	1	1	Halt

Voltage setup 2: R02h

RS1	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	VCOMG	VDV4	VDV3	VDV2	VDV1	VDV0	0	0	0	VCM4	VCM3	VCM2	VCM1	VCM0
Default	-	-	0	0	0	0	0	0	-	-	-	0	0	0	0	0

VCOMG: When VCOMG = “1”, the VcomL output voltage level can be set by instruction according to the VDV[4:0]bits. VCOMG = “1” is enabled when PON = “1”. When VCOMG = “0”, the VcomL output is fixed to the GND level and the VDV[4:0] bits is disenabled. In this case, the VcomL supply voltage VLOUT4 is halted. Since the VCOMG bit is depended on by the power supply start up sequence, set the VCOMG bit according to the power supply startup sequence.

VCM[4:0]: Set the amplyfying factor of the VREG1OUT to generate the VcomH voltage level (the high level of the Vcom voltage) from 0.41 to 1.00. The VcomH adjustment using internal volume is halted by setting VCM[4:0] = "11111" and the VcomH level can be adjusted using an external resistor connected to the VcomR.

Table 16

VCM4	VCM3	VCM2	VCM1	VCM0	VcomH voltage		
0	0	0	0	0	VREG1 x 0.41	24/60R	(Default)
0	0	0	0	1	VREG1 x 0.43	26/60R	
0	0	0	1	0	VREG1 x 0.45	27/60R	
0	0	0	1	1	VREG1 x 0.47	28/60R	
0	0	1	0	0	VREG1 x 0.49	29/60R	
0	0	1	0	1	VREG1 x 0.51	30/60R	
0	0	1	1	0	VREG1 x 0.53	32/60R	
0	0	1	1	1	VREG1 x 0.55	33/60R	
0	1	0	0	0	VREG1 x 0.57	34/60R	
0	1	0	0	1	VREG1 x 0.59	35/60R	
0	1	0	1	0	VREG1 x 0.61	36/60R	
0	1	0	1	1	VREG1 x 0.63	38/60R	
0	1	1	0	0	VREG1 x 0.65	39/60R	
0	1	1	0	1	VREG1 x 0.67	40/60R	
0	1	1	1	0	VREG1 x 0.69	41/60R	
0	1	1	1	1	Setting disabled		
1	0	0	0	0	VREG1 x 0.71	42/60R	
1	0	0	0	1	VREG1 x 0.73	43/40R	
1	0	0	1	0	VREG1 x 0.75	44/60R	
1	0	0	1	1	VREG1 x 0.77	45/60R	
1	0	1	0	0	VREG1 x 0.79	47/60R	
1	0	1	0	1	VREG1 x 0.81	48/60R	
1	0	1	1	0	VREG1 x 0.83	50/60R	
1	0	1	1	1	VREG1 x 0.85	51/60R	
1	1	0	0	0	VREG1 x 0.87	52/60R	
1	1	0	0	1	VREG1 x 0.89	54/60R	
1	1	0	1	0	VREG1 x 0.91	55/60R	
1	1	0	1	1	VREG1 x 0.93	56/60R	
1	1	1	0	0	VREG1 x 0.95	57/60R	
1	1	1	0	1	VREG1 x 0.97	58/60R	
1	1	1	1	0	VREG1 x 1.00	60/60R	
1	1	1	1	1	Disenables internal volume adjustment and enables external resistor adjustment		

VDV[4:0]: Set the factor of VREG1OUT to set the amplitude of Vcom AC voltage defined by VcomH and VcomL from 0.6 to1.48. When VCOMG = "0", the VDV[40] is disenabled.

Table 17

VDV4	VDV3	VDV2	VDV1	VDV0	Vcom amplitude	
0	0	0	0	0	VREG1OUT x 0.60	36/60R (Default)
0	0	0	0	1	VREG1OUT x 0.63	38/60R
0	0	0	1	0	VREG1OUT x 0.66	40/60R
0	0	0	1	1	VREG1OUT x 0.70	42/60R
0	0	1	0	0	VREG1OUT x 0.73	44/60R
0	0	1	0	1	VREG1OUT x 0.77	46/60R
0	0	1	1	0	VREG1OUT x 0.80	48/60R
0	0	1	1	1	VREG1OUT x 0.83	50/60R
0	1	0	0	0	VREG1OUT x 0.87	52/60R
0	1	0	0	1	VREG1OUT x 0.90	54/60R
0	1	0	1	0	VREG1OUT x 0.93	56/60R
0	1	0	1	1	VREG1OUT x 0.97	58/60R
0	1	1	0	0	VREG1OUT x 1.00	60/60R
0	1	1	0	1	VREG1OUT x 1.03	62/60R
0	1	1	1	0	Setting disabled	
0	1	1	1	1	Setting disabled	
1	0	0	0	0	VREG1OUT x 1.05	63/60R
1	0	0	0	1	VREG1OUT x 1.08	65/40R
1	0	0	1	0	VREG1OUT x 1.12	67/60R
1	0	0	1	1	VREG1OUT x 1.15	69/60R
1	0	1	0	0	VREG1OUT x 1.18	71/60R
1	0	1	0	1	VREG1OUT x 1.22	73/60R
1	0	1	1	0	VREG1OUT x 1.25	75/60R
1	0	1	1	1	VREG1OUT x 1.28	77/60R
1	1	0	0	0	VREG1OUT x 1.32	79/60R
1	1	0	0	1	VREG1OUT x 1.35	81/60R
1	1	0	1	0	VREG1OUT x 1.38	83/60R
1	1	0	1	1	VREG1OUT x 1.42	85/60R
1	1	1	0	0	VREG1OUT x 1.45	87/60R
1	1	1	0	1	VREG1OUT x 1.48	89/60R
1	1	1	1	0	Setting disabled	
1	1	1	1	1	Setting disabled	

Driver output control: R03h

RS1	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	VPL	HPL	DPL	EPL	0	0	SHL	0	0	0	0	SDT 1	SDT 0	0	0
Default	-	0	0	0	0	-	-	0	-	-	-	-	0	0	-	-

SDT[1:0]: Set the source output delay time. Set an optimum delay time for the characteristics of the panel when using the source-Vcom equalizing function and the source amplifier halt function.

Table 18

SDT1	SDT0	Delay	Source output delay time		
			18-bit RGB I/F (5MHz)	6-bit RGB I/F (16MHz)	
0	0	10 DOTCLK	2.0 μS	1.8750 μS	(Default)
0	1	40 DOTCLK	8.0 μS	7.5 μS	
1	0	80 DOTCLK	16.0 μS	15.0 μS	
1	1	120 DOTCLK	524 μS	22.5 μS	

Note: the actual delay time changes depending on the DOTCLK frequency.

SHL: Set the shift direction of outputting source signals.

Table 19

SHL	Shift direction	
0	(S1, S2, S3) → (S718, S719, S720)	(Default)
1	(S718, S719, S720) → (S1, S2, S3)	

EPL: Set the signal polarity of ENABLE pin when taking in data.

Table 20

EPL	Porality	
0	If ENABLE = “L”, enables data write operation. If ENABLE = “H”, disenables data write operation.	(Default)
1	If ENABLE = “H”, enables data write operation. If ENABLE = “L”, disenables data write operation.	

DPL: Set the signal polarity of DOTCLK pin.

Table 21

DPL	Porality	
0	Take in data on the falling edge of DOTCLK.	(Default)
1	Take in data on the rising edge of DOTCLK.	

HPL: Set the signal polarity of HSYNC pin.

Table 22

HPL	Porality	
0	Low active.	(Default)
1	High active	

VPL: Sets the signal polarity of VSYNC pin.

Table 23

VPL	Porality	
0	Low active.	(Default)
1	High active	

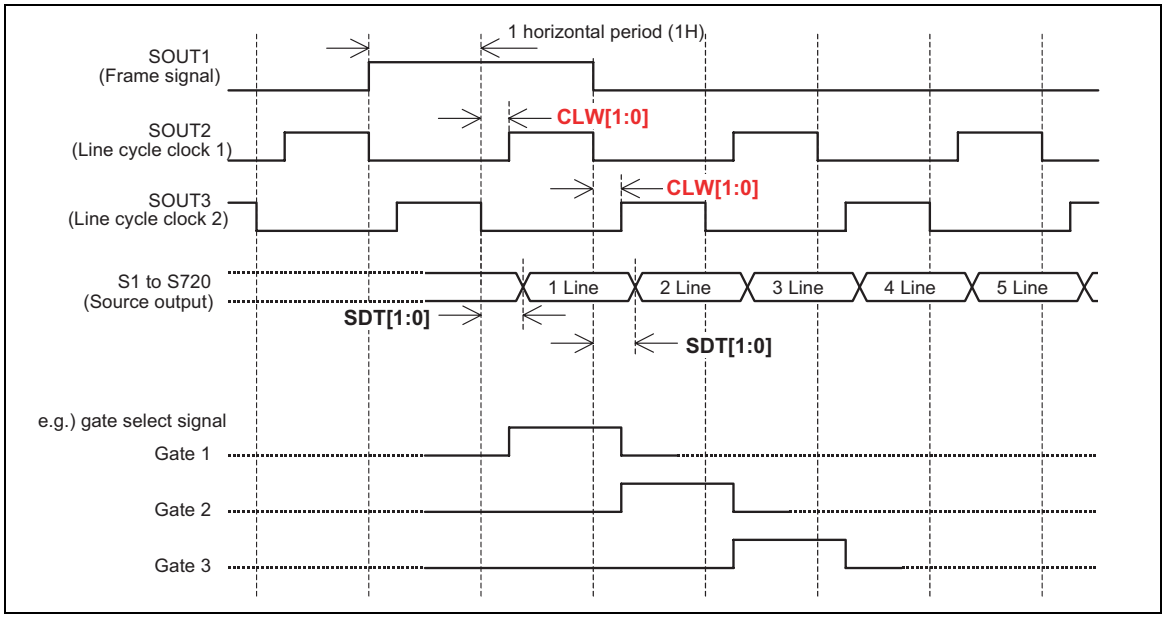


Figure 4

LCD driving waveform control, Source output control: R04h

RS1	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	0	NW 1	NW 0	0	0	0	0	BP3	BP2	BP1	BP0
Default	-	-	-	-	-	-	0	1	-	-	-	-	0	0	1	0

NW[1:0]: Selects the alternating cycle of the VcomH level and the VcomL level to invert polarity. For details, see "LCD AC drive". The setting of NW[1:0] bits is enabled at the next VSYNC assert timing.

Table 24

NW1	NW0	alternating cycle	
0	0	Every frame	
0	1	Every line	(Default)
1	0	Every 2 lines	
1	1	Setting disabled	

BP[3:0]: Sets the blank period (back porch) in the following figure by the line periods. The back porch period should be 14-line period ≥ back porch period ≥ 2-line period. The front porch period starts after the end of the display data transfer and continues until the next VSYNC assert timing. The setting of theBP[3:0] bits is enabled at the next assert timing

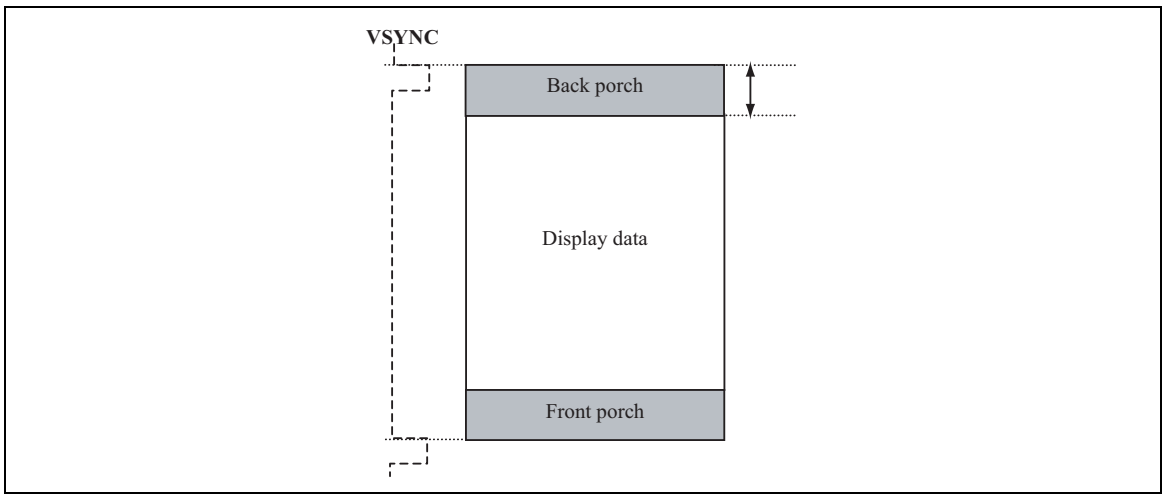


Figure 5

Table 25

BP3	BP2	BP1	BP0	Back porch line period	
0	0	0	0	Setting disabled	
0	0	0	1	Setting disabled	
0	0	1	0	2 line period	(Default)
0	0	1	1	3 line period	
0	1	0	0	4 line period	
0	1	0	0	5 line period	
0	1	1	1	6 line period	
0	1	1	0	7 line period	
1	0	0	0	8 line period	
1	0	0	1	9 line period	
1	0	1	0	10 line period	
1	0	1	1	11 line period	
1	1	0	0	12 line period	
1	1	0	1	13 line period	
1	1	1	0	14 line period	
1	1	1	1	Setting disabled	

Gate output control: R05h

RS1	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	CLW 1	CLW 0	0	0	NO 1	NO 0	0	0	GA ON	DTE	0	RE V	0	0
Default	-	-	0	0	-	-	0	0	-	-	0	0	-	0	-	-

REV: The correspondence between the grayscales and the output voltage levels can be inverted with the REV bit as follows. The setting of the REV bit is enabled at the next VSYNC assert timing.

Table 26

REV	Grayscale level	Source output grayscale voltage		
		Positive porality	Negative porality	
0	000000b[0] 111111b[63]	V0 V63	V63 V0	(Default)
1	000000b[0] 111111b[63]	V63 V0	V0 V63	

DTE: Output a gate off signal. The setting is enabled at the next VSYNC assert timing.

Table 27

DTE	Gate off signal	
0	Halt	(Default)
1	Output	

GAON: Set the level of the gate all ON signal. See "LCD display signal control" for details on selection of output pins. The setting is enabled at the next VSYNC assert timing.

Table 28

GAON	Gate off signal	
0	Gate output signal: SOUT3, SOUT4="0"	(Default)
1	Gate output signal: SOUT3, SOUT4="1"	

NO[1:0]: Set the non-overlap period of gate off signals. The non-overlap time depends on the DOTCLK frequency.

Table 29

NO1	NO0	Delay	non-overlap period: Delay period when 5MHz		
			18-bit RGB I/F (5MHz)	6-bit RGB I/F (16MHz)	
0	0	0 DOTCLK	0.0 μs	0.0000 μs	(Default)
0	1	20 DOTCLK	4.0 μs	3.7500 μs	
1	0	30 DOTCLK	6.0 μs	5.6250 μs	
1	1	40 DOTCLK	8.0 μs	7.5000 μs	

CLW[1:0]: Sets the output timing of display line cycle clocks (SOUT2, 3). The delay period changes according to the DOTCLK frequency.

Table 30

CLW 1	CLW 0	Delay	non-overlap period: Delay period when 5MHz		
			18-bit RGB I/F (5MHz)	6-bit RGB I/F (16MHz)	
0	0	0 DOTCLK	0.0 μs	0.0000 μs	(Default)
0	1	10 DOTCLK	2.0 μs	1.8750 μs	
1	0	20 DOTCLK	4.0 μs	3.6250 μs	
1	1	30 DOTCLK	6.0 μs	4.6875 μs	

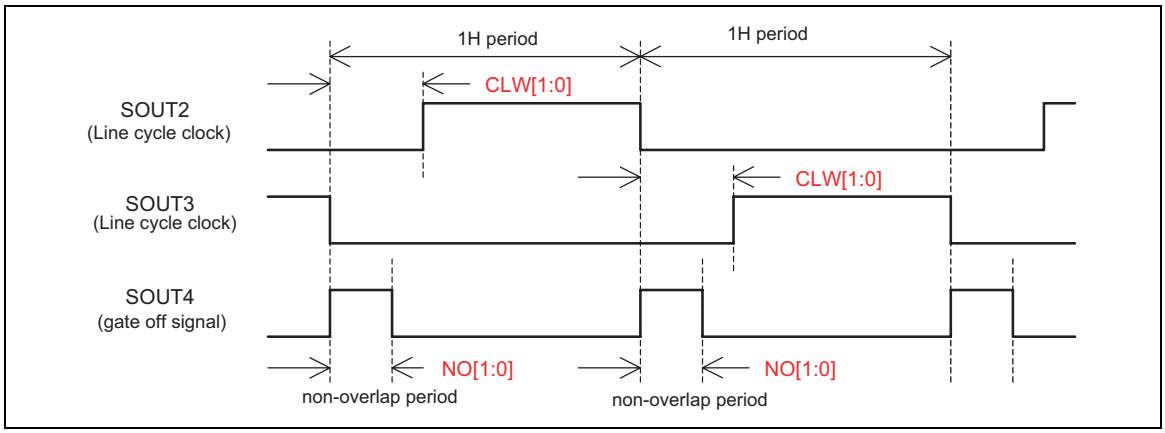


Figure 6

Display signal select control, frame control 1: R06h

RS1	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	DSC	0	0	GIF1	GIF0	FHN	0	FIT1	FIT0	0	0	FWI1	FWI0
Default	-	-	-	1	-	-	0	0	1	-	1	0	-	-	1	1

FWI[1:0]: Set the high width of the SOUT1 signal (frame timing signal). The time for high width period depends on the DOTCLK frequency. The setting of the FWI[1:0] bits is enabled from the next VSYNC assert timing.

Table 31

FWI1	FWI0	High width period	Time for the high width period when 5MHz	
			18-bit RGB I/F (5MHz)	6-bit RGB I/F (16MHz)
0	0	10 DOTCLK	2.0 μs	1.8750 μs
0	1	40 DOTCLK	8.0 μs	7.5000 μs
1	0	80 DOTCLK	17.0 μs	15.000 μs
1	1	Until the end of 1H period	-	- (Default)

FTI1-0: Set the assert timing of the SOUT1 signal (frame timing signal) by the number of DOTCLK in 1H period. The time lag before the assert timing depends on the DOTCLK frequency. The setting of FTI[1:0] bits is enabled at the next VSYNC assert timing.

Table 32

FTI1	FTI0	Assert timing delay	Time lag before assert timing when 5MHz		
			18-bit RGB I/F (5MHz)	6-bit RGB I/F (16MHz)	
0	0	0.0 DOTCLK	0.0 μs	0.00000 μs	
0	1	7.5 DOTCLK	1.5 μs	1.40625 μs	
1	0	17.5 DOTCLK	3.5 μs	3.28125 μs	
1	1	37.5 DOTCLK	7.5 μs	7.03125 μs	(Default)

FHN: Set the assert period of the SOUT1 signal (frame timing signal). The setting of the FHN bit is enabled from the next VSYNC assert timing.

Table 33

FHN	Assert period	
0	Lasts up to 1H period. The FWI[1:0] bits are enabled.	
1	Lasts up to 2H periods. (the first 1H period starts after the assert timing delay set with FTI[1:0])	(Default)

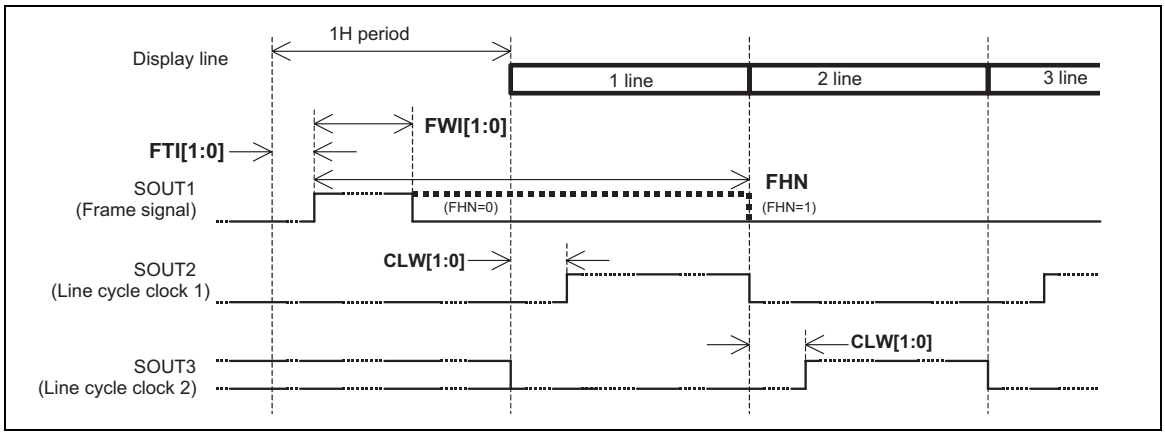


Figure 7

DSC: Control ON and OFF of LCD display signals. The setting of the DSC bit is enabled at the next VSYNC assert timing. When the level shifter outputs from the SOUT1/2/3/4 are on, the amplitude of the signals is defined by the VGH and VGL levels. Be sure to set DSC = "0" before power supply startup. See "Power Supply Setting"(p.74) for details.

Table 34

DSC	SOUT1/2/3/4 output	
0	OFF (fix all the output at the VGL level)	
1	ON	(Default)

Note 1) SOUT 1/2/3/4 are outputs from the level shifter (voltage: VGH-VGL).

GIF[1:0]: Select the combination of various LCD display signals as follows. The setting of GIF[1:0] bits is enabled at the next VSYNC assert timing. When GIF[1:0] = "11", the assert period always lasts for 1H whatever the setting of the FHN bit.

Table 35

GIF1	GIF0	SOUT2	SOUT3	SOUT4	
0	0	Line cycle clock 1	Line cycle clock 2	Output VGL	(Default)
0	1	Line cycle clock 1	Line cycle clock 2	Gete OFF signal	
1	0	Line cycle clock 1	Line cycle clock 2	Gate All ON	
1	1	Line cycle clock 3	Gate All On	Gate OFF signal	

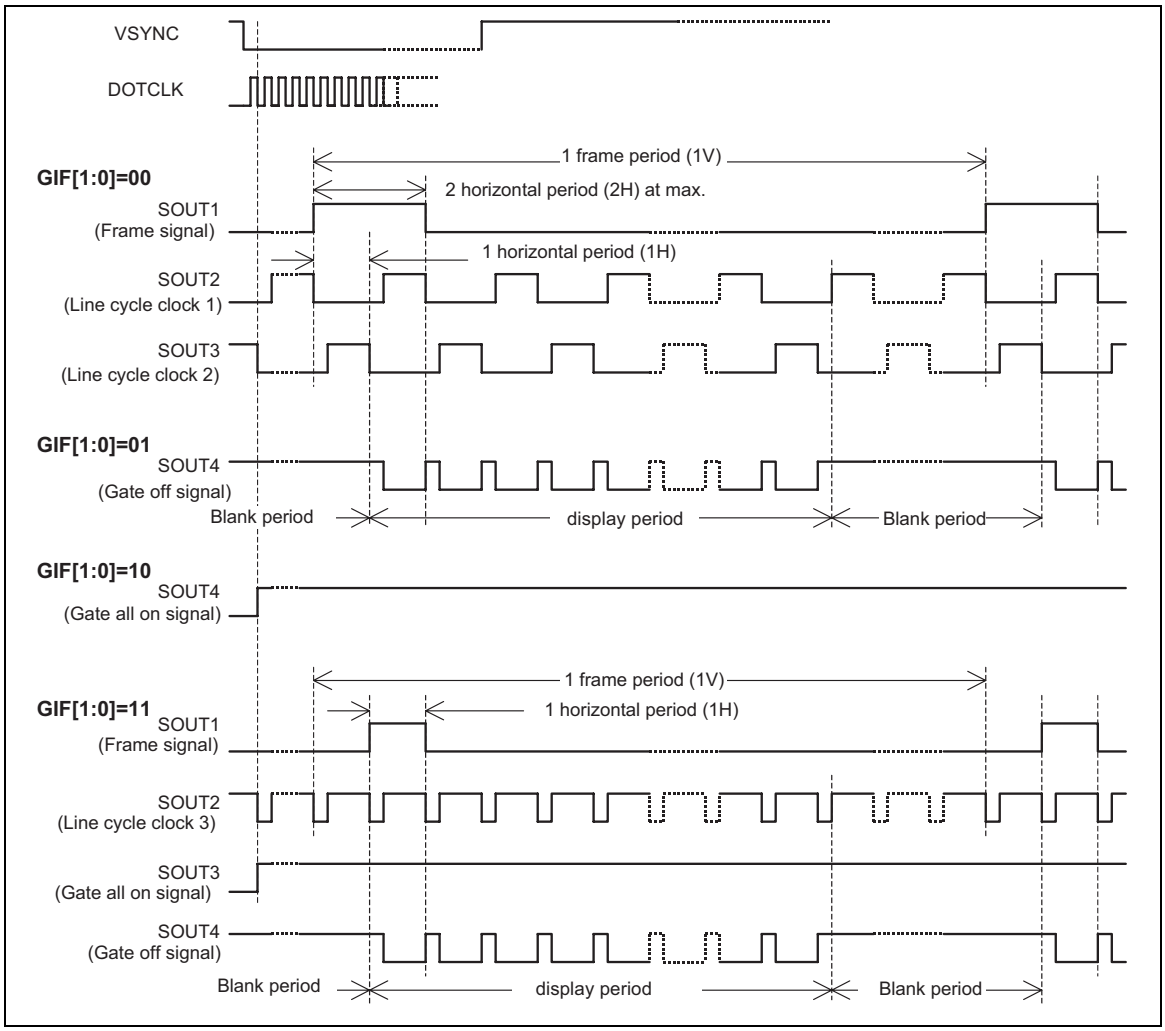


Figure 8

γ Control – positive polarity gradient adjustment: R07h

RS1	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	PRP 12	PRP 11	PRP 10	0	0	0	0	0	PRP 02	PRP 01	PRP 00
Default	-	-	-	-	-	0	0	0	-	-	-	-		0	0	0

γ Control – negative polarity gradient adjustment: R08h

RS1	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	PRN 12	PRN 11	PRN 10	0	0	0	0	0	PRN 02	PRN 01	PRN 00
Default	-	-	-	-	-	0	0	0	-	-	-	-		0	0	0

γ Control – positive polarity amplitude adjustment: R09h

RS1	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	VRP 14	VRP 13	VRP 12	VRP 11	VRP 10	0	0	0	0	VRP 03	VRP 02	VRP 01	VRP 00
Default	-	-	-	0	0	0	0	0	-	-	-	-	0	0	0	0

γ Control – negative polarity amplitude adjustment: R0Ah

RS1	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	VRN 14	VRN 13	VRN 12	VRN 11	VRN 10	0	0	0	0	VRN 03	VRN 02	VRN 01	VRN 00
Default	-	-	-	0	0	0	0	0	-	-	-	-	0	0	0	0

γ Control – Positive polarity fine adjustment: R0Bh

RS1	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	PKP 12	PKP 11	PKP 10	0	0	0	0	0	PKP 02	PKP 01	PKP 00
Default	-	-	-	-	-	0	0	0	-	-	-	-		0	0	0

γ Control – Positive polarity fine adjustment: R0Ch

RS1	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	PKP 32	PKP 31	PKP 30	0	0	0	0	0	PKP 22	PKP 21	PKP 20
Default	-	-	-	-	-	0	0	0	-	-	-	-		0	0	0

γ Control – Positive polarity fine adjustment: R0Dh

RS1	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	PKP 52	PKP 51	PKP 50	0	0	0	0	0	PKP 42	PKP 41	PKP 40
Default	-	-	-	-	-	0	0	0	-	-	-	-		0	0	0

γ Control – Negative polarity fine adjustment: R0Eh

RS1	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	PKN 12	PKN 11	PKN 10	0	0	0	0	0	PKN 02	PKN 01	PKN 00
Default	-	-	-	-	-	0	0	0	-	-	-	-		0	0	0

γ Control – Negative polarity fine adjustment: R0Fh

RS1	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	PKN 32	PKN 31	PKN 30	0	0	0	0	0	PKN 22	PKN 21	PKN 20
Default	-	-	-	-	-	0	0	0	-	-	-	-		0	0	0

γ Control – Negaitive polarity fine adjustment: R10h

RS1	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	PKN 52	PKN 51	PKN 50	0	0	0	0	0	PKN 42	PKN 41	PKN 40
Default	-	-	-	-	-	0	0	0	-	-	-	-		0	0	0

Low Power Mode: R26h

RS1	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	0	0	0	0	0	EQE	SDC	0	0	TMB1	TMB0
Default	-	-	-	-	-	-	-	-	-	-	0	0	-	0	0	0

EQE: Enable the source-Vcom equalize function. This function is available when VCOML ≥ GND. In the equalize period, the Vcom drive and source amplifiers are halted and all source output levels and the Vcom output levels are short-circuited. The equalize period lasts for the delay time set with the SDT[1:0] bits minus 10-DOTCLK period in 18-bit interface mode. In case of 6-bit interface mode, the equalize period lasts for three times longer than in 18-bit interface mode, i.e. (the delay time set with the SDT[1:0] bits minus 10-DOTCLK period) x 3.

Table 36

EQE	Function	
0	Disenable the source-Vcom equalize function	(Default)
1	Enable the source-Vcom equalize function	

SDC: The source amplifiers are halted temporarily when EQE = "0" by setting SDC = "1". The source amplifier halt period lasts for the delay time set with the SDT[1:0] bits minus 10-DOTCLK period in 18-bit interface mode. In case of 6-bit interface mode, the period lasts for three times longer than in 18-bit interface mode, i.e. (the delay time set with the SDT[1:0] bits minus 10 DOTCLK periods) x 3. When EQE = "1", the source-Vcom equalize function is dominant over this function.

Table 37

SDC	Function	
0	Disenable the source amplifier halt function	(Default)
1	Enable the source amplifier halt function	

TMB[1:0]: Changes the bias current in the source amplifiers, taking the drive capacity of different panel loads into account. When saving power consumption, set TMB[1:0] = "11" (x 0.8).

Table 38

TMB1	TMB0	Function	
0	0	Constant current in source amplifiers: x 1	(Default)
0	1	Constant current in source amplifiers: x 1.15	
1	0	Setting disabled	
1	1	Constant current in source amplifiers: x 0.8	

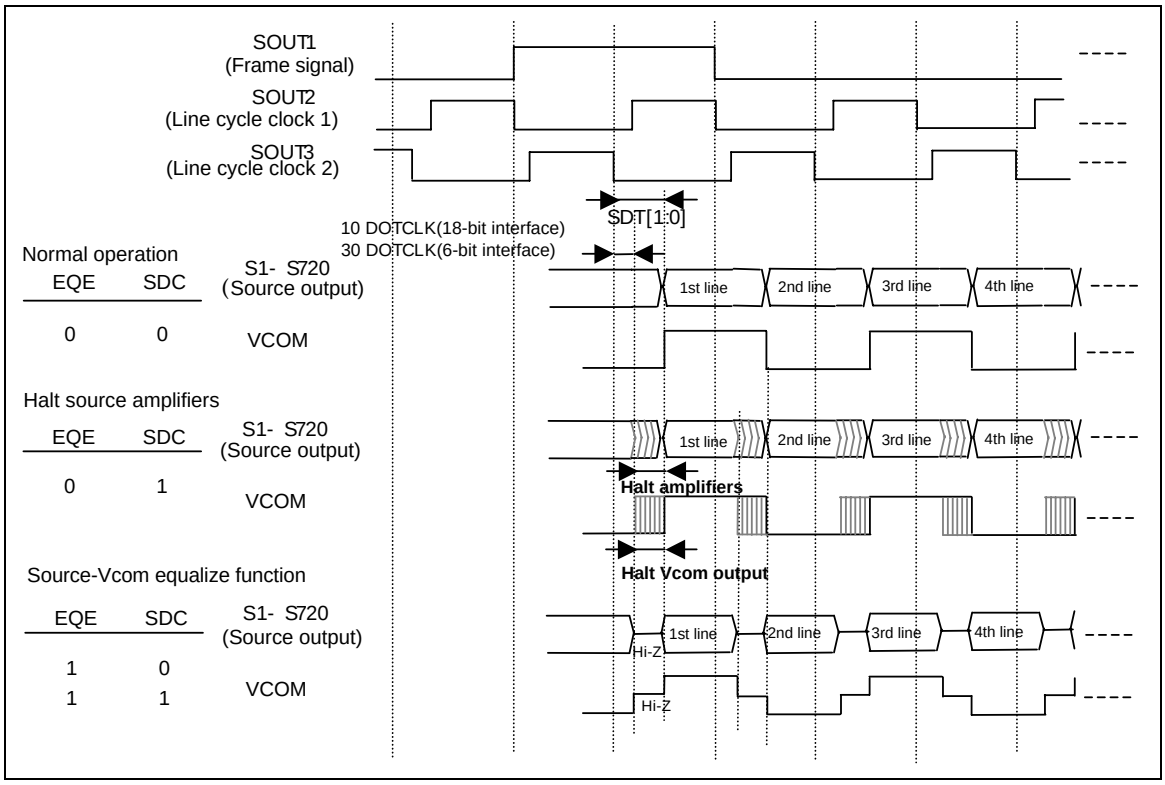

SOUT1
(Frame signal)
SOUT2
(Line cycle clock 1)
SOUT3
(Line cycle clock 2)
SDT[1:0]
10 DOTCLK(18-bit interface)
30 DOTCLK(6-bit interface)
Normal operation
EQE SDC
S1- S720
(Source output)
0 0
VCOM
1st line
2nd line
3rd line
4th line
Halt source amplifiers
EQE SDC
S1- S720
(Source output)
0 1
VCOM
Halt amplifiers
Halt Vcom output
Source-Vcom equalize function
EQE SDC
S1- S720
(Source output)
1 0
1 1
VCOM
Hi-Z

Figure 9

Instruction List

	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Index	0	0	0	0	0	0	0	0	0	0	0	0	ID4	ID3	ID21	ID1	ID0
R00h	1	0	DC12	DC11	DC10	GON	0	BT2	BT1	BT0	DC02	DC01	DC00	AP2	AP1	AP0	SLP
R01h	1	0	0	0	0	DK	0	POC	0	PON	VRH3	VRH2	VRH1	VRH0	VC2	VC1	VC0
R02h	1	0	0	VCOMG	VDV4	VDV3	VDV2	VDV1	VDV0	0	0	0	VCM4	VCM3	VCM2	VCM1	VCM0
R03h	1	0	VPL	HPL	DPL	EPL	0	0	SHL	0	0	0	0	SDT1	SDT0	0	0
R04h	1	0	0	0	0	0	0	NW1	NW0	0	0	0	0	BP3	BP2	BP1	BP0
R05h	1	0	0	CLW1	CLW0	0	0	NO1	NO0	0	0	GAON	DTE	0	REV	0	0
R06h	1	0	0	0	DSC	0	0	GIF1	GIF0	FHN	0	FTI1	FTI0	0	0	FWI1	FWI0
R07h	1	0	0	0	0	0	PRP12	PRP11	PRP10	0	0	0	0	0	PRP02	PRP01	PRP00
R08h	1	0	0	0	0	0	PRN12	PRN11	PRN10	0	0	0	0	0	PRN02	PRN01	PRN00
R09h	1	0	0	0	VRP14	VRP13	VRP12	VRP11	VRP10	0	0	0	0	VRP03	VRP02	VRP01	VRP00
R0Ah	1	0	0	0	VRN14	VRN13	VRN12	VRN11	VRN10	0	0	0	0	VRN03	VRN02	VRN01	VRN00
R0Bh	1	0	0	0	0	0	PKP12	PKP11	PKP10	0	0	0	0	0	PKP02	PKP01	PKP00
R0Ch	1	0	0	0	0	0	PKP32	PKP31	PKP30	0	0	0	0	0	PKP22	PKP21	PKP20
R0Dh	1	0	0	0	0	0	PKP52	PKP51	PKP50	0	0	0	0	0	PKP42	PKP41	PKP40
R0Eh	1	0	0	0	0	0	PKN12	PKN11	PKN10	0	0	0	0	0	PKN02	PKN01	PKN00
R0Fh	1	0	0	0	0	0	PKN32	PKN31	PKN30	0	0	0	0	0	PKN22	PKN21	PKN20
R10h	1	0	0	0	0	0	PKN52	PKN51	PKN50	0	0	0	0	0	PKN42	PKN41	PKN40
R26h	1	0	0	0	0	0	0	0	0	0	0	EQE	SDC	0	0	TMB1	TMB0

Reset Function

The HD66790 is internally initialized with an input of RESET. During the reset period, the intenal state of the HD66790 is busy and no access from external devices is accepted. At least 1 ms must be secured for the reset period. In case of power-on reset, data transfer and making initial instruction setting are prohibited.

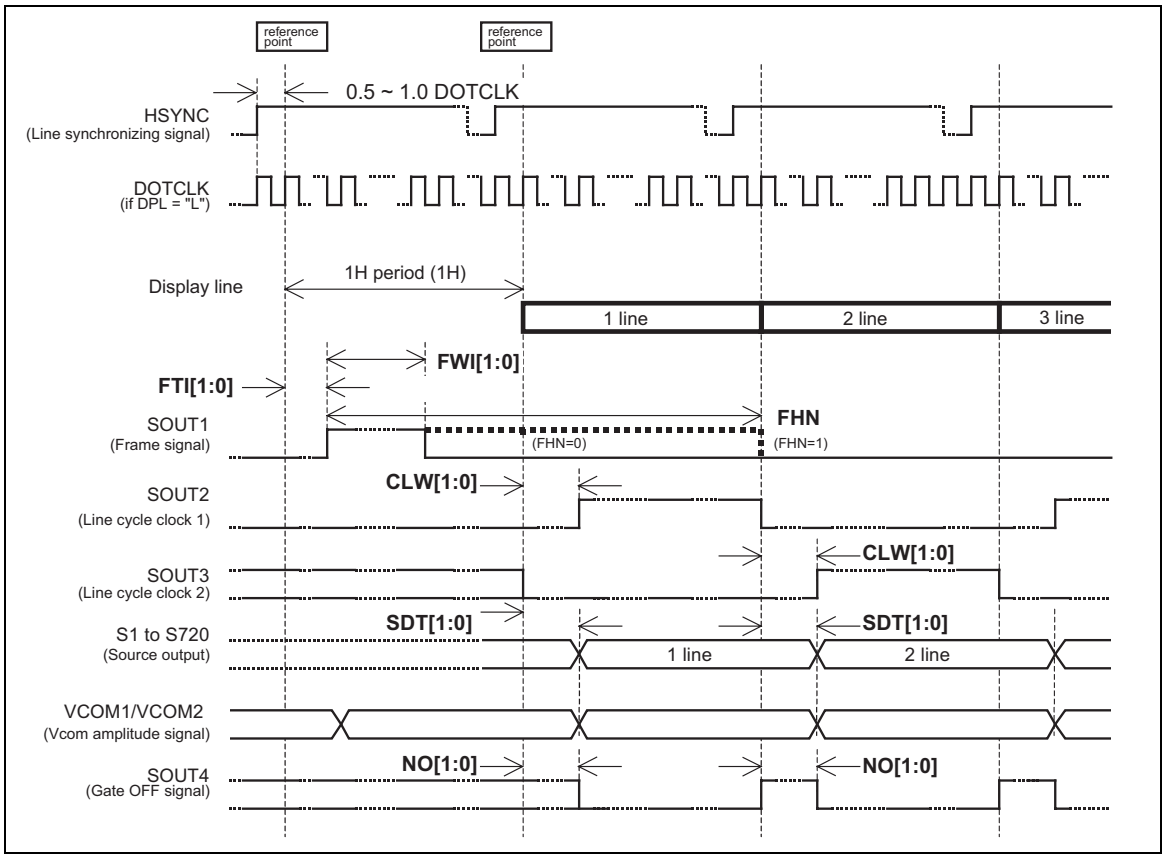
1. Initial setting of instruction: See the descriptions of registers in the “Instruction” section.

2. Initial state of output pins:

LCD display outputs:	SOUT1-4R/L	Output the “VGL” level.
AC drive amplitude signal:	VCOMS	Output the “GND” level.

LCD Signal Output Timing Control Function

The following is a timing chart of control signals of the HD66790.



Note: When GIF[1:0] = “11”, the assert period is always 1H whatever the setting of the FHN bit.

Figure 10

Power Control Function

When POC = “L”, a white display is shown on the screen.

Note 1) In POC mode, the panel display signals (from the SOUT1/2/3/4 pins) are output normally.
Note 2) The setting of the POC bit changes in synchronization with the VSYNC signal and the resulting source output levels are output from the next assert timing.

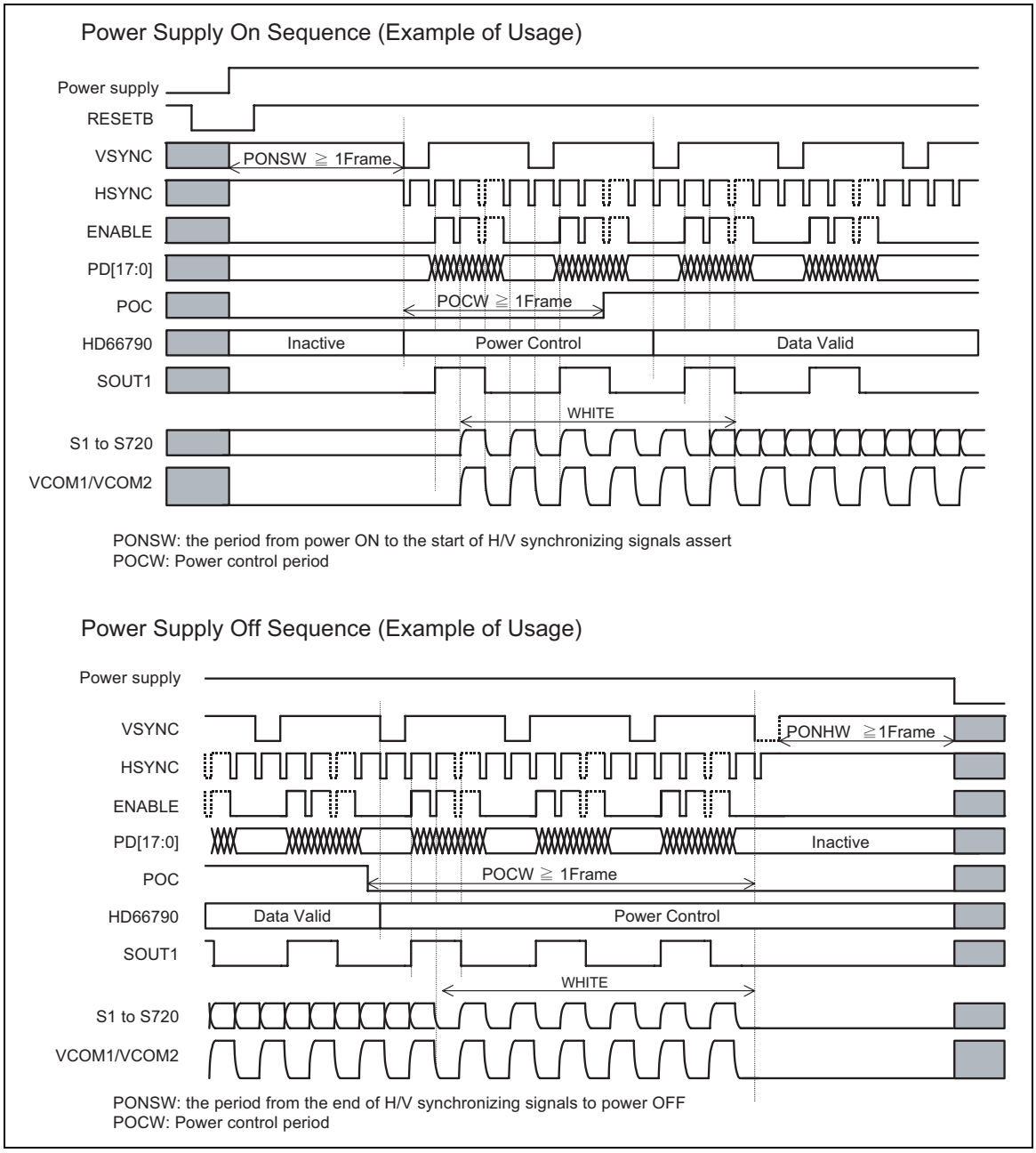


Figure 11

POC, VCOMG, LSENR/L output control

The setting of these three bits and the respective output control functions are as follows.

Source output (Sn) control by POC

Table 39

POC	Operation mode	Source output (Sn)
0	Power control mode	WHITE
1	Normal operation mode	Input data

Panel display signals (SOUT*) control by LSENL/LSENR

Table 40

LSENL	LSENR	Level shifter output level	
		SOUT1/2/3/4L	SOUT1/2/3/4R
0	0	Fixed to VGL	Fixed to VGL
0	1	Fixed to VGL	VGH – VGL
1	0	VGH – VGL	Fixed to VGL
1	1	VGH – VGL	VGH – VGL

VCOM control by VCOMG

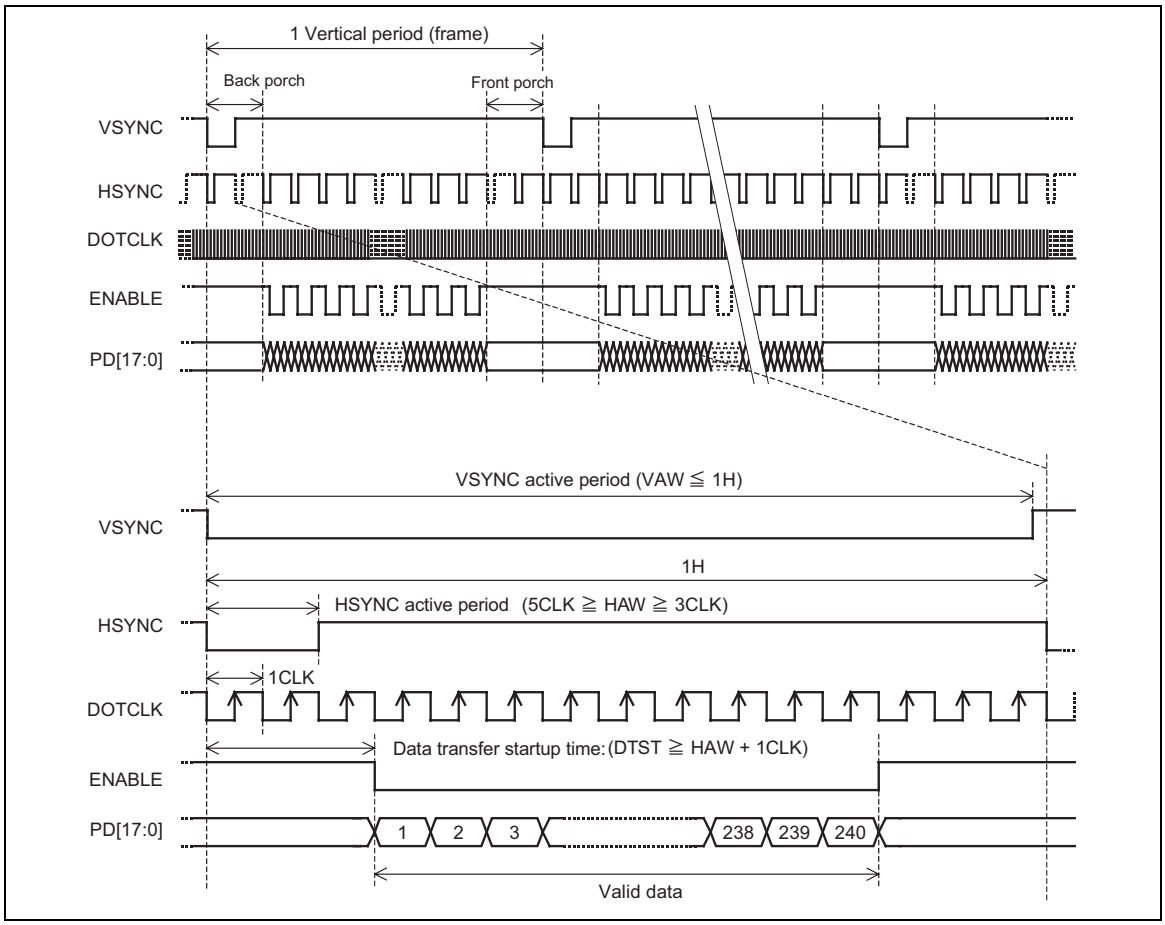
Table 41

VCOMG	VCOM output
0	GND
1	Vcom output

RGB Interface

RGB interface timing 1 (18-bit transfer mode)

The following is the timing chart of signals in 18-bit RGB interface mode.

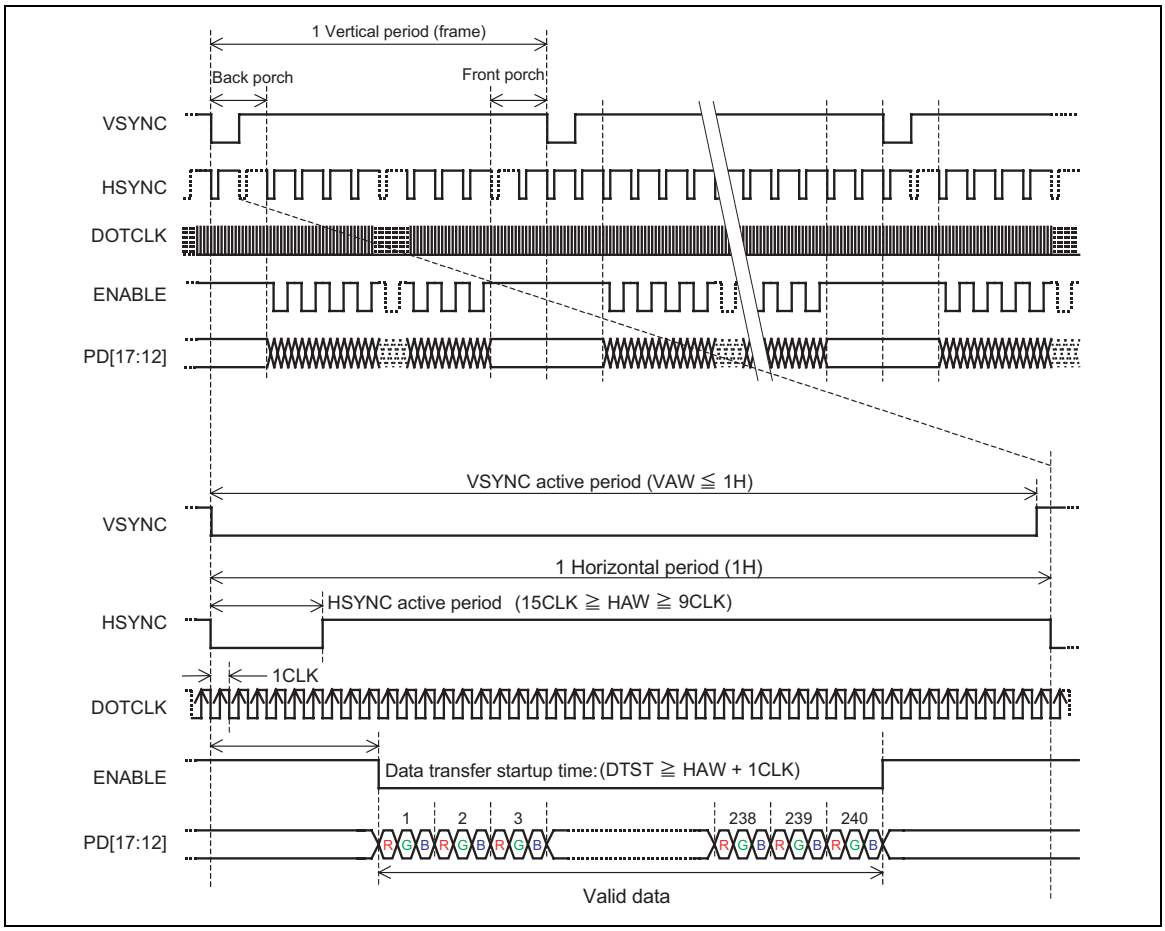


VAW: VSYNC active period
HAW: HSYNC active period
DTST: data transfer startup time

Figure 12

RGB interface timing 2 (6-bit transfer x 3)

The following is the timing chart of signals in 6-bit RGB interface mode.



VAW: VSYNC active period
HAW: HSYNC active period
DTST: data transfer startup time

Figure 13

Interface timing to the LCD panel

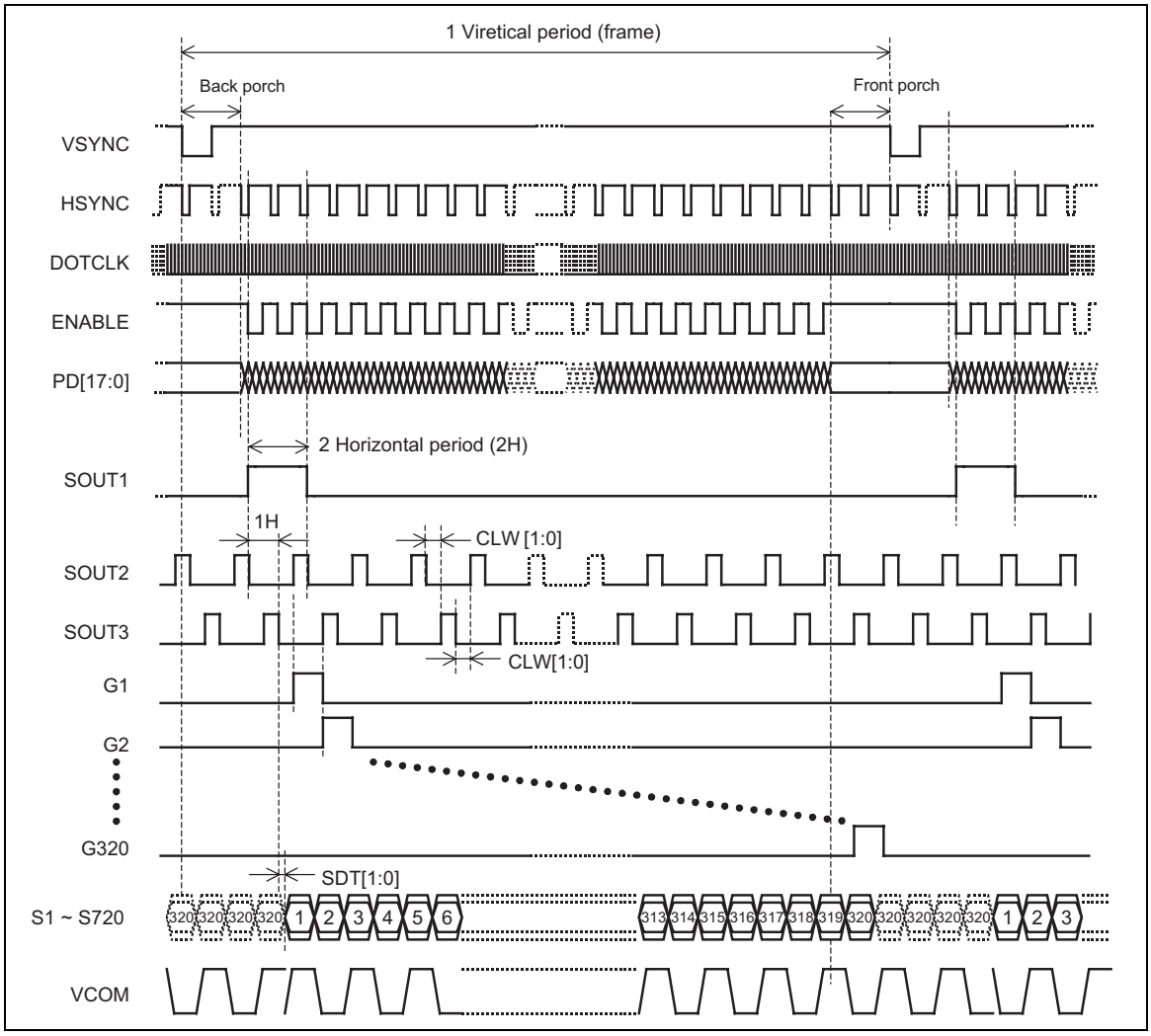


Figure 14

Serial Peripheral Interface (SPI)

The Serial Peripheral Interface enables instruction set in the registers via the chip select (CS), serial clock (SCL), and serial data input (SDI) ports.

The HD66790 recognizes the start of data transfer on the falling edge of a CS input and starts taking in data. The HD66790 recognizes the end of data transfer on the rising edge of a CS input and stops transferring data. Data are transferred in units of 16 bits from the MSB.

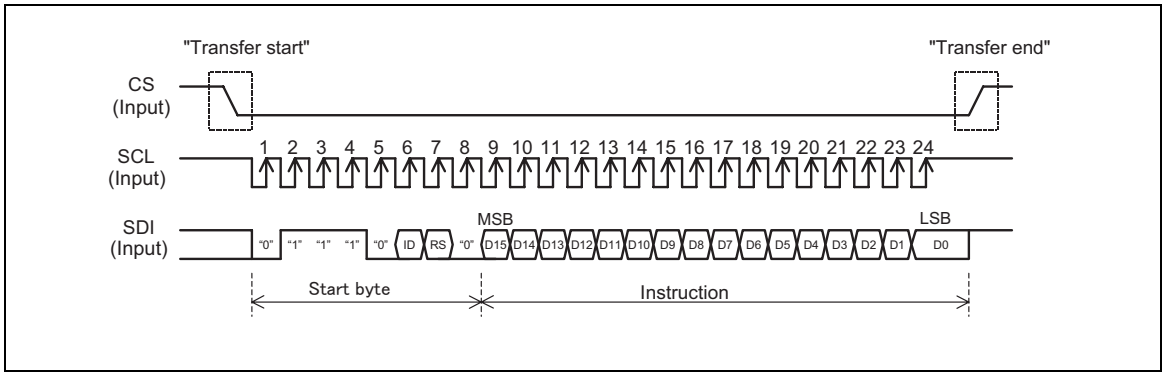


Figure 15

Data Shift Direction

The HD66790 allows changing the data shift direction of source signals by setting the register R03h: D8 (SHL bit). Select either one direction suitable for the module.

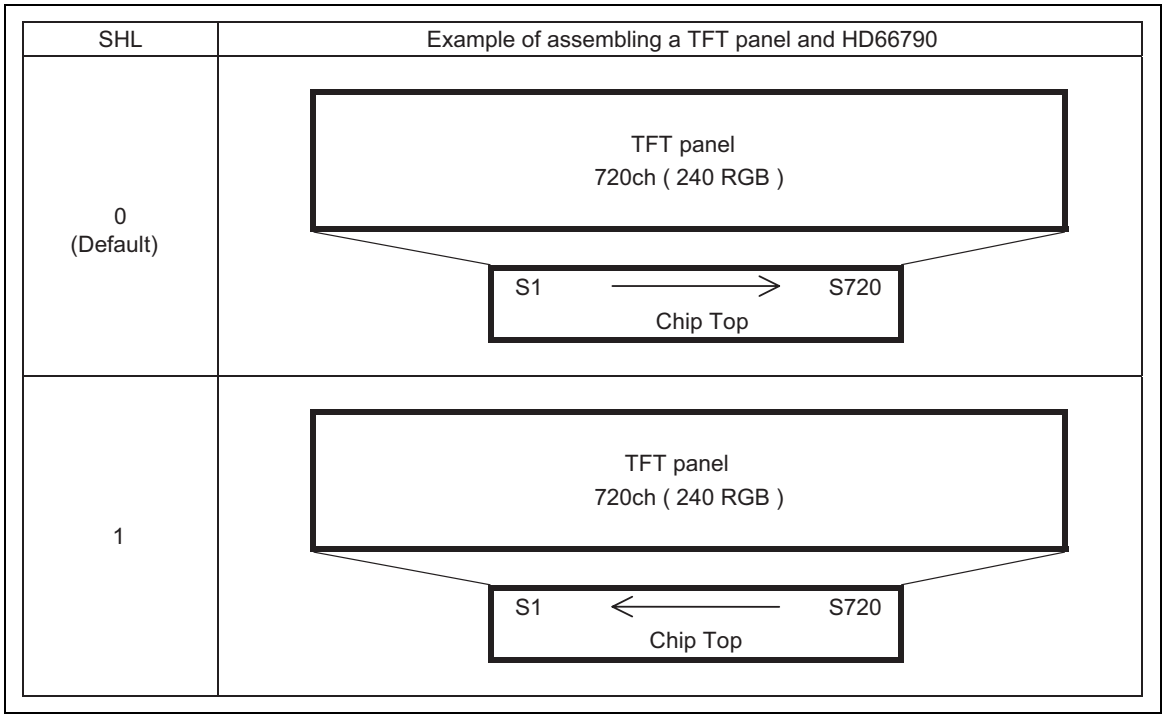


Figure 16

Liquid Crystal AC Drive

The HD66790 supports the line-inversion or the 2-line inversion AC drive in addition to the frame-inversion AC drive of the LCD panel, selected by setting the register R04h:D[9:8](NW[1:0] bits). Check the quality of display on the panel in selecting the alternating cycle. Note that the shorter alternating interval increases charging/discharging current on liquid crystal cells due to the high liquid crystal alternating frequency.

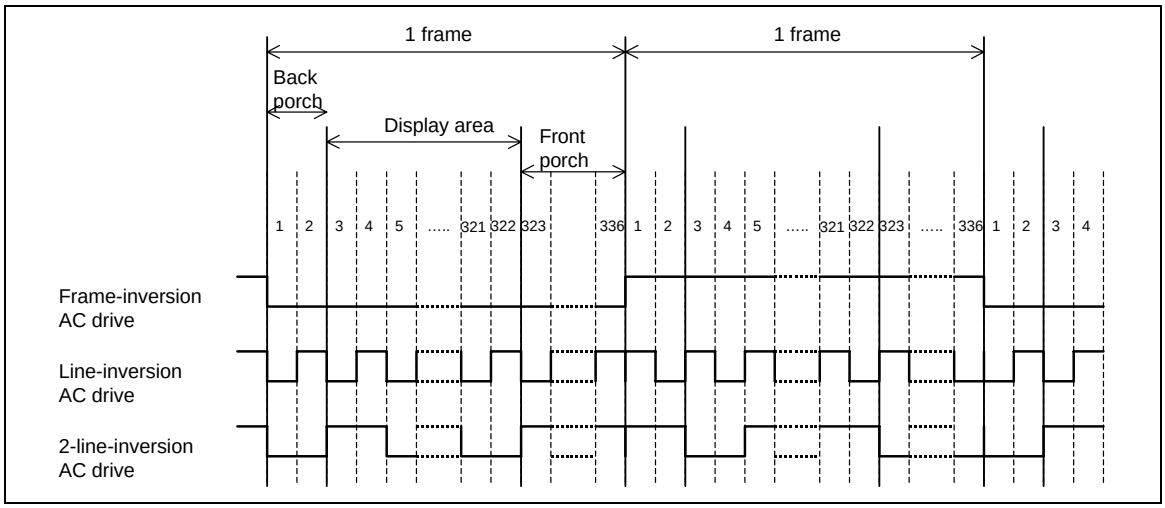


Figure 17

LCD Display Signal Control

The HD66790 allows selecting the optimal LCD signal combination for the system structure. Also, see the description of "Display signal select control: R06h" in the "Instruction" section for details on the timing relationship of these signals.

Register setting

Table 42

DSC	GIF1	GIF0	Voltage amplitude of outputs from the Level shifter: VGH-VGL (unless specified otherwise)		
			SOUT2	SOUT3	SOUT4
0	0	0	Output the VGL level		
	0	1			
	1	0			
	1	1			
1	0	0	Line cycle clock 1	Line cycle clock 2	Output the VGL level
	0	1			Gate off signal
	1	0			Gate-all-on signal
	1	1	Line cycle clock 3	Gate-all-on signal	Gate off signal

Configuration of Grayscale Amplifier Unit

The following is the configuration of grayscale amplifier unit of the HD66790. The supply voltage inputs into the VREF0P ~ VREFF4P, VREF0N ~ VREF4N are divided internally with internal resistors to generate 64 voltage levels for grayscales V0 ~ V63.

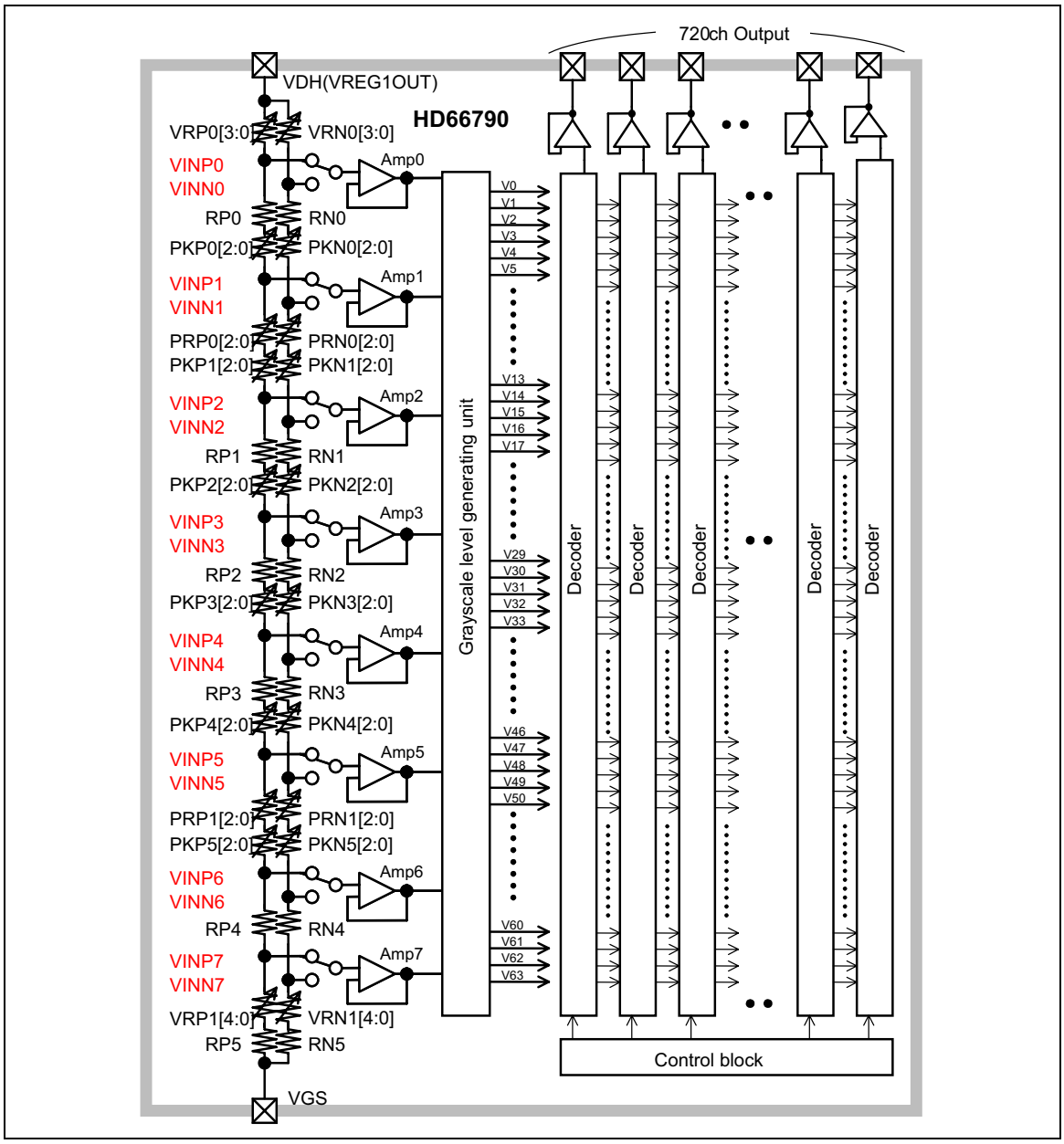


Figure 18

Configuration of grayscale level generating unit

The following is the configuration of grayscale level generating unit. To generate 64 grayscale voltages (V0~V63), the HD66790 first generates eight reference grayscale voltage levels (VINP0-7/VINN0-7) according to the gradient and fine adjustment registers, which are then divided with the ladder resistors.

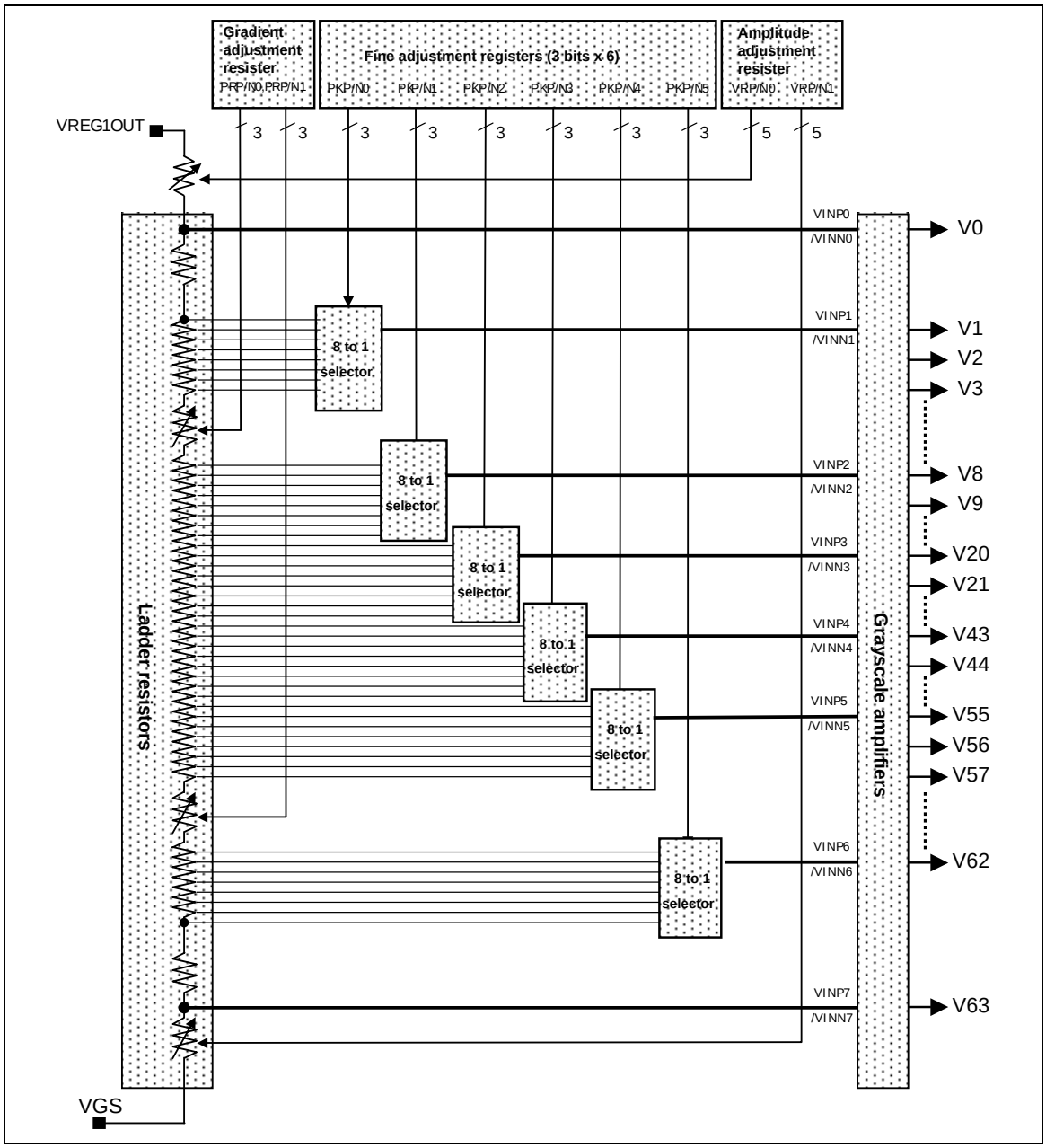


Figure 19

Reference voltage generating block (ladder resistor units and 8-to-1 selectors)

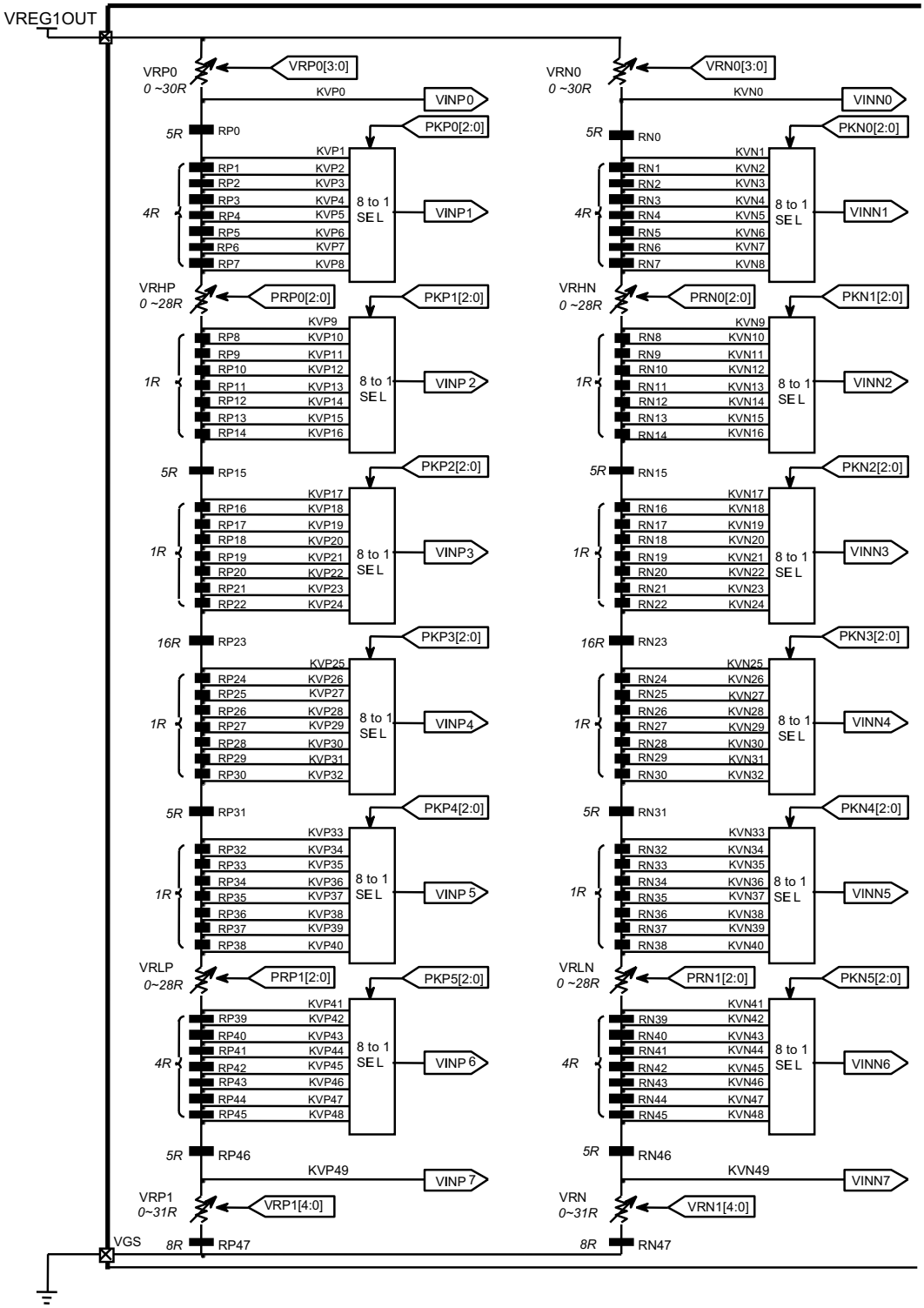


Figure 20

γ-Correction Register

The γ-correction registers of the HD66790 consist of gradient adjustment, amplitude adjustment, and fine-adjustment registers, each consists of registers of positive and negative polarities. Each register can be set independently, enabling optimal adjustment of grayscale voltage levels in relation to grayscales for the γ-characteristics of the liquid crystal panel. These settings in the γ-correction registers and the reference levels for the 64 grayscales, to which these three kinds of adjustments are made, are common to all RGB dots.

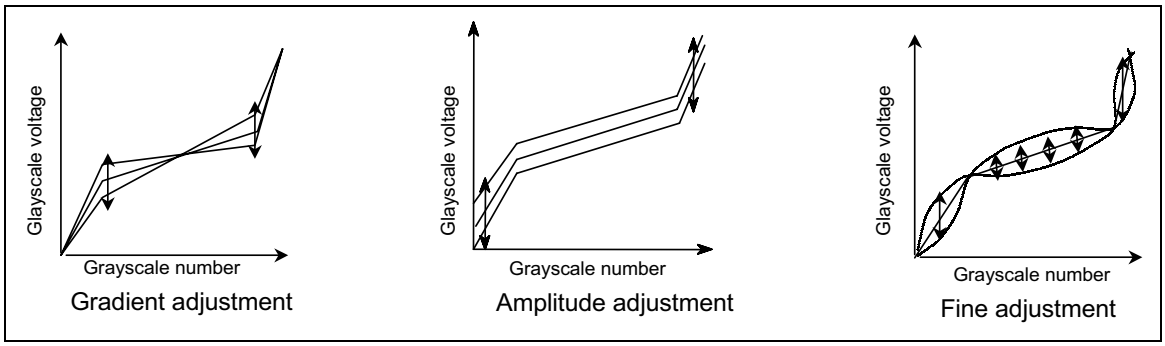


Figure 21

1. Gradient adjustment registers

The gradient adjustment registers are used to adjust the gradient of the curve representing the relationship between the grayscale and the grayscale voltage level around middle grayscales without changing the dynamic range. To adjust the gradient, the resistance values of grayscale reference voltage generating variable resistors (VRHP(N)/VRLP(N)) in the middle of the ladder resistor unit are adjusted. The registers consist of positive and negative polarity registers, allowing asymmetric drive.

2. Amplitude adjustment registers

The amplitude adjustment registers are used to adjust the amplitude of grayscale voltages. To adjust the amplitude, the resistance values of the grayscale voltage generating variable resistors (VRP(N)1/0) at the top and bottom of the ladder resistor unit are adjusted. Same with the gradient registers, the amplitude adjustment registers consist of positive and negative polarity registers.

3. Fine adjustment registers

The fine adjustment registers are used to fine-adjust grayscale voltage levels. To fine-adjust grayscale voltage levels, fine adjustment registers adjust the reference voltage levels, 8 levels for each register generated from the ladder resistor unit, in respective 8-to-1 selectors. Same with other registers, the fine adjustment registers consist of positive and negative polarity registers.

Table 43

Register Groups	Positive Polarity	Negative Polarity	Description
Gradient adjustment	PRP0 [2:0]	PRN0 [2:0]	Variable resistor VRHP (N)
	PRP1 [2:0]	PRN1 [2:0]	Variable resistor VRLP (N)
Amplitude adjustment	VRP0 [3:0]	VRN0 [3:0]	Variable resistor VRP (N)0
	VRP1 [4:0]	VRN1 [4:0]	Variable resistor VRP (N)1
Fine adjustment	PKP0 [2:0]	PKN0 [2:0]	8-to-1 selector (voltage level of grayscale 1)
	PKP1 [2:0]	PKN1 [2:0]	8-to-1 selector (voltage level of grayscale 8)
	PKP2 [2:0]	PKN2 [2:0]	8-to-1 selector (voltage level of grayscale 20)
	PKP3 [2:0]	PKN3 [2:0]	8-to-1 selector (voltage level of grayscale 43)
	PKP4 [2:0]	PKN4 [2:0]	8-to-1 selector (voltage level of grayscale 55)
	PKP5 [2:0]	PKN5 [2:0]	8-to-1 selector (voltage level of grayscale 62)

Ladder resistors and 8-to-1 selector

Block configuration

The reference voltage generating unit as illustrated in page 62 consists of two ladder resistor units including variable resistors and 8-to-1 selectors. Each 8-to-1 selector selects one of the 8 voltage levels generated from the ladder resistor unit to output as a grayscale reference voltage. Both variable resistors and 8-to-1 selectors are controlled according to the γ correction registers. This unit has pins to connect a volume resistor externally to compensate differences in various characteristics of panels.

Variable resistors

The HD66790 uses variable resistors of the following three purposes: gradient adjustment (VRHP(N)/VRLP(N)); amplitude adjustment (1) (VRP(N)0); and the amplitude adjustment (2) (VRP(N)1). The resistance values of these variable resistors are set by gradient adjustment registers and amplitude adjustment registers as follows.

Table 44

Gradient adjustment

Contents of Register PRP(N) 0/1[2:0]	Resistance VRHP(N) VRLP(N)
000	0R
001	4R
010	8R
011	12R
100	16R
101	20R
110	24R
111	28R

Table 45

Amplitude adjustment (1)

Contents of Register VRP(N)0[3:0]	Resistance VRP(N)0
0000	0R
0001	2R
0010	4R
:	:
:	:
1101	26R
1111	28R
1111	30R

Table 46

Amplitude adjustment (2)

Contents of Register VRP(N)1[4:0]	Resistance VRP(N)1
00000	0R
00001	1R
00010	2R
:	:
:	:
11101	29R
11110	30R
11111	31R

8-to-1 selectors

The 8-to-1 selector selects one of eight voltage levels generated from the ladder resistor unit according to the fine adjustment register, and output the selected voltage level as a reference grayscale voltage (VINP(N)1~ VINP(N 6). The table below shows the setting in the fine adjustment register and the selected voltage levels for respective reference grayscale voltages.

Table 47 Fine adjustment registers and selected voltage

The value of Register	Selected Voltage					
PKP(N)[2:0]	VINP(N)1	VINP(N)2	VINP(N)3	VINP(N)4	VINP(N)5	VINP(N)6
000	KVP(N)1	KVP(N)9	KVP(N)17	KVP(N)25	KVP(N)33	KVP(N)41
001	KVP(N)2	KVP(N)10	KVP(N)18	KVP(N)26	KVP(N)34	KVP(N)42
010	KVP(N)3	KVP(N)11	KVP(N)19	KVP(N)27	KVP(N)35	KVP(N)43
011	KVP(N)4	KVP(N)12	KVP(N)20	KVP(N)28	KVP(N)36	KVP(N)44
100	KVP(N)5	KVP(N)13	KVP(N)21	KVP(N)29	KVP(N)37	KVP(N)45
101	KVP(N)6	KVP(N)14	KVP(N)22	KVP(N)30	KVP(N)38	KVP(N)46
110	KVP(N)7	KVP(N)15	KVP(N)23	KVP(N)31	KVP(N)39	KVP(N)47
111	KVP(N)8	KVP(N)16	KVP(N)24	KVP(N)32	KVP(N)40	KVP(N)48

Grayscale voltage calculating formulae (Positive polarity)

Table 48

Pin	Formula	Fine adjustment register value	Reference Voltage
KVP0	VREG1OUT - ΔV*VRP0/SUMRP	-	VINP0
KVP1	VREG1OUT - ΔV*(VRP0+5R)/SUMRP	PKP02-00 = "000"	VINP1
KVP2	VREG1OUT - ΔV*(VRP0+9R)/SUMRP	PKP02-00 = "001"	
KVP3	VREG1OUT - ΔV*(VRP0+13R)/SUMRP	PKP02-00 = "010"	
KVP4	VREG1OUT - ΔV*(VRP0+17R)/SUMRP	PKP02-00 = "011"	
KVP5	VREG1OUT - ΔV*(VRP0+21R)/SUMRP	PKP02-00 = "100"	
KVP6	VREG1OUT - ΔV*(VRP0+25R)/SUMRP	PKP02-00 = "101"	
KVP7	VREG1OUT - ΔV*(VRP0+29R)/SUMRP	PKP02-00 = "110"	
KVP8	VREG1OUT - ΔV*(VRP0+33R)/SUMRP	PKP02-00 = "111"	
KVP9	VREG1OUT - ΔV*(VRP0+33R+VRHP)/SUMRP	PKP12-10 = "000"	VINP2
KVP10	VREG1OUT - ΔV*(VRP0+34R+VRHP)/SUMRP	PKP12-10 = "001"	
KVP11	VREG1OUT - ΔV*(VRP0+35R+VRHP)/SUMRP	PKP12-10 = "010"	
KVP12	VREG1OUT - ΔV*(VRP0+36R+VRHP)/SUMRP	PKP12-10 = "011"	
KVP13	VREG1OUT - ΔV*(VRP0+37R+VRHP)/SUMRP	PKP12-10 = "100"	
KVP14	VREG1OUT - ΔV*(VRP0+38R+VRHP)/SUMRP	PKP12-10 = "101"	
KVP15	VREG1OUT - ΔV*(VRP0+39R+VRHP)/SUMRP	PKP12-10 = "110"	
KVP16	VREG1OUT - ΔV*(VRP0+40R+VRHP)/SUMRP	PKP12-10 = "111"	
KVP17	VREG1OUT - ΔV*(VRP0+45R+VRHP)/SUMRP	PKP22-20 = "000"	VINP3
KVP18	VREG1OUT - ΔV*(VRP0+46R+VRHP)/SUMRP	PKP22-20 = "001"	
KVP19	VREG1OUT - ΔV*(VRP0+47R+VRHP)/SUMRP	PKP22-20 = "010"	
KVP20	VREG1OUT - ΔV*(VRP0+48R+VRHP)/SUMRP	PKP22-20 = "011"	
KVP21	VREG1OUT - ΔV*(VRP0+49R+VRHP)/SUMRP	PKP22-20 = "100"	
KVP22	VREG1OUT - ΔV*(VRP0+50R+VRHP)/SUMRP	PKP22-20 = "101"	
KVP23	VREG1OUT - ΔV*(VRP0+51R+VRHP)/SUMRP	PKP22-20 = "110"	
KVP24	VREG1OUT - ΔV*(VRP0+52R+VRHP)/SUMRP	PKP22-20 = "111"	
KVP25	VREG1OUT - ΔV*(VRP0+68R+VRHP)/SUMRP	PKP32-30 = "000"	VINP4
KVP26	VREG1OUT - ΔV*(VRP0+69R+VRHP)/SUMRP	PKP32-30 = "001"	
KVP27	VREG1OUT - ΔV*(VRP0+70R+VRHP)/SUMRP	PKP32-30 = "010"	
KVP28	VREG1OUT - ΔV*(VRP0+71R+VRHP)/SUMRP	PKP32-30 = "011"	
KVP29	VREG1OUT - ΔV*(VRP0+72R+VRHP)/SUMRP	PKP32-30 = "100"	
KVP30	VREG1OUT - ΔV*(VR P0+73R+VRHP)/SUMRP	PKP32-30 = "101"	
KVP31	VREG1OUT - ΔV*(VRP0+74R+VRHP)/SUMRP	PKP32-30 = "110"	
KVP32	VREG1OUT - ΔV*(VRP0+75R+VRHP)/SUMRP	PKP32-30 = "111"	
KVP33	VREG1OUT - ΔV*(VRP0+80R+VRHP)/SUMRP	PKP42-40 = "000"	VINP5
KVP34	VREG1OUT - ΔV*(VRP0+81R+VRHP)/SUMRP	PKP42-40 = "001"	
KVP35	VREG1OUT - ΔV*(VRP0+82R+VRHP)/SUMRP	PKP42-40 = "010"	
KVP36	VREG1OUT - ΔV*(VRP0+83R+VRHP)/SUMRP	PKP42-40 = "011"	
KVP37	VREG1OUT - ΔV*(VRP0+84R+VRHP)/SUMRP	PKP42-40 = "100"	
KVP38	VREG1OUT - ΔV*(VRP0+85R+VRHP)/SUMRP	PKP42-40 = "101"	
KVP39	VREG1OUT - ΔV*(VRP0+86R+VRHP)/SUMRP	PKP42-40 = "110"	
KVP40	VREG1OUT - ΔV*(VRP0+87R+VRHP)/SUMRP	PKP42-40 = "111"	
KVP41	VREG1OUT - ΔV*(VRP0+87R+VRHP+VRLP)/SUMRP	PKP52-50 = "000"	VINP6
KVP42	VREG1OUT - ΔV*(VRP0+91R+VRHP+VRLP)/SUMRP	PKP52-50 = "001"	
KVP43	VREG1OUT - ΔV*(VRP0+95R+VRHP+VRLP)/SUMRP	PKP52-50 = "010"	
KVP44	VREG1OUT - ΔV*(VRP0+99R+VRHP+VRLP)/SUMRP	PKP52-50 = "011"	
KVP45	VREG1OUT - ΔV*(VRP0+103R+VRHP+VRLP)/SUMRP	PKP52-50 = "100"	
KVP46	VREG1OUT - ΔV*(VRP0+107R+VRHP+VRLP)/SUMRP	PKP52-50 = "101"	
KVP47	VREG1OUT - ΔV*(VRP0+111R+VRHP+VRLP)/SUMRP	PKP52-50 = "110"	
KVP48	VREG1OUT - ΔV*(VRP0+115R+VRHP+VRLP)/SUMRP	PKP52-50 = "111"	
KVP49	VREG1OUT - ΔV*(VRP0+120R+VRHP+VRLP)/SUMRP	-	VINP7

SUMRP : Sum of positive ladder resistors = 128R+VRHP+VRLP+VRP0+VRP1
SUMRN : Sum of negative ladder resistors = 128R+VRHN+VRLN+VRN0+VRN1
ΔV : Voltage difference between VREG1OUT and VGS.

Grayscale voltage calculating formulae (Positive polarity)

Table 49

Grayscale	Formula
V0	VINP0
V1	VINP1
V2	V1-(V1-V8)*(9/24)
V3	V1-(V1-V8)*(12.5/24)
V4	V1-(V1-V8)*(16/24)
V5	V1-(V1-V8)*(18/24)
V6	V1-(V1-V8)*(20/24)
V7	V1-(V1-V8)*(22/24)
V8	VINP2
V9	V8-(V8-V12)*6/24
V10	V8-(V8-V12)*12/24
V11	V8-(V8-V12)*18/24
V12	V8-(V8-V20)*8/24
V13	V12-(V12-V16)*6/24
V14	V12-(V12-V16)*12/24
V15	V12-(V12-V16)*18/24
V16	V8-(V8-V20)*16/24
V17	V16-(V16-V20)*6/24
V18	V16-(V16-V20)*12/24
V19	V16-(V16-V20)*18/24
V20	VINP3
V21	V20-(V20-V26)*4/24
V22	V20-(V20-V26)*8/24
V23	V20-(V20-V26)*12/24
V24	V20-(V20-V26)*16/24
V25	V20-(V20-V26)*20/24
V26	V20-(V20-V43)*6/24
V27	V26-(V26-v3132)*4/24
V28	V26-(V26-v3132)*8/24
V29	V26-(V26-v3132)*12/24
V30	V26-(V26-v3132)*16/24
V31	V26-(V26-v3132)*20/24

∴v3132=V20-(V20-V43)*12/24

Grayscale	Formula
V32	v3132-(v3132-V37)*4/24
V33	v3132-(v3132-V37)*8/24
V34	v3132-(v3132-V37)*12/24
V35	v3132-(v3132-V37)*16/24
V36	v3132-(v3132-V37)*20/24
V37	V20-(V20-V43)*18/24
V38	V37-(V37-V43)*4/24
V39	V37-(V37-V43)*8/24
V40	V37-(V37-V43)*12/24
V41	V37-(V37-V43)*16/24
V42	V37-(V37-V43)*20/24
V43	VINP4
V44	V43-(V43-V47)*6/24
V45	V43-(V43-V47)*12/24
V46	V43-(V43-V47)*18/24
V47	V43-(V43-V55)*8/24
V48	V47-(V47-V51)*6/24
V49	V47-(V47-V51)*12/24
V50	V47-(V47-V51)*18/24
V51	V43-(V43-V55)*16/24
V52	V51-(V51-V55)*6/24
V53	V51-(V51-V55)*12/24
V54	V51-(V51-V55)*18/24
V55	VINP5
V56	V55-(V55-V62)*2/24
V57	V55-(V55-V62)*4/24
V58	V55-(V55-V62)*6/24
V59	V55-(V55-V62)*8/24
V60	V55-(V55-V62)*11.5/24
V61	V55-(V55-V62)*15/24
V62	VINP6
V63	VINP7

Note: Make sure the following relationship:
DDVDH-V0>0.5V
DDVDH-V8>1.1V

Grayscale voltage calculating formulae (Negative polarity)

Table 50

Pin	Formula	Fine adjustment register value	Reference Voltage
KVP0	VREG1OUT - ΔV*VRN0/SUMRN	-	VINN0
KVN1	VREG1OUT - ΔV* (VRN0+5R)/SUMRN	PKN 02-00 = "000"	VINN1
KVN2	VREG1OUT - ΔV* (VRN0+9R)/SUMRN	PKN 02-00 = "001"	
KVN3	VREG1OUT - Δ V* (VRN0+13R)/SUMRN	PKN 02-00 = "010"	
KVN4	VREG1OUT - Δ V* (VRN0+17R)/SUMRN	PKN 02-00 = "011"	
KVN5	VREG1OUT - Δ V* (VRN0+21R)/SUMRN	PKN 02-00 = "100"	
KVN6	VREG1OUT - Δ V* (VRN0+25R)/SUMRN	PKN 02-00 = "101"	
KVN7	VREG1OUT - Δ V* (VRN0+29R)/SUMRN	PKN 02-00 = "110"	
KVN8	VREG1OUT - Δ V* (VRN0+33R)/SUMRN	PKN 02-00 = "111"	
KVN9	VREG1OUT - Δ V*(VRN0+33R+VRHN)/SUMRN	PKN 12-10 = "000"	VINN2
KVN10	VREG1OUT - Δ V*(VRN0+34R+VRHN)/SUMRN	PKN 12-10 = "001"	
KVN11	VREG1OUT - Δ V*(VRN0+35R+VRHN)/SUMRN	PKN 12-10 = "010"	
KVN12	VREG1OUT - Δ V*(VRN0+36R+VRHN)/SUMRN	PKN 12-10 = "011"	
KVN13	VREG1OUT - Δ V*(VRN0+37R+VRHN)/SUMRN	PKN 12-10 = "100"	
KVN14	VREG1OUT - Δ V*(VRN0+38R+VRHN)/SUMRN	PKN 12-10 = "101"	
KVN15	VREG1OUT - Δ V*(VRN0+39R+VRHN)/SUMRN	PKN 12-10 = "110"	
KVN16	VREG1OUT - Δ V*(VRN0+40R+VRHN)/SUMRN	PKN 12-10 = "111"	
KVN17	VREG1OUT - Δ V*(VRN0+45R+VRHN)/SUMRN	PKN 22-20 = "000"	VINN3
KVN18	VREG1OUT - Δ V*(VRN0+46R+VRHN)/SUMRN	PKN 22-20 = "001"	
KVN19	VREG1OUT - Δ V*(VRN0+47R+VRHN)/SUMRN	PKN 22-20 = "010"	
KVN20	VREG1OUT - Δ V*(VRN0+48R+VRHN)/SUMRN	PKN 22-20 = "011"	
KVN21	VREG1OUT - Δ V*(VRN0+49R+VRHN)/SUMRN	PKN 22-20 = "100"	
KVN22	VREG1OUT - Δ V*(VRN0+50R+VRHN)/SUMRN	PKN 22-20 = "101"	
KVN23	VREG1OUT - Δ V*(VRN0+51R+VRHN)/SUMRN	PKN 22-20 = "110"	
KVN24	VREG1OUT - Δ V*(VRN0+52R+VRHN)/SUMRN	PKN 22-20 = "111"	
KVN25	VREG1OUT - Δ V*(VRN0+68R+VRHN)/SUMRN	PKN 32-30 = "000"	VINN4
KVN26	VREG1OUT - Δ V*(VRN0+69R+VRHN)/SUMRN	PKN 32-30 = "001"	
KVN27	VREG1OUT - Δ V*(VRN0+70R+VRHN)/SUMRN	PKN 32-30 = "010"	
KVN28	VREG1OUT - Δ V*(VRN0+71R+VRHN)/SUMRN	PKN 32-30 = "011"	
KVN29	VREG1OUT - Δ V*(VRN0+72R+VRHN)/SUMRN	PKN 32-30 = "100"	
KVN30	VREG1OUT - Δ V*(VRN0+73R+VRHN)/SUMRN	PKN 32-30 = "101"	
KVN31	VREG1OUT - Δ V*(VRN0+74R+VRHN)/SUMRN	PKN 32-30 = "110"	
KVN32	VREG1OUT - Δ V*(VRN0+75R+VRHN)/SUMRN	PKN 32-30 = "111"	
KVN33	VREG1OUT - Δ V*(VRN0+80R+VRHN)/SUMRN	PKN 42-40 = "000"	VINN5
KVN34	VREG1OUT - Δ V*(VRN0+81R+VRHN)/SUMRN	PKN 42-40 = "001"	
KVN35	VREG1OUT - Δ V*(VRN0+82R+VRHN)/SUMRN	PKN 42-40 = "010"	
KVN36	VREG1OUT - Δ V*(VRN0+83R+VRHN)/SUMRN	PKN 42-40 = "011"	
KVN37	VREG1OUT - Δ V*(VRN0+84R+VRHN)/SUMRN	PKN 42-40 = "100"	
KVN38	VREG1OUT - Δ V*(VRN0+85R+VRHN)/SUMRN	PKN 42-40 = "101"	
KVN39	VREG1OUT - Δ V*(VRN0+86R+VRHN)/SUMRN	PKN 42-40 = "110"	
KVN40	VREG1OUT - Δ V*(VRN0+87R+VRHN)/SUMRN	PKN 42-40 = "111"	
KVN41	VREG1OUT - Δ V*(VRN0+87R+VRHN+VRLN)/SUMRN	PKN 52-50 = "000"	VINN6
KVN42	VREG1OUT - Δ V*(VRN0+91R+VRHN+VRLN)/SUMRN	PKN 52-50 = "001"	
KVN43	VREG1OUT - Δ V*(VRN0+95R+VRHN+VRLN)/SUMRN	PKN 52-50 = "010"	
KVN44	VREG1OUT - Δ V*(VRN0+99R+VRHN+VRLN)/SUMRN	PKN 52-50 = "011"	
KVN45	VREG1OUT - Δ V*(VRN0+103R+VRHN+VRLN)/SUMRN	PKN 52-50 = "100"	
KVN46	VREG1OUT - Δ V*(VRN0+107R+VRHN+VRLN)/SUMRN	PKN 52-50 = "101"	
KVN47	VREG1OUT - Δ V*(VRN0+111R+VRHN+VRLN)/SUMRN	PKN 52-50 = "110"	
KVN48	VREG1OUT - Δ V*(VRN0+115R+VRHN+VRLN)/SUMRN	PKN 52-50 = "111"	
KVN49	VREG1OUT - Δ V*(VRN0+120R+VRHN+VRLN)/SUMRN	-	VINN7

SUMRP : Sum of positive ladder resistors = 128R+VRHP+VRLP+VRP0+VRP1
SUMRN : Sum of negative ladder resistors = 128R+VRHN+VRLN+VRN0+VRN1
ΔV: Voltage difference between VREG1OUT and VGS

Grayscale voltage calculating formulae (Negative polarity)

Table 51

Grayscale	Formula
V0	VINN0
V1	VINN1
V2	V1-(V1-V8)*(9/24)
V3	V1-(V1-V8)*(12.5/24)
V4	V1-(V1-V8)*(16/24)
V5	V1-(V1-V8)*(18/24)
V6	V1-(V1-V8)*(20/24)
V7	V1-(V1-V8)*(22/24)
V8	VINN2
V9	V8-(V8-V12)*6/24
V10	V8-(V8-V12)*12/24
V11	V8-(V8-V12)*18/24
V12	V8-(V8-V20)*8/24
V13	V12-(V12-V16)*6/24
V14	V12-(V12-V16)*12/24
V15	V12-(V12-V16)*18/24
V16	V8-(V8-V20)*16/24
V17	V16-(V16-V20)*6/24
V18	V16-(V16-V20)*12/24
V19	V16-(V16-V20)*18/24
V20	VINN3
V21	V20-(V20-V26)*4/24
V22	V20-(V20-V26)*8/24
V23	V20-(V20-V26)*12/24
V24	V20-(V20-V26)*16/24
V25	V20-(V20-V26)*20/24
V26	V20-(V20-V43)*6/24
V27	V26-(V26-v3132)*4/24
V28	V26-(V26-v3132)*8/24
V29	V26-(V26-v3132)*12/24
V30	V26-(V26-v3132)*16/24
V31	V26-(V26-v3132)*20/24

∴v3132=V20-(V20-V43)*12/24

Grayscale	Formula
V32	v3132-(v3132-V37)*4/24
V33	v3132-(v3132-V37)*8/24
V34	v3132-(v3132-V37)*12/24
V35	v3132-(v3132-V37)*16/24
V36	v3132-(v3132-V37)*20/24
V37	V20-(V20-V43)*18/24
V38	V37-(V37-V43)*4/24
V39	V37-(V37-V43)*8/24
V40	V37-(V37-V43)*12/24
V41	V37-(V37-V43)*16/24
V42	V37-(V37-V43)*20/24
V43	VINN4
V44	V43-(V43-V47)*6/24
V45	V43-(V43-V47)*12/24
V46	V43-(V43-V47)*18/24
V47	V43-(V43-V55)*8/24
V48	V47-(V47-V51)*6/24
V49	V47-(V47-V51)*12/24
V50	V47-(V47-V51)*18/24
V51	V43-(V43-V55)*16/24
V52	V51-(V51-V55)*6/24
V53	V51-(V51-V55)*12/24
V54	V51-(V51-V55)*18/24
V55	VINN5
V56	V55-(V55-V62)*2/24
V57	V55-(V55-V62)*4/24
V58	V55-(V55-V62)*6/24
V59	V55-(V55-V62)*8/24
V60	V55-(V55-V62)*11.5/24
V61	V55-(V55-V62)*15/24
V62	VINN6
V63	VINN7

Note: Make sure the following relationship:
DDVDH-V0>0.5V
DDVDH-V8>1.1V

I/O level relation

The relationship between the data for each grayscale and its output level is as follows.

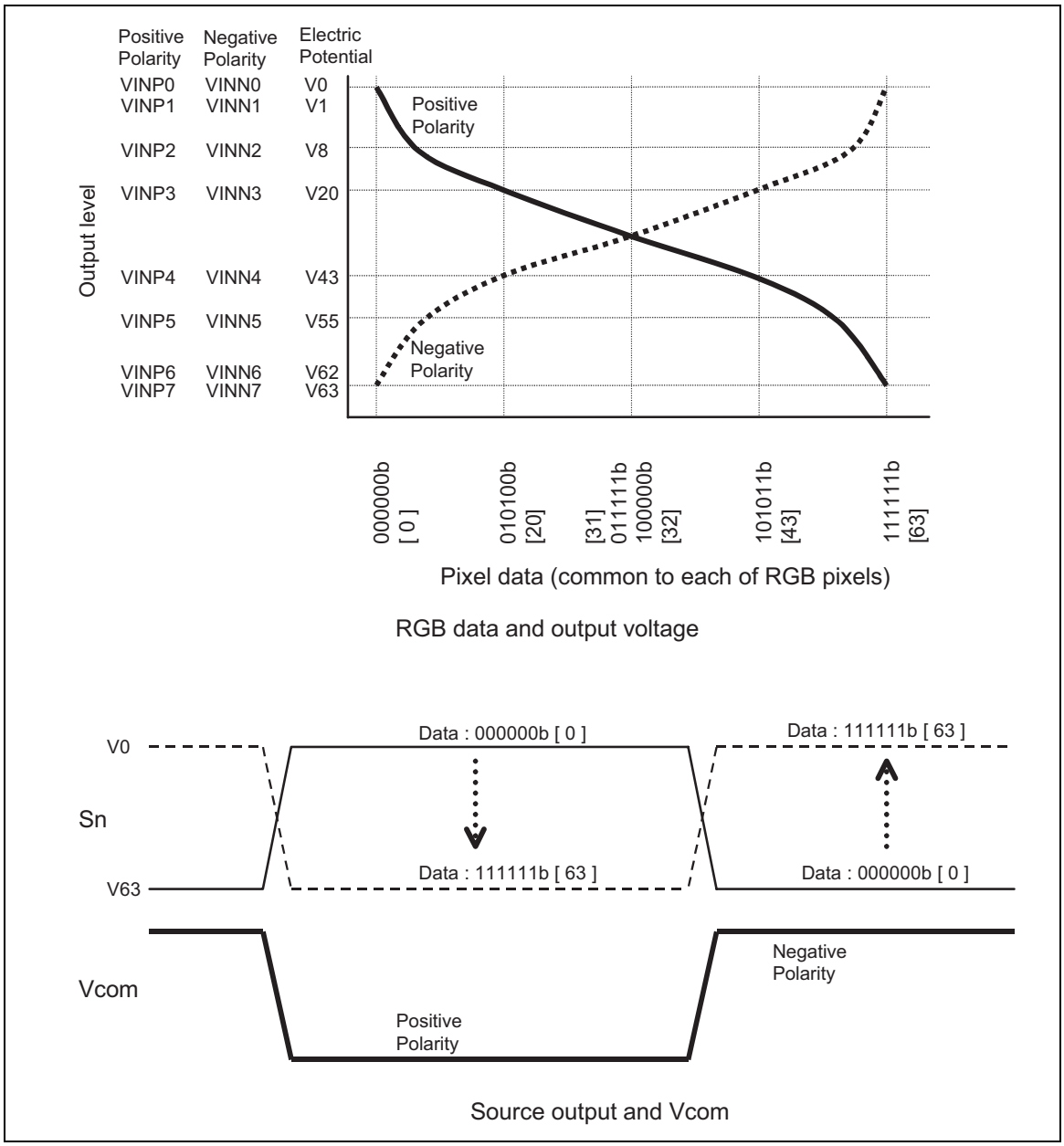


Figure 22

System configuration example

System example: 240(horizontal) x 320(vertical) pixels, using SPI

The following is an example of a module of TFT LCD panel incorporating a gate driver, using the HD66790.

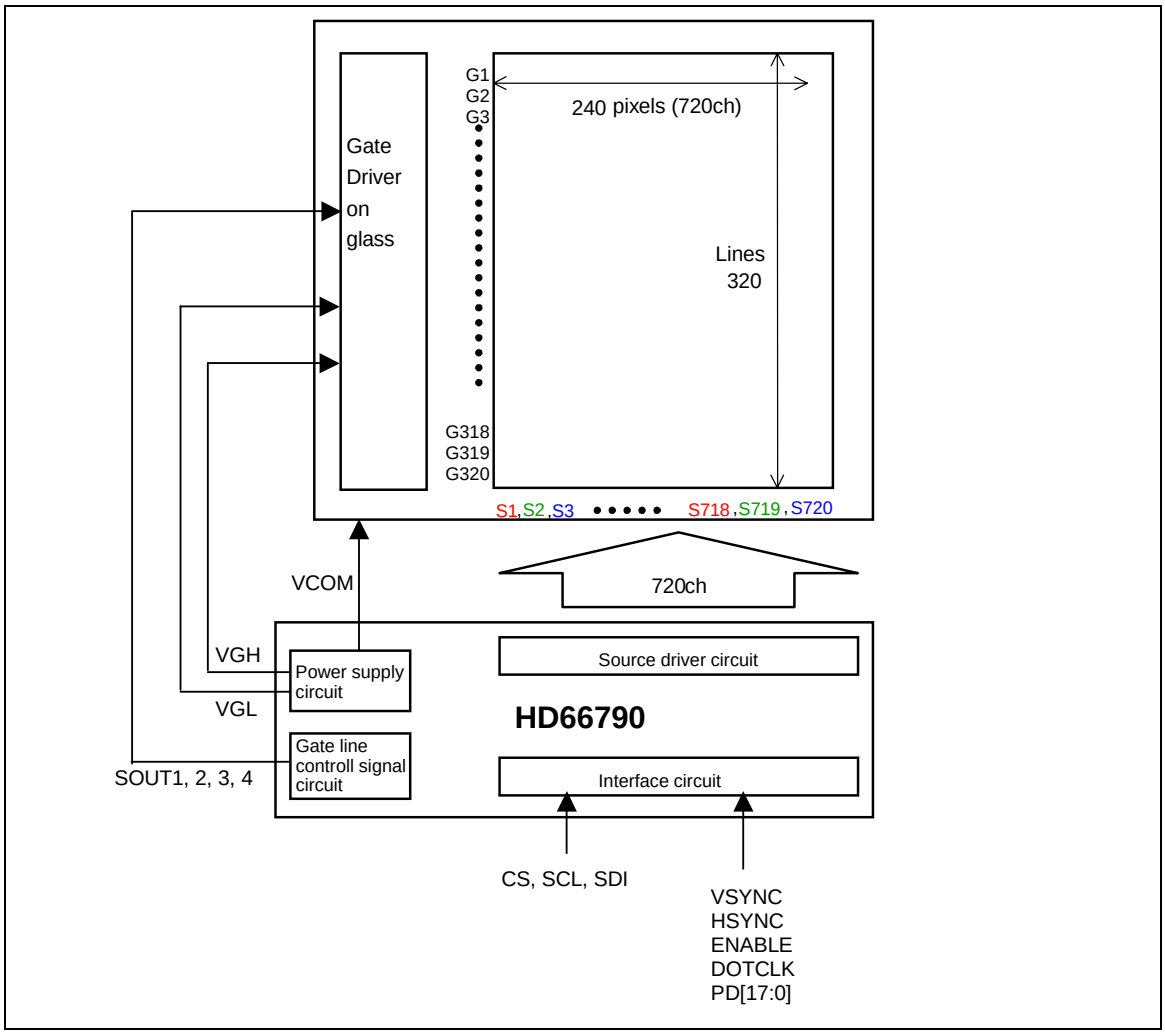


Figure 23

Voltage Setting Pattern Diagram

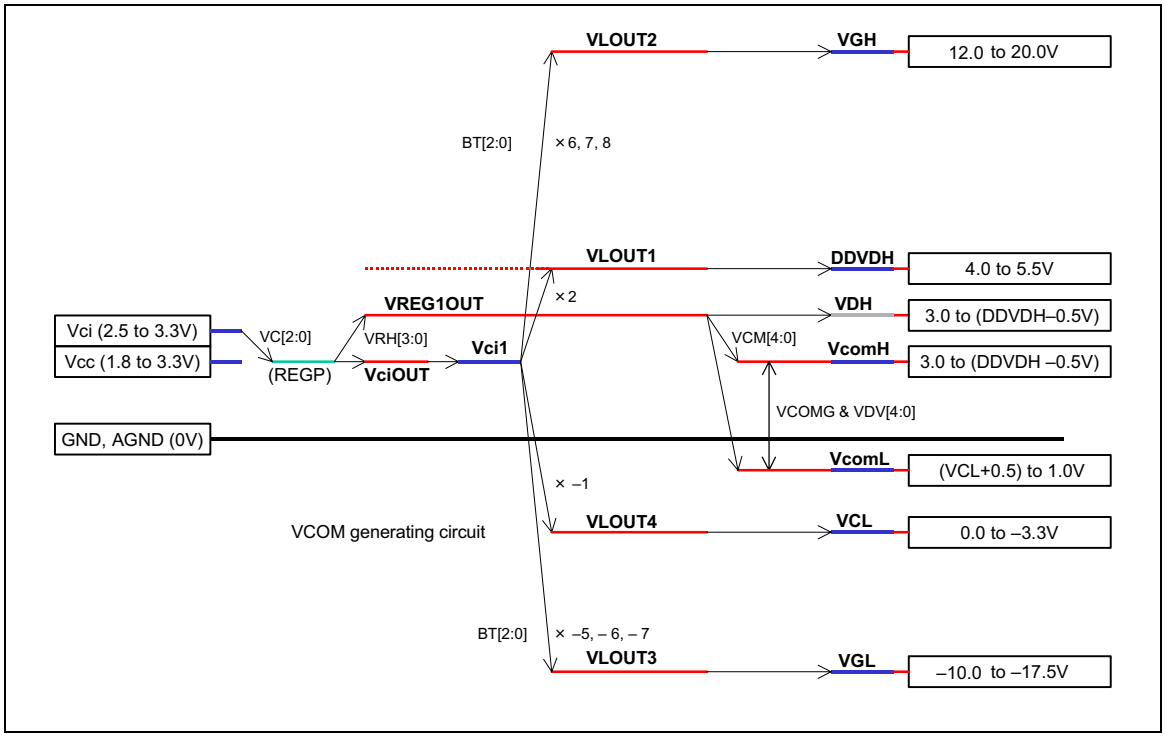


Figure 24

Internal state transition of the HD66790

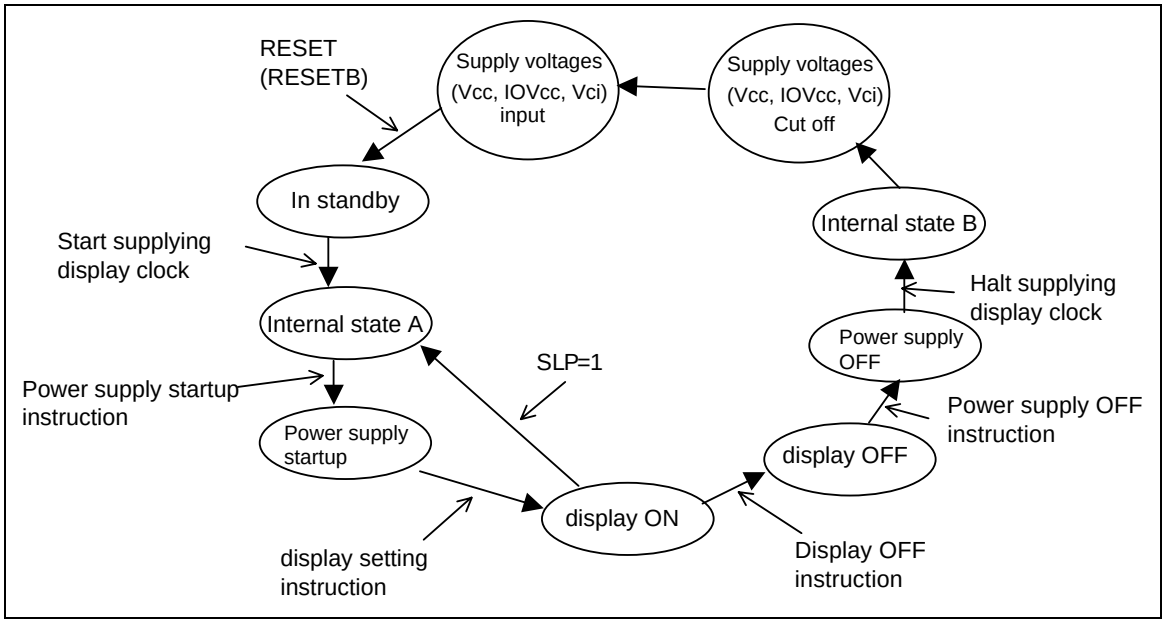
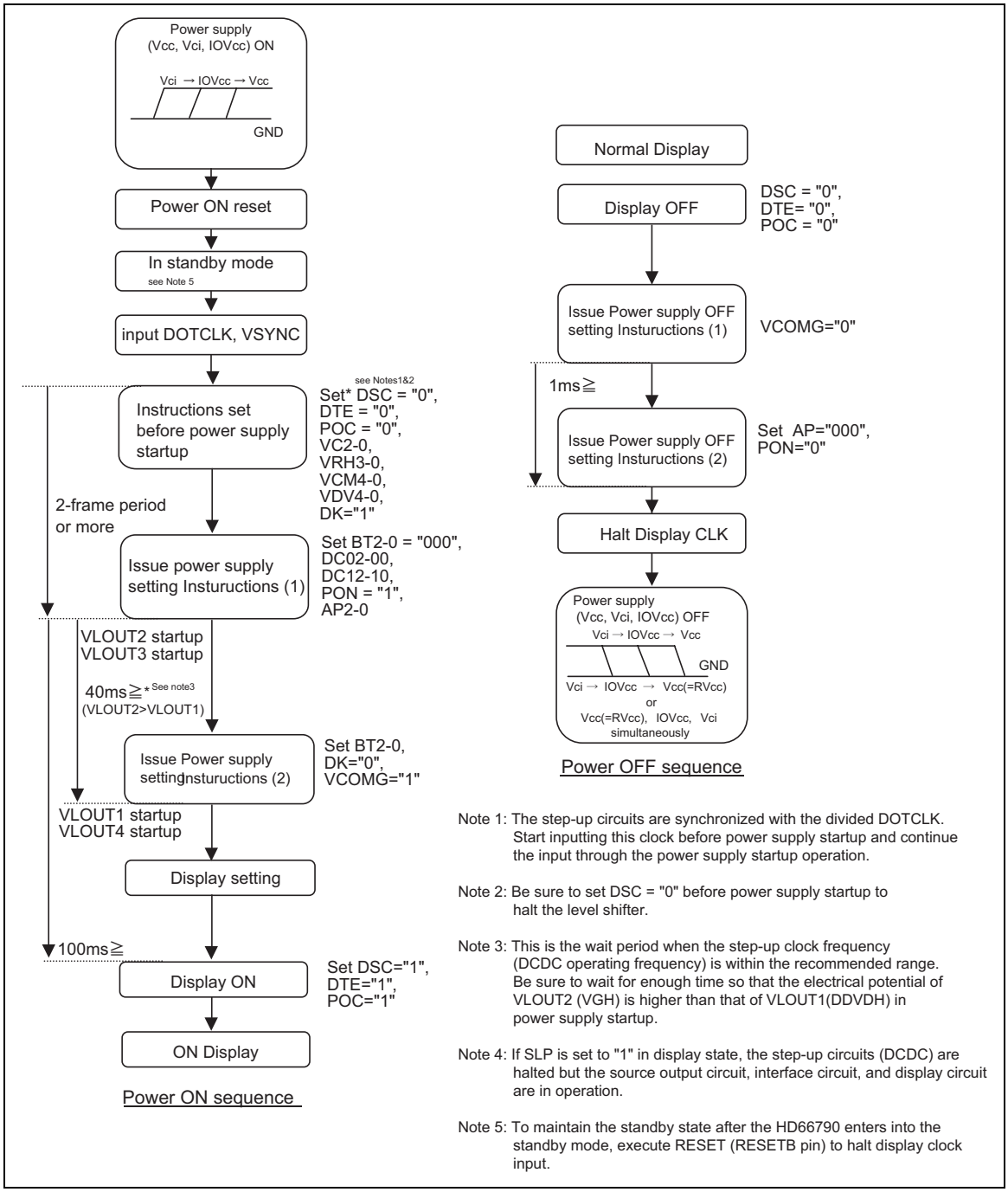


Figure 25

Power Supply Setting

When supplying and cutting off the power, follow the sequences below. The setting time for step-up circuits and operational amplifiers depends on external resistance and capacitance.



Note 1: The step-up circuits are synchronized with the divided DOTCLK. Start inputting this clock before power supply startup and continue the input through the power supply startup operation.

Note 2: Be sure to set DSC = "0" before power supply startup to halt the level shifter.

Note 3: This is the wait period when the step-up clock frequency (DCDC operating frequency) is within the recommended range. Be sure to wait for enough time so that the electrical potential of VLOUT2 (VGH) is higher than that of VLOUT1(DDVDH) in power supply startup.

Note 4: If SLP is set to "1" in display state, the step-up circuits (DCDC) are halted but the source output circuit, interface circuit, and display circuit are in operation.

Note 5: To maintain the standby state after the HD66790 enters into the standby mode, execute RESET (RESETB pin) to halt display clock input.

Figure 26

Absolute Maximum Ratings

Table 52

Item	Symbol	Unit	Rated value	Notes
Power supply voltage (1)	Vcc-GND	V	- 0.3 ~ + 4.3	(1), (2)
Power supply voltage (2)	IOVcc-GND	V	- 0.3 ~ + 4.3	(1), (3)
Power supply voltage (3)	Vci-AGND	V	- 0.3 ~ + 4.3	(1), (4)
Power supply voltage (4)	DDVDH-AGND	V	- 0.3 ~ + 6.0	(1), (5)
Power supply voltage (5)	AGND-VCL	V	- 0.3 ~ + 4.3	(1)
Power supply voltage (6)	DDVDH-VCL	V	- 0.3 ~ + 9.0	(1), (6)
Power supply voltage (7)	VGH-AGND	V	- 0.3 ~ + 22.0	(1), (7)
Power supply voltage (8)	AGND-VGL	V	- 0.3 ~ - 18.5	(1), (8)
Input/output voltage	V_t	V	- 0.3 ~ Vcc + 0.3	(1)
Operating temperature	Topr	ºC	- 40 ~ + 85	(1), (9)
Storage temperature	Tstg	ºC	- 55 ~ + 110	(1)

Note 1) If used beyond the absolute maximum ratings, the LSI may permanently be damaged. It is strongly recommended to use the LSI at a condition within the electrical characteristics in normal operation. Exposure to a condition not within the electrical characteristics may affect device reliability.

Note 2) Make sure Vcc (High) ≥ GND (Low).

Note 3) Make sure IOVcc (High) ≥ GND (Low).

Note 4) Make sure Vci (High) ≥ AGND (Low).

Note 5) Make sure DDVDH (High) ≥ AGND (Low).

Note 6) Make sure DDVDH (High) ≥ VCL (Low).

Note 7) Make sure VGH (High) ≥ AGND (Low).

Note 8) Make sure AGND (High) ≥ VGL (Low).

Note 9) The DC/AC characteristics of die and wafer products is guaranteed at 85 ºC.

Capacitance

Ta = - 25ºC, Vcc = 3.3V ± 0.3V

Table 53

Parameter	Symbol	Typ.	Max.	Unit	Notes
Input capacitance	C_{I1}	-	20	pF	1
Input capacitance	C_{I2}	-	20	pF	1

Note 1: The capacitance measured with a Booton Meter or by other equivalent methods and when CAS = V_{IH} so that Dout is not selected.

DC Operating Condition

Table 54

Parameter	Symbol	Min	Typ	Max	Unit	Note
Logic supply voltage	Vcc	2.5	3.0	3.6	V	1, 2
Analog supply voltage	V_{CI}	2.5	3.0	3.6	V	1
Interface supply voltage	IOVcc	1.65	3.0	3.6	V	1
Source driver supply voltage	V_{DDVDH}	3.5	-	5.5	V	1, 2
Supply voltage for level shifter output “high” level	V_{GH}	8.0	-	20.0	V	1, 2
Supply voltage for level shifter output “low” level	V_{GL}	-17.5	-	-4.0	V	1
Supply voltage for Vcom amplitude	V_{COMR}	0.0	-	V_{DDVDH} -0.3	V	1, 2

Note 1: All above voltages are measured with either GND or AGND level as the reference level.

Note 2: Make sure the relationship of the electrical potentials of the following voltages: $V_{GH} > V_{DDVDH} > V_{cc}$.

Electrical characteristics

DC characteristics

Ta = -40ºC ~ +85ºC, IOVcc = 1.65V ~ 3.6 V, Vcc = Vci = 2.5 ~ 3.6V* see Note 1

Table 55

Items		Symbol	Min.	typ.	Max.	Unit	Test Condition	Notes
Input “High” level voltage		V_{IH}	0.7 IOVcc	—	IOVcc	V		2, 3
Input “Low” level voltage		V_{IL}	0	—	0.3 IOVcc	V		2, 3
Output “High” level voltage		V_{OH}	0.7 IOVcc	—	—	V	I_{OH} = -0.1mA	2
Output “Low” level voltage		V_{OL}	—	—	0.15 IOVcc	V	I_{OL} = 0.1mA	2
Input/output leak current		I_{LO}	-5	—	5	μA	V_{IN} = 0 ~ IOVcc	4
Current Consumption (Normal operation mode)	Vcc-GND	I_{Vcc}	—	0.45	0.6	mA	Vcc=Vci=IOVcc= 2.8V, BT; x7, x-5, DC0: 1/256, DC1: 1/1024 fDOTCLK = 5MHz, 18-bit interface, Ta = 25ºC, AP = “001”, LSENL=”0”, LSENR=”1”	5, 6
	Vci-GND	I_{Vci}	—	4.7	6	mA		
Current Consumption (Standby mode)	Vcc-GND +Vci-GND	I_{stb}	—	2	10	μA	Vcc=Vci=IOVcc= 2.8V, Ta = 25ºC	5
Output voltage difference		ΔVo	—	±15	±25	mV	—	7
Average output voltage variance		ΔVΔ	—	±15	—	mV	—	8
Level Shifter ON resistance		R_{ON}	—	—	250	Ohm	VGH-VGL Iload=±500μA	9

Note 1: Refer to the corresponding numbers in “Note to electrical characteristics” for notes.

Note 2: The standby state is defined as that signal input pins are fixed to a certain level after a RESET input (RESETB = “0”). In standby mode, the internal state of the HD66790 can be described as static, in which all circuit operation, including power supply, source amplifiers, display, interface circuits, are halted.

Note 3: In standby mode, the source amplifiers are got started when a display clock is input into the HD66790, upon which the HD66790 exits the standby mode. While the HD66790 is in display operation, it cannot be got into the standby mode by setting SLP = “1” as long as the source amplifiers are in operation.

Step-up circuit output characteristics

Ta = -40ºC ~ +85ºC, IOVcc = 1.65V ~ 3.6V, Vcc=Vci= 2.5V ~ 3.6 V* see Note 1

Table 56

Items	Symbol	Min.	typ.	Max.	Unit	Test Condition	Notes
Step-up output voltage1	VLOUT1	4.85	4.9	—	V	IOVcc=Vcc=Vci=3.0V, fDOTCLk=5MHz, Ta=25ºC, Vci=VciOUT(directly input Vci externally), DC0="010", DC1="011", BT="101", AP="001", TMB="11", C11=C12=C21=C22=1uF/B, VLOUT1=VLOUT2=VLOUT3=VLOUT4=1uF/B, No panel load, Iload = -5mA	11
Step-up output voltage2	VLOUT2	15.5	16.2	—	V	IOVcc=Vcc=Vci=3.0V, fDOTCLk=5MHz, Ta=25ºC, Vci=VciOUT(directly input Vci externally), DC0="010", DC1="011", BT="101", AP="001", TMB="11", C11=C12=C21=C22=1uF/B, VLOUT1=VLOUT2=VLOUT3=VLOUT4=1uF/B, No panel load, Iload = -500uA	11
Step-up output voltage3	VLOUT3	-11.2	-11.9	—	V	IOVcc=Vcc=Vci=3.0V, fDOTCLk=5MHz, Ta=25ºC, Vci=VciOUT(directly input Vci externally), DC0="010", DC1="011", BT="101", AP="001", TMB="11", C11=C12=C21=C22=1uF/B, VLOUT1=VLOUT2=VLOUT3=VLOUT4=1uF/B, No panel load, Iload = +500uA	11
Step-up output voltage4	VLOUT4	-2.4	-2.6	—	V	IOVcc=Vcc=Vci=3.0V, fDOTCLk=5MHz, Ta=25ºC, Vci=VciOUT(directly input Vci externally), DC0="010", DC1="011", BT="101", AP="001", TMB="11", C11=C12=C21=C22=1uF/B, VLOUT1=VLOUT2=VLOUT3=VLOUT4=1uF/B, No panel load, Iload = +500uA	11
Input voltage	V_{CI}	2.5	—	3.6	V		11

Note: Refer to the corresponding numbers in "Note to electrical characteristics" for notes.

AC characteristics

Serial Peripheral Interface Timing Characteristics

Ta = -40ºC ~ +85ºC, IOVcc = 1.65V ~ 3.6 V, Vcc = 2.5V ~ 3.6V* see Note 1

Table 57

Item	Symbol	Min	Typ	Max	Unit	Timing diagram
Serial clock cycle time	t_{SCYC}	0.2	—	40	μs	Figure 27
Serial clock “High” level pulse width	t_{SCH}	80	—	—	nS	Figure 27
Serial clock “Low” level pulse width	t_{SCL}	80	—	—	nS	Figure 27
Serial clock rising time	t_{scr}	—	—	40	nS	Figure 27
Serial clock falling time	t_{scf}	—	—	40	nS	Figure 27
Chip select setup time	t_{CSU}	40	—	—	nS	Figure 27
Chip select hold time	t_{CSH}	120	—	—	nS	Figure 27
Serial input data setup time	t_{SISU}	60	—	—	nS	Figure 27
Serial input data hold time	t_{SIH}	60	—	—	nS	Figure 27

Note 1: Refer to the corresponding number in “Note to electrical characteristics” for notes.
Note 2: Refer to the corresponding Figure in “Note to electrical characteristics” for timing diagram.

Reset Timing Characteristics

Ta = -40ºC ~ +85ºC, IOVcc = 1.65V ~ 3.6 V, Vcc = 2.5V ~ 3.6V* see Note 1

Table 58

Item	Symbol	Min	Typ	Max	Unit	Timing diagram
Reset “Low” level width	t_{RES}	1	—	—	ms	Figure 28
Reset startup time	t_{rRES}	—	—	10	μs	Figure 28
Reset exit delay time	t_{DRES}	—	—	500	μs	Figure 28

Note 1: Refer to the corresponding number in “Note to electrical characteristics” for notes.
Note 2: Refer to the corresponding Figure in “Note to electrical characteristics” for timing diagram.

18-bit RGB interface timing characteristics

Ta = -40ºC ~ +85ºC, IOVcc = 1.65V ~ 3.6 V, Vcc = 2.5V ~ 3.6V* see Note 1

Table 59

Item	Symbol	min.	typ.	max.	Unit	Timing diagram
VSYNC/HSYNC Setup time	t_{SYNCS}	20	—	—	nS	Figure 29
ENABLE Setup time	t_{ENS}	30	—	—	nS	Figure 29
ENABLE Hold time	t_{ENH}	30	—	—	nS	Figure 29
DOTCLK “Low” level pulse width	P_{WDL}	40	—	—	nS	Figure 29
DOTCLK “High” level pulse width	P_{WDH}	40	—	—	nS	Figure 29
DOTCLK cycle time	t_{CYCD}	100	—	—	nS	Figure 29
Data Setup time	t_{PDS}	30	—	—	nS	Figure 29
Data Hold time	t_{PDH}	30	—	—	nS	Figure 29
DOTCLK, VSYNC, HSYNC rise/fall time	t_{rgbr}, t_{rgbf}	—	—	25	nS	Figure 29

Note 1: Refer to the corresponding number in “Note to electrical characteristics” for notes.

Note 2: Refer to the corresponding Figure in “Note to electrical characteristics” for timing diagram.

16-bit RGB interface timing characteristics

Ta = -40ºC ~ +85ºC, IOVcc = 1.65V ~ less than 2.5V, Vcc = 2.5V ~ 3.6V* see Note 1

Table 60

Item	Symbol	min.	typ.	max.	Unit	Timing diagram
VSYNC/HSYNC Setup time	t_{SYNCS}	15	—	—	nS	Figure 29
ENABLE Setup time	t_{ENS}	18	—	—	nS	Figure 29
ENABLE Hold time	t_{ENH}	20	—	—	nS	Figure 29
DOTCLK “Low” level pulse width	P_{WDL}	24	—	—	nS	Figure 29
DOTCLK “High” level pulse width	P_{WDH}	24	—	—	nS	Figure 29
DOTCLK cycle time	t_{CYCD}	60	—	—	nS	Figure 29
Data Setup time	t_{PDS}	15	—	—	nS	Figure 29
Data Hold time	t_{PDH}	20	—	—	nS	Figure 29
DOTCLK, VSYNC, HSYNC rise/fall time	t_{rgbr}, t_{rgbf}	—	—	10	nS	Figure 29

Note 1: Refer to the corresponding number in “Note to electrical characteristics” for notes.

Note 2: Refer to the corresponding Figure in “Note to electrical characteristics” for timing diagram.

6-bit RGB interface timing characteristics

Ta = -40ºC ~ +85ºC, IOVcc = 2.5V ~ 3.6V, Vcc = 2.5V ~ 3.6V* see Note 1

Table 61

Item	Symbol	min.	typ.	max.	Unit	Timing diagram
VSYNC/HSYNC Setup time	t_{SYNCS}	15	—	—	nS	Figure 29
ENABLE Setup time	t_{ENS}	18	—	—	nS	Figure 29
ENABLE Hold time	t_{ENH}	20	—	—	nS	Figure 29
DOTCLK “Low” level pulse width	P_{WDL}	16	—	—	nS	Figure 29
DOTCLK “High” level pulse width	P_{WDH}	16	—	—	nS	Figure 29
DOTCLK cycle time	t_{CYCD}	40	—	—	nS	Figure 29
Data Setup time	t_{PDS}	15	—	—	nS	Figure 29
Data Hold time	t_{PDH}	20	—	—	nS	Figure 29
DOTCLK, VSYNC, HSYNC rise/fall time	t_{rgbr}, t_{rgbf}	—	—	10	nS	Figure 29

Note 1: Refer to the corresponding number in “Note to electrical characteristics” for notes.

Note 2: Refer to the corresponding Figure in “Note to electrical characteristics” for timing diagram.

LCD driver output characteristics

Table 62

Item	Symbol	min.	typ.	max.	Unit	Test Condition	Timing diagram	Note
Driver output delay time	t_{DD}	—	20	35	μs	Vcc = 3.0V, V_{DDVDH} = 5.0V, VGH = 8.0V, VGL = 0V, Ta = 25ºC, DOTCLK = 8MHz, Time to reach the target voltage level ±25mV from a same grayscale level at all source pins from Vcom polarity inversion timing Load resistance R = 10kΩ, Load capacity 50pF	Figure 30	10

Note 1: Refer to the corresponding number in “Note to electrical characteristics” for notes.

Note 2: Refer to the corresponding Figure in “Note to electrical characteristics” for timing diagram.

Timing diagram

Serial Peripheral Interface Operation

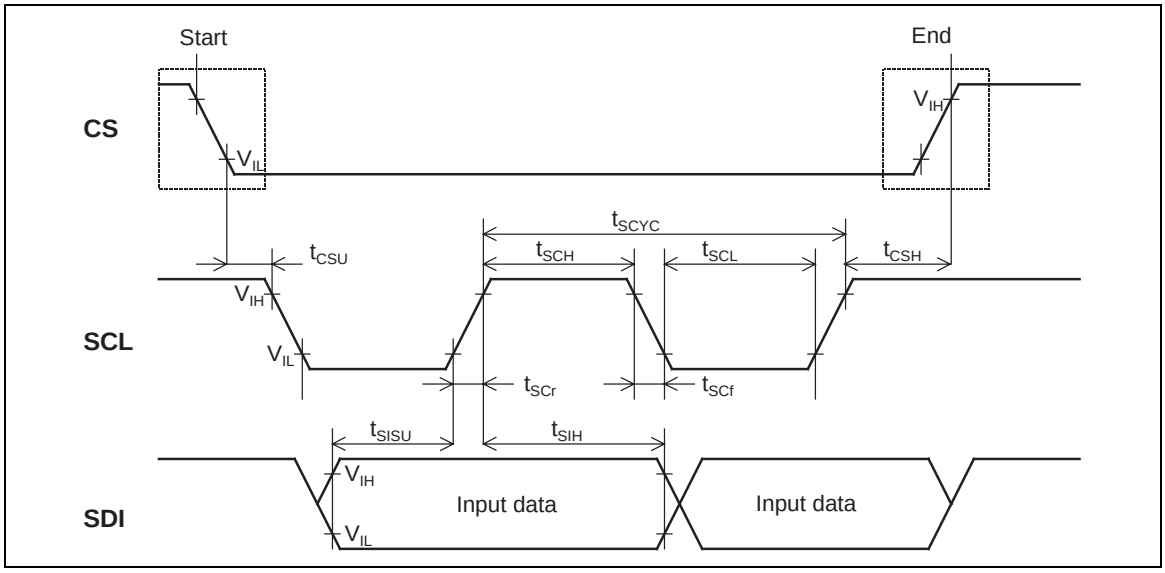


Figure 27

Reset Operation

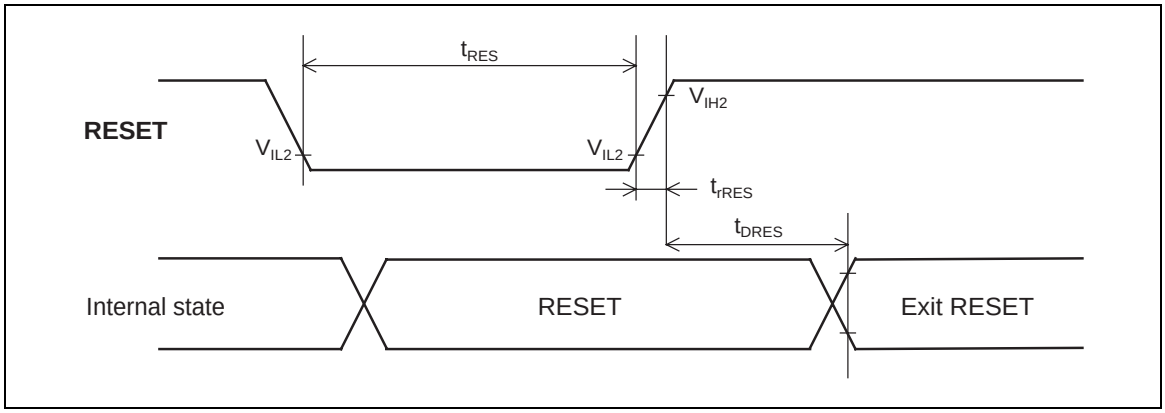


Figure 28

Interfacing Operation

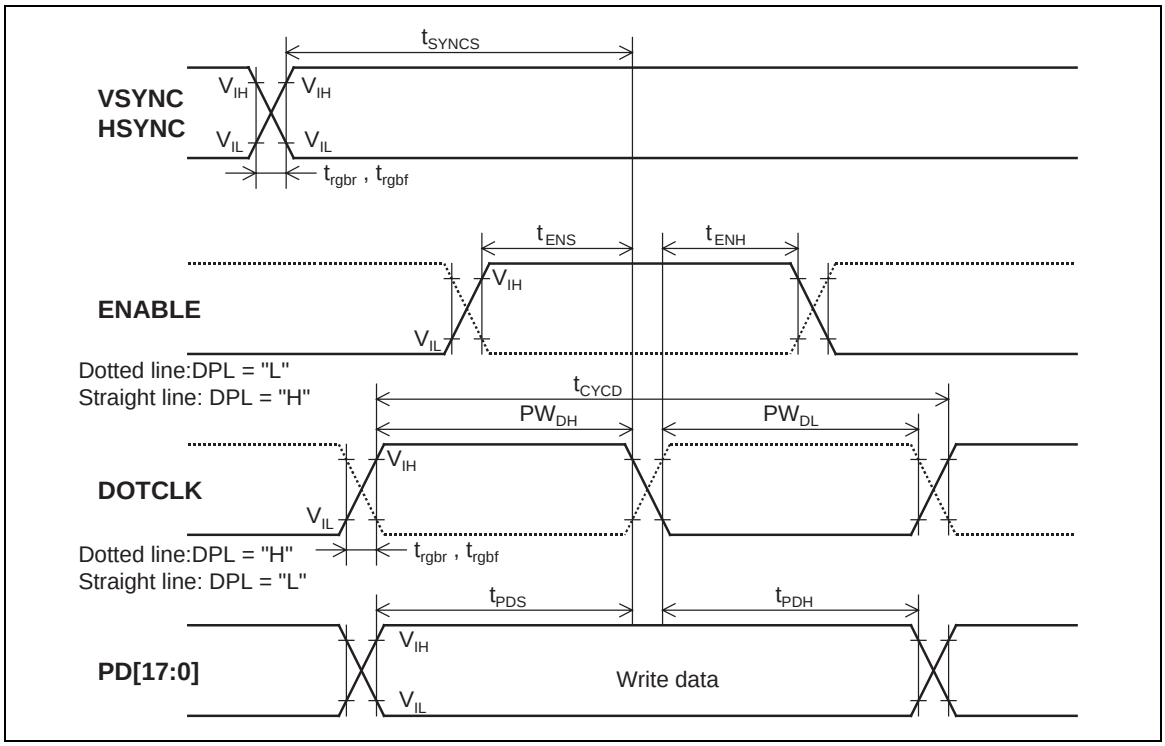


Figure 29

Switching Operation

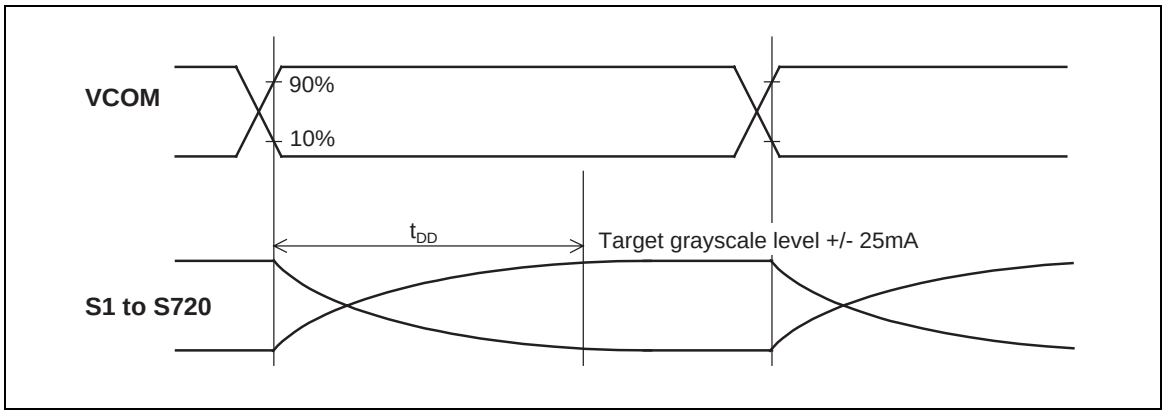


Figure 30

Notes to Electrical Characteristics

1. The DC/AC electrical characteristics of bare die and wafer products are guaranteed at 85°C.

2. The following are the configurations of inputs pin and output pins.

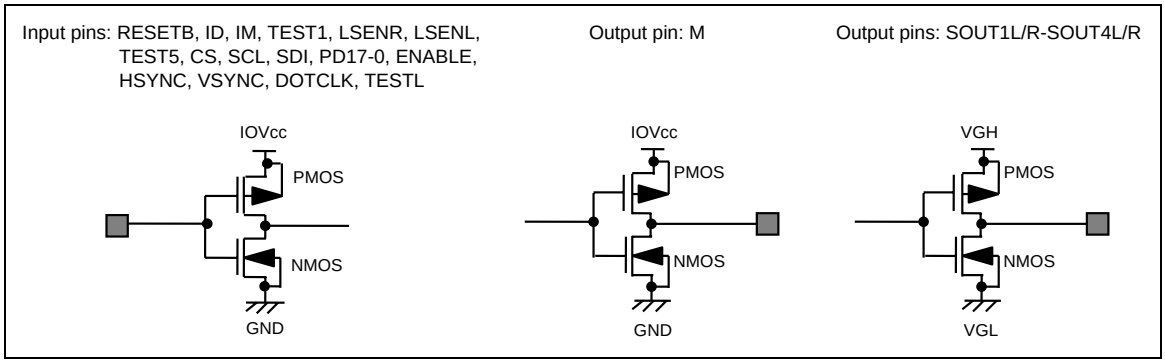


Figure 31

3. The TEST1, TEST5 and TESTL pins must be grounded (GND). The LSENR, LSENL, ID, IM pins must be fixed at either GND or the Vcc level.

4. This excludes currents through the output drive MOS.

5. This excludes currents flowing through input/output units. Make sure that input levels are fixed to prevent increase in the transient current in input units when a CMOS input level takes medium range. While not accessing via interface pins, current consumption will not change whether the CS* pin is set to "High" or "Low".

6. The relationships between the voltages and current consumption are as follows (reference data).

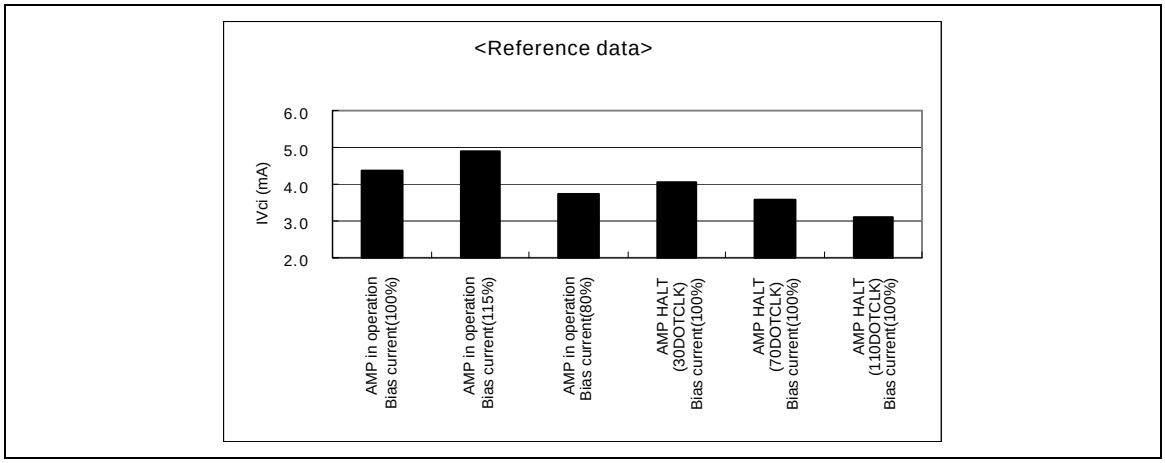


Figure 32

7. The output voltage difference is the difference in voltage levels of adjacent source output pins for a same grayscale. In off set cancel operation, this difference is within +/-10mV.

8. The average output voltage variance is the difference in average source output voltages of multiple chips of the same product. The average source output voltage is measured for each chip when all pins output the same grayscale. This value is just for reference.

9. In this test, an input level of amplitude VGH = 16.5V and VGL = -16.5 is applied externally. In this case, the voltage drop on each SOUT pin from externally input levels minus load current 500 μA is defined as ΔV, and ΔV/500(μA) is defined as the ON resistance of the buffer closest to the level shifter output. The following are reference data under the TYP. condition.

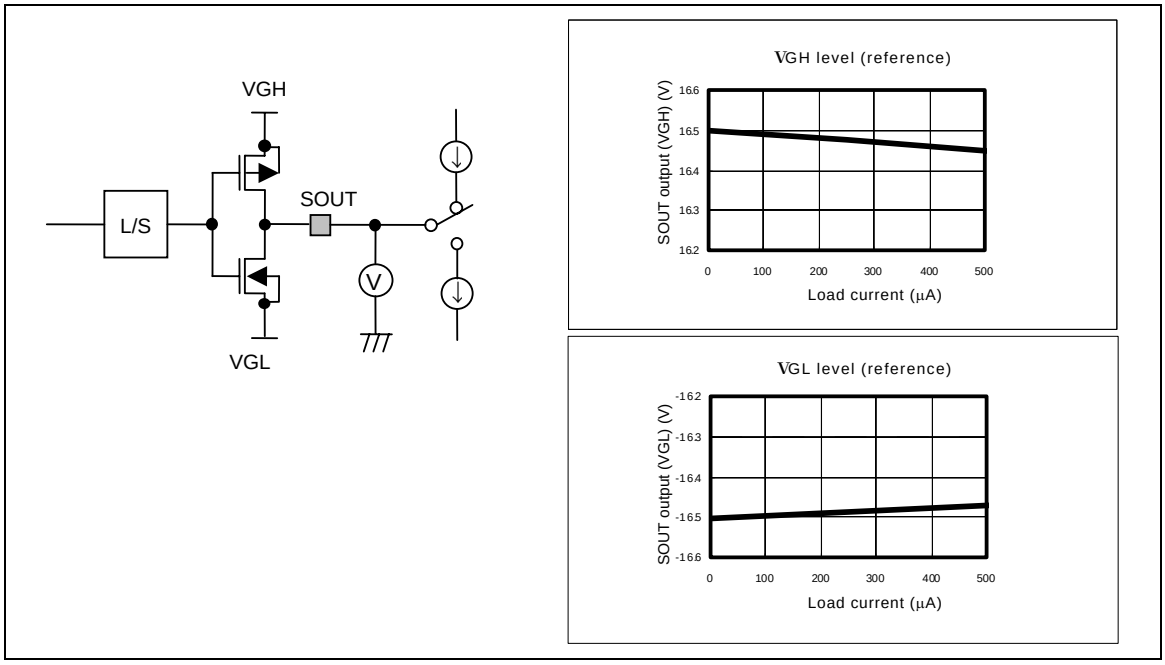


Figure 33

10. The LCD driver output delay time depends on the LCD panel load. Check the quality of display on the panel when setting a frame frequency and a cycle per line.

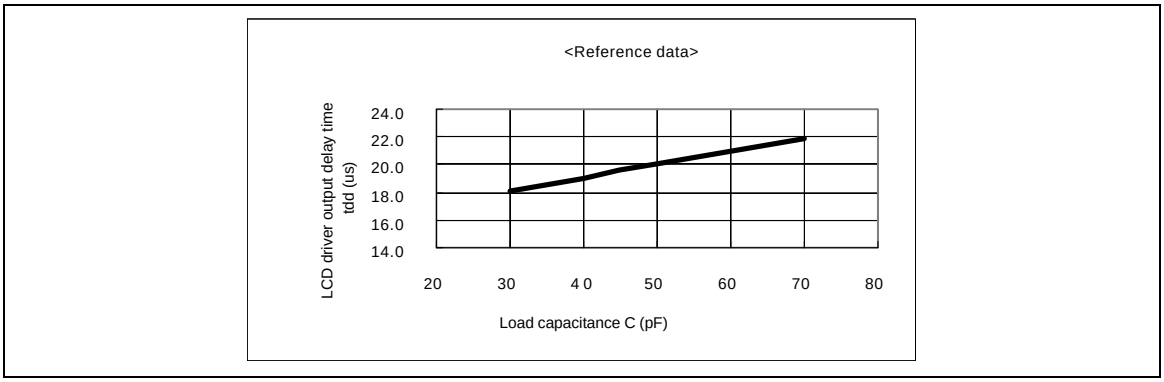


Figure 34

11. This does not include the wiring resistance when an LSI chip is mounted on glass, i.e. COG. No load is applied to pins except those being tested.

Example of test circuits

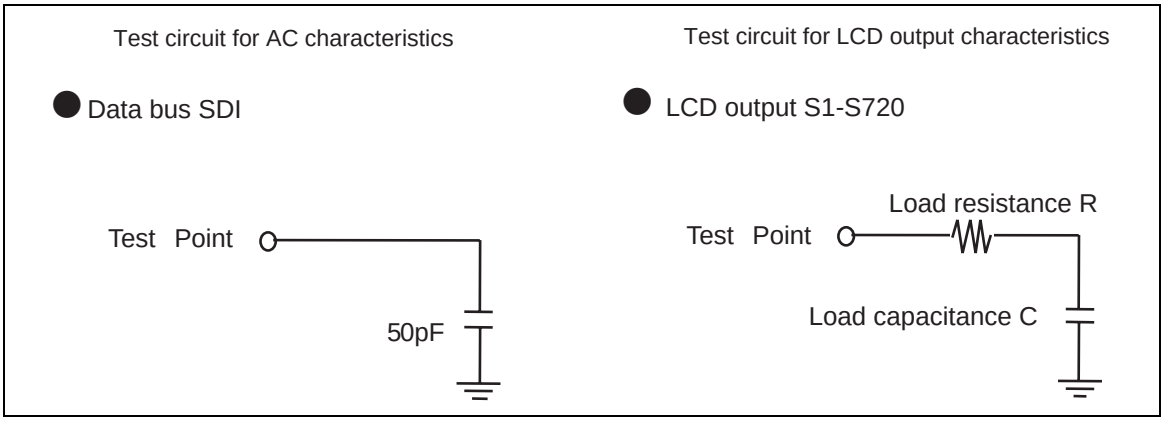


Figure 35

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http://www.renesas.com

Colophon 0.0

Revision Record

Rev.	Date	Page	Contents of Modification	Approved by
0.07	2003.9.26		First issue	
1.00	2004.05.26		Add Figure No., Table No.	
		5	Delete Built-in Vcom generating circuit	
			Add Vcom AC drive	
			Delete HWD667B90BP (product lineup)	
		6	Changes in Figure 1	
		20	Add wiring example	
		22	VciOUT, connected to: add “or Vci”	
		25	LSENL/R: Add “In consideration of current consumption increase and voltage drop, set LSENL/R = “L” if LSENR/L =”H”.”	
		26	DUMMYR: add description of function.	
		27	SLP: Change description	
		28	Table 7: Add (Default)	
			DC0[2:0]: Change description, Table 8	
		29	DC1[2:0]: Change description, Table 9	
		30~31	Add “Note” to DC0/DC1	
		31	VC2-0: Add Set VC[2:0] to “000” when directly inputting the Vci level externally.	
		32	POC: Change description	
		33	VCM[4:0]: Change description	
		35	Error correction: VDV[4:0] Table 17	
		36	SDT[1:0]: Change description, Table 18	
		36, 37	Change descriptions EPL, DPL, HPL, VPL.	
		39	Error correction in Table 25	
		41	Change description of FGI[1:0], table 31	
		42	Change description: DSC	
		46, 47	Add “Low Power Mode (R26h) register”, Figure 9	
		48	Changes in Instruction List (according to changes in “Instruction” section)	
		52	Delete “VcomS”	
		61~65	Grayscale amplifier unit: add more description	
		66~69	Add Voltage calculating formulae	
		70	Error correction in Figure 22: [31]010100b	
		71	Change Figure 23 (System configuration example)	
		73	Add figure 25 (Internal state transition of the HD66790)	
		74	Change in figure 26 (Power supply ON/OFF sequences). Add Note 4 and 5.	
		77	Add Note 2 and 3 and changes to Table 55	

Rev.	Date	Page	Contents of Modification	Approved by
1.00	2004.05.26	79	Delete “Serial output data hold time (tSOH)” and “Serial output data delay time (tSOD)” from Table 57	
		80, 81	Change in Tables 60, 61	
		84~86	Add “Notes to electrical characteristics”	