Model Name : JE50-HR/SJV50-HR
Compal Project Name : P5WE0/P5WS0
File Name : LA-6901P

Compal Confidential

JE50-HR/SJV50-HR(P5WE0/P5WS0) M/B Schematics Document

Intel Sandy Bridge Processor with DDRIII + Cougar Point PCH
Nvidia N12P GS/GV

2011-02-08

REV:2.0

Security Classification	Compal Secret Data		Compal Electronics, Inc.
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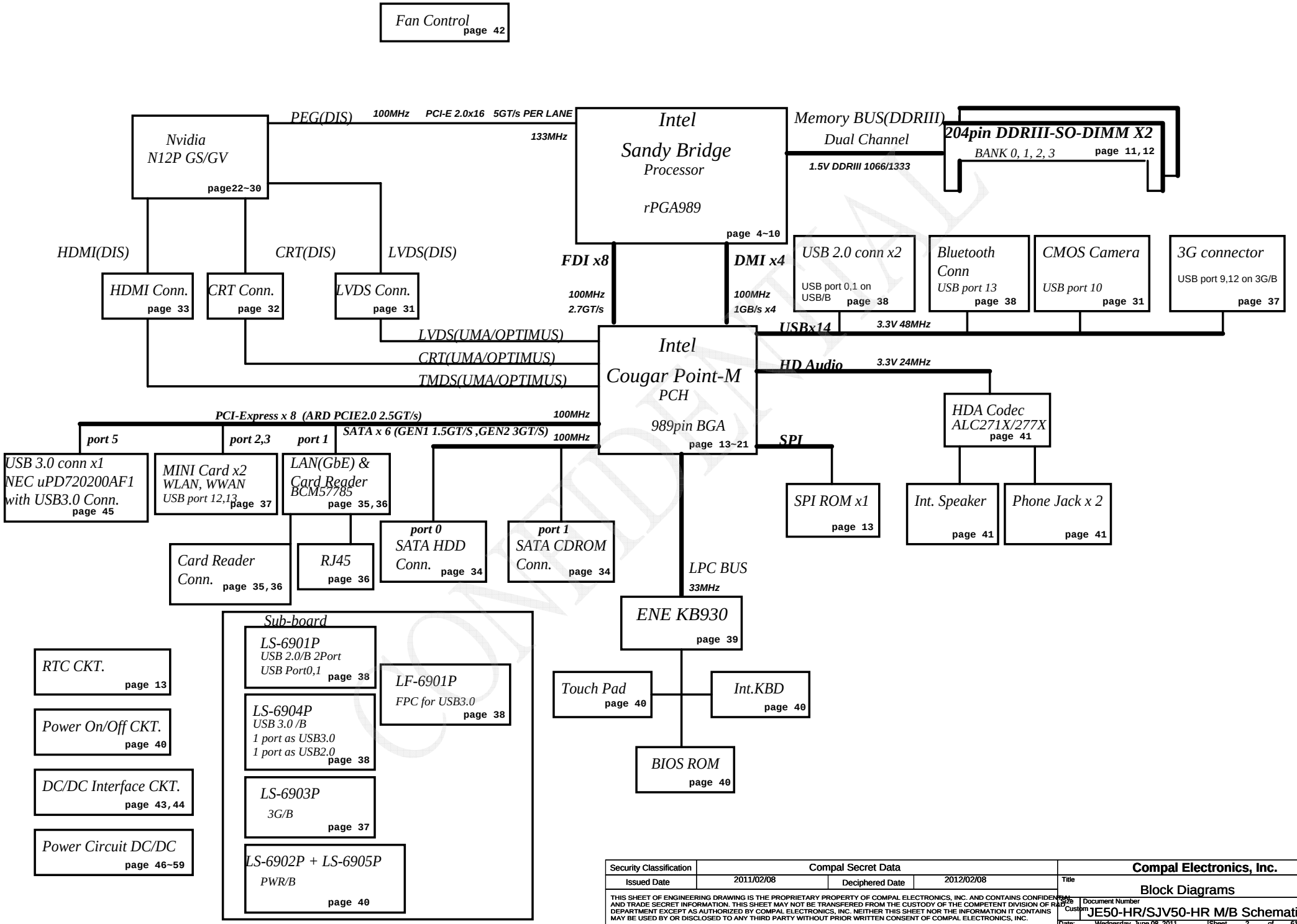
Date: Wednesday, June 08, 2011	Sheet 1 of 61		



Security Classification	Compal Secret Data		
Issued Date	2011/02/08	Deciphered Date	2012/02/08

Compal Electronics, Inc.	
Title	Block Diagrams
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Rev: E	
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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF
+VGFX_CORE	Core voltage for UMA graphic	ON	OFF	OFF
+0.75VS	+0.75VP to +0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.05VSDGPU	+1.0VSPDGPU to +1.0VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.05VS_VTT	+1.05VS_VCCPP to +1.05VS_VCCP switched power rail for CPU	ON	OFF	OFF
+1.05VS_PCH	+1.05VS_VCCP to +1.05VS_PCH power for PCH	ON	OFF	OFF
+1.5V	+1.5VP to +1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	+1.5V to +1.5VS switched power rail	ON	OFF	OFF
+1.5VSDGPU	+1.5VS to +1.5VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.8VS	(+5VALW or +3VALW) to 1.8V switched power rail to PCH & GPU	ON	OFF	OFF
+1.8VSDGPU	+1.8VS to +1.8VSDGPU switched power rail for GPU	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+3VALW_EC	+3VALW always to KBC	ON	ON	ON*
+3V_LAN	+3VALW to +3V_LAN power rail for LAN	ON	ON	ON*
+3VALW_PCH	+3VALW to +3VALW_PCH power rail for PCH (Short Jumper)	ON	ON	ON*
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5VALW_PCH	+5VALW to +5VALW_PCH power rail for PCH (Short resister)	ON	ON	ON*
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+VSB	+VSBP to +VSB always on power rail for sequence control	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address

PCH SM Bus address

Device	Address
Clock Generator (9LVS3199AKLFT, RTM890N-631-VB-GRT)	1101 0010b
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

3G & BT & USB30 & USB20 Config

3G SKU: 3G@ **USB30 SKU:** USB30@ **OPTMIUS SKU:** OPT@
BT SKU: BT@ **USB20 SKU:** USB20@ **Non-OPTMIUS SKU:** NOPT@
LAN Chip A0 version: A0@ **N12P-GS:** GS@
LAN chip B0 Version: B0@ **N12P-GV:** GV@

BOM Config

UMA Only: BT@/3G@/USB30@/UMA@/UMAO@/NOPT@/A0@
OPTIMUS(N12P-GS): BT@/3G@/USB30@/UMA@/DIS@/X76@/OPT@/A0@/GS@
DIS Only(N12P-GS): BT@/3G@/USB30@/DISO@/DIS@/X76@/NOPT@/A0@/GS@
OPTIMUS(N12P-GV): BT@/3G@/USB30@/UMA@/DIS@/X76@/OPT@/A0@/GV@
DIS Only(N12P-GV): BT@/3G@/USB30@/DISO@/DIS@/X76@/NOPT@/A0@/GV@

VRAM P/N :
64*16
Samsung : SA000035700
Hynix : SA000032400/SA0000324C0
128*16
Samsung : SA00003MQ40
Hynix : SA00003VS00

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	
0	0	0 V	0 V	0 V	EVT
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	EVT2
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	DVT
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	PVT
4	56K +/- 5%	1.036 V	1.185 V	1.264 V	Pre-MP
5	100K +/- 5%	1.453 V	1.650 V	1.759 V	
6	200K +/- 5%	1.935 V	2.200 V	2.341 V	
7	NC	2.500 V	3.300 V	3.300 V	

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	0.4
4	1.0
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure
UMA Only	UMAO@
UMA with OPTIMUS	UMA@
Dis with OPTIMUS	DIS@
DIS Only	DISO@
OPTIMUS	OPT@
Non-OPTIMUS	NOPT@
3G	3G@
Blue Tooth	BT@
USB2.0	USB20@
USB3.0	USB30@
VRAM	X76@
Connector	CONN@
Unpop	@
LAN Chip A0 version	A0@
LAN Chip B0 version	B0@
N12P-GS	GS@
N12P-GV	GV@

USB Port Table

USB 2.0	USB 1.1	Port	3 External USB Port
EHCI1	UHCI0	0	USB/B (Right Side)
		1	USB/B (Right Side)
	UHCI1	2	USB3.0 colay USB2.0 Conn.
		3	USB/B Colay USB3.0
	UHCI2	4	
		5	
	UHCI3	6	
		7	
EHCI2	UHCI4	8	Mini Card 1(WLAN)
		9	3G/B(WWAN)
	UHCI5	10	Camera
		11	Mini Card 2(Reserved)
	UHCI6	12	3G/B(SIM Card)
		13	BlueTooth

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ZZZ
DA60000KC10

PEG_ICOMPI and PEG_RCOMPO signals should be shorted and routed,
max length = 500 mils,trace width=4mils
PEG_ICOMPO signals should be routed with - max length = 500 mils,trace width=12mils
spacing =15mils

+1.05VS_VTT

R517
24.9_0402_1%

PEG_COMP

JCPU1A

PEG_ICOMPI J22
PEG_ICOMPO J21
PEG_RCOMPO H22

DMI

15 DMI_CRX_PTX_N0	B27	DMI_RX#[0]	
15 DMI_CRX_PTX_N1	B25	DMI_RX#[1]	
15 DMI_CRX_PTX_N2	A25	DMI_RX#[2]	
15 DMI_CRX_PTX_N3	B24	DMI_RX#[3]	
15 DMI_CRX_PTX_P0	B28	DMI_RX[0]	
15 DMI_CRX_PTX_P1	B26	DMI_RX[1]	
15 DMI_CRX_PTX_P2	A24	DMI_RX[2]	
15 DMI_CRX_PTX_P3	B23	DMI_RX[3]	
15 DMI_CTX_PRX_N0	G21	DMI_TX#[0]	
15 DMI_CTX_PRX_N1	F22	DMI_TX#[1]	
15 DMI_CTX_PRX_N2	F21	DMI_TX#[2]	
15 DMI_CTX_PRX_N3	D21	DMI_TX#[3]	
15 DMI_CTX_PRX_P0	G22	DMI_TX[0]	
15 DMI_CTX_PRX_P1	D22	DMI_TX[1]	
15 DMI_CTX_PRX_P2	F20	DMI_TX[2]	
15 DMI_CTX_PRX_P3	C21	DMI_TX[3]	

Intel(R) FDI

15 FDI_CTX_PRX_N0	A21	FDI0_TX#[0]
15 FDI_CTX_PRX_N1	H19	FDI0_TX#[1]
15 FDI_CTX_PRX_N2	E19	FDI0_TX#[2]
15 FDI_CTX_PRX_N3	F18	FDI0_TX#[3]
15 FDI_CTX_PRX_N4	B21	FDI1_TX#[0]
15 FDI_CTX_PRX_N5	C20	FDI1_TX#[1]
15 FDI_CTX_PRX_N6	D18	FDI1_TX#[2]
15 FDI_CTX_PRX_N7	E17	FDI1_TX#[3]
15 FDI_CTX_PRX_P0	A22	FDI0_TX[0]
15 FDI_CTX_PRX_P1	G19	FDI0_TX[1]
15 FDI_CTX_PRX_P2	E20	FDI0_TX[2]
15 FDI_CTX_PRX_P3	G18	FDI0_TX[3]
15 FDI_CTX_PRX_P4	B20	FDI1_TX[0]
15 FDI_CTX_PRX_P5	C19	FDI1_TX[1]
15 FDI_CTX_PRX_P6	D19	FDI1_TX[2]
15 FDI_CTX_PRX_P7	F17	FDI1_TX[3]
15 FDI_FSYNC0	J18	FDI0_FSYNC
15 FDI_FSYNC1	J17	FDI1_FSYNC
15 FDI_INT	H20	FDI_INT
15 FDI_LSYNC0	J19	FDI0_LSYNC
15 FDI_LSYNC1	H17	FDI1_LSYNC

+1.05VS_VTT

R145
24.9_0402_1%

EDP_COMP A18

eDP

	A17	eDP_COMPIO
		eDP_ICOMPO
	B16	eDP_HPD
C15		eDP_AUX
D15		eDP_AUX#
C17		eDP_TX[0]
F16		eDP_TX[1]
C16		eDP_TX[2]
G15		eDP_TX[3]
C18		eDP_TX#[0]
E16		eDP_TX#[1]
D16		eDP_TX#[2]
F15		eDP_TX#[3]

PCI EXPRESS* - GRAPHICS

PEG_RX#[0]	K33	PEG_GTX_C_HRX_N15	C46	1	2	DIS@ 0.22U 0402 10V6K PEG_GTX_HRX_N15
PEG_RX#[1]	M35	PEG_GTX_C_HRX_N14	C49	1	2	DIS@ 0.22U 0402 10V6K PEG_GTX_HRX_N14
PEG_RX#[2]	L34	PEG_GTX_C_HRX_N13	C51	1	2	DIS@ 0.22U 0402 10V6K PEG_GTX_HRX_N13
PEG_RX#[3]	J35	PEG_GTX_C_HRX_N12	C53	1	2	DIS@ 0.22U 0402 10V6K PEG_GTX_HRX_N12
PEG_RX#[4]	J32	PEG_GTX_C_HRX_N11	C60	1	2	DIS@ 0.22U 0402 10V6K PEG_GTX_HRX_N11
PEG_RX#[5]	H34	PEG_GTX_C_HRX_N10	C71	1	2	DIS@ 0.22U 0402 10V6K PEG_GTX_HRX_N10
PEG_RX#[6]	H31	PEG_GTX_C_HRX_N9	C75	1	2	DIS@ 0.22U 0402 10V6K PEG_GTX_HRX_N9
PEG_RX#[7]	G33	PEG_GTX_C_HRX_N8	C82	1	2	DIS@ 0.22U 0402 10V6K PEG_GTX_HRX_N8
PEG_RX#[8]	G30	PEG_GTX_C_HRX_N7	C92	1	2	DIS@ 0.22U 0402 10V6K PEG_GTX_HRX_N7
PEG_RX#[9]	E35	PEG_GTX_C_HRX_N6	C93	1	2	DIS@ 0.22U 0402 10V6K PEG_GTX_HRX_N6
PEG_RX#[10]	E34	PEG_GTX_C_HRX_N5	C102	1	2	DIS@ 0.22U 0402 10V6K PEG_GTX_HRX_N5
PEG_RX#[11]	E32	PEG_GTX_C_HRX_N4	C111	1	2	DIS@ 0.22U 0402 10V6K PEG_GTX_HRX_N4
PEG_RX#[12]	D33	PEG_GTX_C_HRX_N3	C113	1	2	DIS@ 0.22U 0402 10V6K PEG_GTX_HRX_N3
PEG_RX#[13]	D31	PEG_GTX_C_HRX_N2	C125	1	2	DIS@ 0.22U 0402 10V6K PEG_GTX_HRX_N2
PEG_RX#[14]	B33	PEG_GTX_C_HRX_N1	C129	1	2	DIS@ 0.22U 0402 10V6K PEG_GTX_HRX_N1
PEG_RX#[15]	C32	PEG_GTX_C_HRX_N0	C144	1	2	DIS@ 0.22U 0402 10V6K PEG_GTX_HRX_N0
PEG_RX[0]	J33	PEG_GTX_C_HRX_P15	C47	1	2	DIS@ 0.22U 0402 10V6K PEG_GTX_HRX_P15
PEG_RX[1]	L35	PEG_GTX_C_HRX_P14	C50	1	2	DIS@ 0.22U 0402 10V6K PEG_GTX_HRX_P14
PEG_RX[2]	K34	PEG_GTX_C_HRX_P13	C52	1	2	DIS@ 0.22U 0402 10V6K PEG_GTX_HRX_P13
PEG_RX[3]	H35	PEG_GTX_C_HRX_P12	C56	1	2	DIS@ 0.22U 0402 10V6K PEG_GTX_HRX_P12
PEG_RX[4]	H32	PEG_GTX_C_HRX_P11	C66	1	2	DIS@ 0.22U 0402 10V6K PEG_GTX_HRX_P11
PEG_RX[5]	G34	PEG_GTX_C_HRX_P10	C68	1	2	DIS@ 0.22U 0402 10V6K PEG_GTX_HRX_P10
PEG_RX[6]	G31	PEG_GTX_C_HRX_P9	C81	1	2	DIS@ 0.22U 0402 10V6K PEG_GTX_HRX_P9
PEG_RX[7]	E33	PEG_GTX_C_HRX_P8	C86	1	2	DIS@ 0.22U 0402 10V6K PEG_GTX_HRX_P8
PEG_RX[8]	E30	PEG_GTX_C_HRX_P7	C89	1	2	DIS@ 0.22U 0402 10V6K PEG_GTX_HRX_P7
PEG_RX[9]	E35	PEG_GTX_C_HRX_P6	C100	1	2	DIS@ 0.22U 0402 10V6K PEG_GTX_HRX_P6
PEG_RX[10]	E33	PEG_GTX_C_HRX_P5	C105	1	2	DIS@ 0.22U 0402 10V6K PEG_GTX_HRX_P5
PEG_RX[11]	E32	PEG_GTX_C_HRX_P4	C106	1	2	DIS@ 0.22U 0402 10V6K PEG_GTX_HRX_P4
PEG_RX[12]	D34	PEG_GTX_C_HRX_P3	C117	1	2	DIS@ 0.22U 0402 10V6K PEG_GTX_HRX_P3
PEG_RX[13]	E31	PEG_GTX_C_HRX_P2	C119	1	2	DIS@ 0.22U 0402 10V6K PEG_GTX_HRX_P2
PEG_RX[14]	C33	PEG_GTX_C_HRX_P1	C135	1	2	DIS@ 0.22U 0402 10V6K PEG_GTX_HRX_P1
PEG_RX[15]	B32	PEG_GTX_C_HRX_P0	C138	1	2	DIS@ 0.22U 0402 10V6K PEG_GTX_HRX_P0
PEG_TX#[0]	M29	PEG_HTX_GRX_N15	C516	1	2	DIS@ 0.22U 0402 10V6K PEG_HTX_C_GRX_N15
PEG_TX#[1]	M32	PEG_HTX_GRX_N14	C520	1	2	DIS@ 0.22U 0402 10V6K PEG_HTX_C_GRX_N14
PEG_TX#[2]	M31	PEG_HTX_GRX_N13	C529	1	2	DIS@ 0.22U 0402 10V6K PEG_HTX_C_GRX_N13
PEG_TX#[3]	L32	PEG_HTX_GRX_N12	C534	1	2	DIS@ 0.22U 0402 10V6K PEG_HTX_C_GRX_N12
PEG_TX#[4]	L29	PEG_HTX_GRX_N11	C538	1	2	DIS@ 0.22U 0402 10V6K PEG_HTX_C_GRX_N11
PEG_TX#[5]	K31	PEG_HTX_GRX_N10	C540	1	2	DIS@ 0.22U 0402 10V6K PEG_HTX_C_GRX_N10
PEG_TX#[6]	K28	PEG_HTX_GRX_N9	C542	1	2	DIS@ 0.22U 0402 10V6K PEG_HTX_C_GRX_N9
PEG_TX#[7]	J30	PEG_HTX_GRX_N8	C544	1	2	DIS@ 0.22U 0402 10V6K PEG_HTX_C_GRX_N8
PEG_TX#[8]	J28	PEG_HTX_GRX_N7	C546	1	2	DIS@ 0.22U 0402 10V6K PEG_HTX_C_GRX_N7
PEG_TX#[9]	H29	PEG_HTX_GRX_N6	C548	1	2	DIS@ 0.22U 0402 10V6K PEG_HTX_C_GRX_N6
PEG_TX#[10]	G27	PEG_HTX_GRX_N5	C550	1	2	DIS@ 0.22U 0402 10V6K PEG_HTX_C_GRX_N5
PEG_TX#[11]	E29	PEG_HTX_GRX_N4	C552	1	2	DIS@ 0.22U 0402 10V6K PEG_HTX_C_GRX_N4
PEG_TX#[12]	E27	PEG_HTX_GRX_N3	C554	1	2	DIS@ 0.22U 0402 10V6K PEG_HTX_C_GRX_N3
PEG_TX#[13]	D28	PEG_HTX_GRX_N2	C556	1	2	DIS@ 0.22U 0402 10V6K PEG_HTX_C_GRX_N2
PEG_TX#[14]	F26	PEG_HTX_GRX_N1	C558	1	2	DIS@ 0.22U 0402 10V6K PEG_HTX_C_GRX_N1
PEG_TX#[15]	E25	PEG_HTX_GRX_N0	C560	1	2	DIS@ 0.22U 0402 10V6K PEG_HTX_C_GRX_N0
PEG_TX[0]	M28	PEG_HTX_GRX_P15	C515	1	2	DIS@ 0.22U 0402 10V6K PEG_HTX_C_GRX_P15
PEG_TX[1]	M33	PEG_HTX_GRX_P14	C528	1	2	DIS@ 0.22U 0402 10V6K PEG_HTX_C_GRX_P14
PEG_TX[2]	M30	PEG_HTX_GRX_P13	C533	1	2	DIS@ 0.22U 0402 10V6K PEG_HTX_C_GRX_P13
PEG_TX[3]	L31	PEG_HTX_GRX_P12	C536	1	2	DIS@ 0.22U 0402 10V6K PEG_HTX_C_GRX_P12
PEG_TX[4]	L28	PEG_HTX_GRX_P11	C539	1	2	DIS@ 0.22U 0402 10V6K PEG_HTX_C_GRX_P11
PEG_TX[5]	K30	PEG_HTX_GRX_P10	C541	1	2	DIS@ 0.22U 0402 10V6K PEG_HTX_C_GRX_P10
PEG_TX[6]	K27	PEG_HTX_GRX_P9	C543	1	2	DIS@ 0.22U 0402 10V6K PEG_HTX_C_GRX_P9
PEG_TX[7]	J29	PEG_HTX_GRX_P8	C545	1	2	DIS@ 0.22U 0402 10V6K PEG_HTX_C_GRX_P8
PEG_TX[8]	J27	PEG_HTX_GRX_P7	C547	1	2	DIS@ 0.22U 0402 10V6K PEG_HTX_C_GRX_P7
PEG_TX[9]	H28	PEG_HTX_GRX_P6	C549	1	2	DIS@ 0.22U 0402 10V6K PEG_HTX_C_GRX_P6
PEG_TX[10]	G28	PEG_HTX_GRX_P5	C551	1	2	DIS@ 0.22U 0402 10V6K PEG_HTX_C_GRX_P5
PEG_TX[11]	F28	PEG_HTX_GRX_P4	C553	1	2	DIS@ 0.22U 0402 10V6K PEG_HTX_C_GRX_P4
PEG_TX[12]	F28	PEG_HTX_GRX_P3	C555	1	2	DIS@ 0.22U 0402 10V6K PEG_HTX_C_GRX_P3
PEG_TX[13]	D27	PEG_HTX_GRX_P2	C557	1	2	DIS@ 0.22U 0402 10V6K PEG_HTX_C_GRX_P2
PEG_TX[14]	F26	PEG_HTX_GRX_P1	C559	1	2	DIS@ 0.22U 0402 10V6K PEG_HTX_C_GRX_P1
PEG_TX[15]	D25	PEG_HTX_GRX_P0	C561	1	2	DIS@ 0.22U 0402 10V6K PEG_HTX_C_GRX_P0

PEG_GTX_HRX_N[0..15] 22
PEG_GTX_HRX_P[0..15] 22
PEG_HTX_C_GRX_N[0..15] 22
PEG_HTX_C_GRX_P[0..15] 22

Sandy Bridge_rPGA_Rev0p61
CONN@

eDP_COMPIO and ICOMPO signals should be shorted near balls,
Trace Width for EDP_COMPIO=4mils,
EDP_ICOMPO=12mils,
and both length less than 500 mils...
should not be left floating
,even if disable eDP function...

Typ- suggest 220nF. The change in AC capacitor value from 100nF to 220nF is to enable compatibility with future platforms having PCIE Gen3 (8GT/s)

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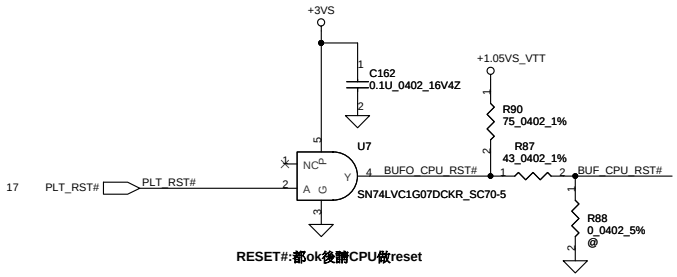
Issued Date	2011/02/08	Deciphered Date	2012/02/08

Title: **PROCESSOR(1/7) DMI,FDI,PEG**

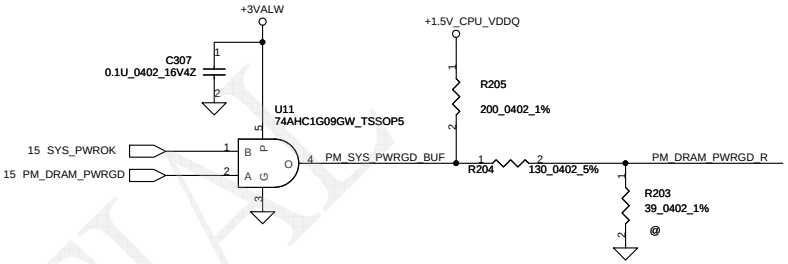
Size: Custom | Document Number: **JE50-HR/SJV50-HR M/B Schematics** | Rev: E

Date: Wednesday, June 08, 2011 | Sheet 4 of 61

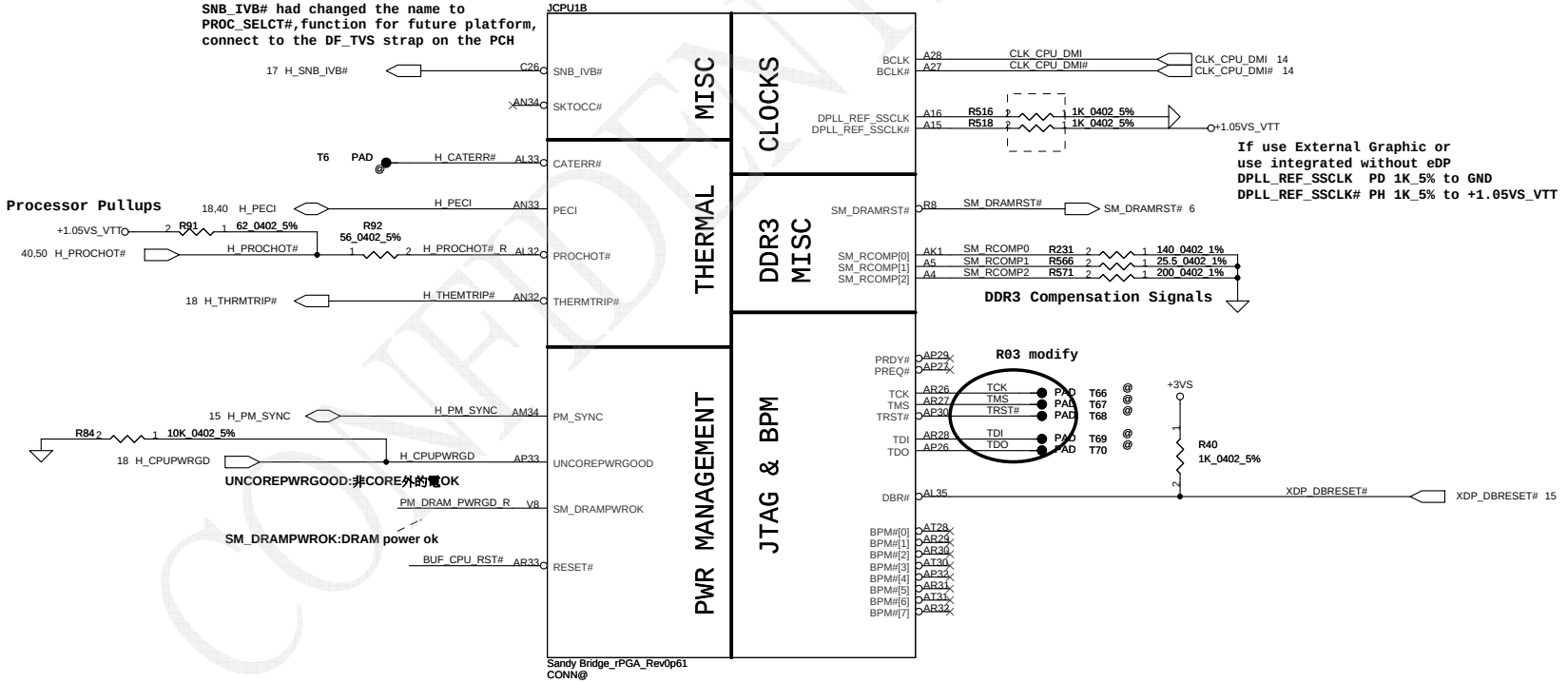
Buffered reset to CPU



RESET#:都ok後給CPU做reset

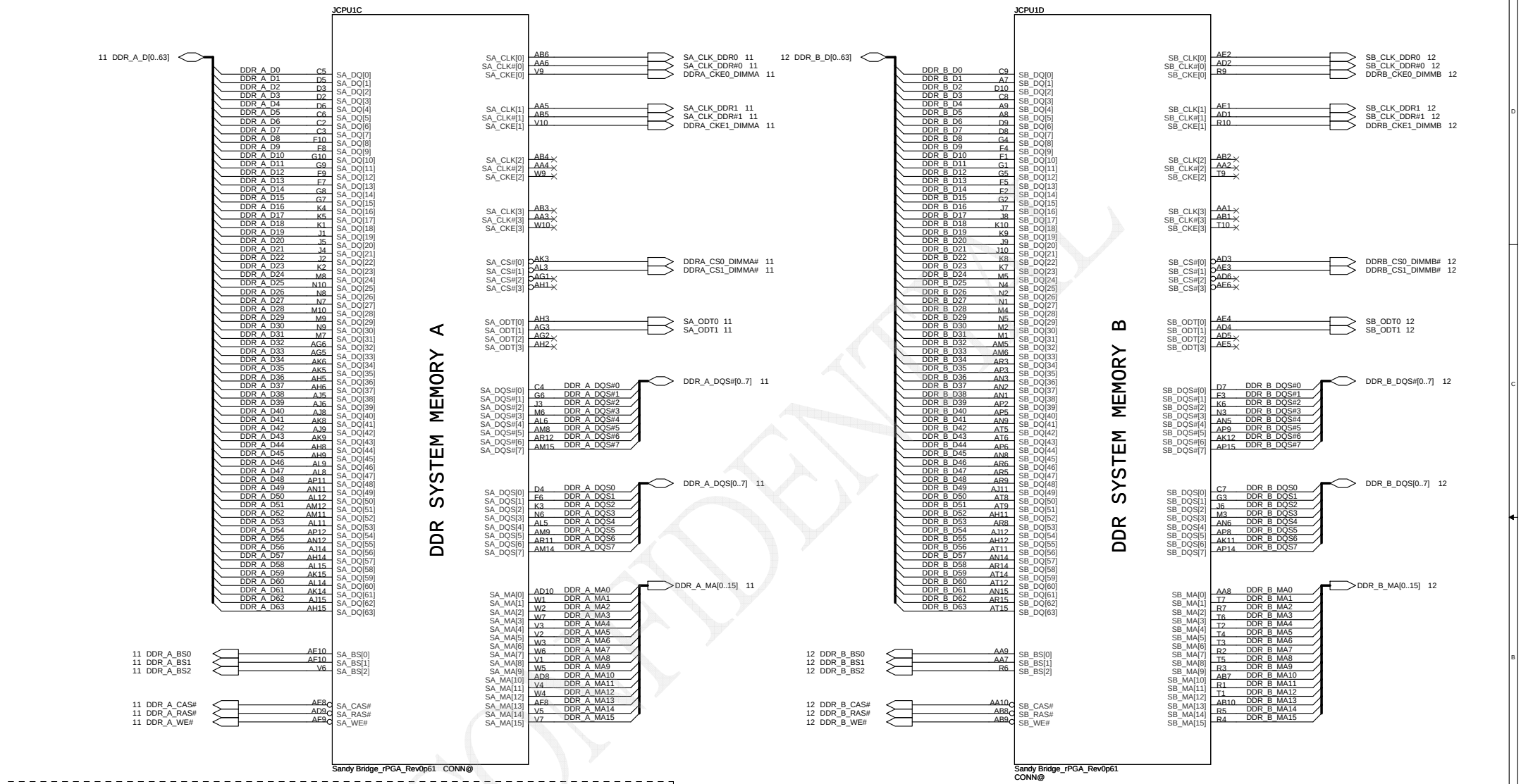


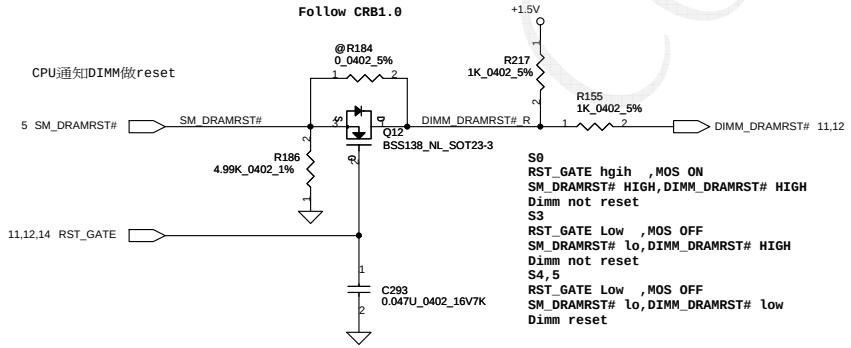
SNB_IVB# had changed the name to PROC_SELCT#,function for future platform, connect to the DF_TVS strap on the PCH



Security Classification	Compal Secret Data		
Issued Date	2011/02/08	Deciphered Date	2012/02/08

Compal Electronics, Inc.	
Title	PROCESSOR(2/7) PM,XDP,CLK
Size: Custom	Document Number: JE50-HR/SJV50-HR M/B Schematics
Rev: E	
Date: Wednesday, June 08, 2011	Sheet 5 of 61





Security Classification	Compal Secret Data		
Issued Date	2011/02/08	Deciphered Date	2012/02/08

Compal Electronics, Inc.	
Title	PROCESSOR(3/7) DDRIII
Size: Custom	Document Number: JE50-HR/SJV50-HR M/B Schematics
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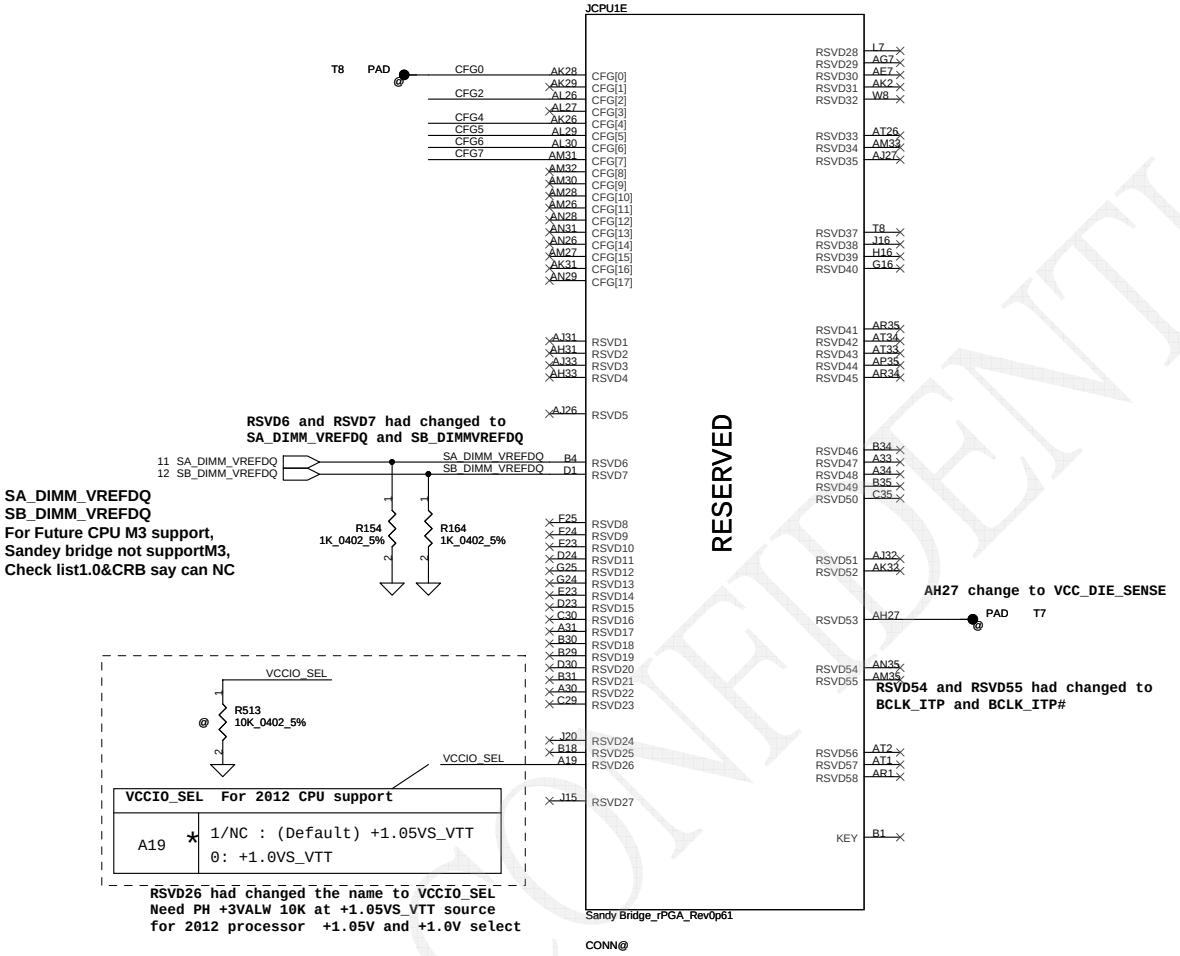
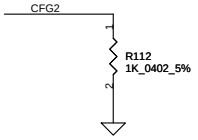
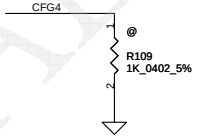
Date: Wednesday, June 08, 2011	Sheet 6 of 61

CFG Straps for Processor

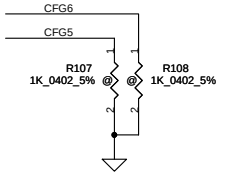




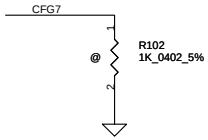
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0:Lane Reversed



Display Port Presence Strap	
CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIE Port Bifurcation Straps	
CFG[6:5]	*11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

Security Classification	Compal Secret Data		
Issued Date	2011/02/08	Deciphered Date	2012/02/08

Compal Electronics, Inc.

Title: PROCESSOR(4/7) RSVD,CFG

Size: Custom | Document Number: JE50-HR/SJV50-HR M/B Schematics | Rev: E

Date: Wednesday, June 08, 2011 | Sheet 7 of 61

POWER

SV type CPU

QC 94A
DC 53A

JCPU1F

PEG AND DDR

CORE SUPPLY

SVID

SENSE LINES

8.5A

INTEL Recommend
4*470uF,16*22uF and 10*10uF
from PDDG 1.0

INTEL Recommend
2*330uF,12*22uF
from PDDG 1.0

PAW00
use 470uF*2
330uF*3

Follow Power Suggestion ,
place 3-pin Cap for CPU_CORE

R02 modify
@
ME interefer,not pop!!

Place the PU
resistors close to VR

Place the PU
resistors close to CPU

VSSIO_SENSE
change to
VSS_SENSE_VCCIO

Should change to connect form
power cirucit & layout differential
with VCCIO_SENSE.

Sandy Bridge rPGA Rev0p61

Security Classification	Compal Secret Data		
Issued Date	2011/02/08	Deciphered Date	2012/02/08

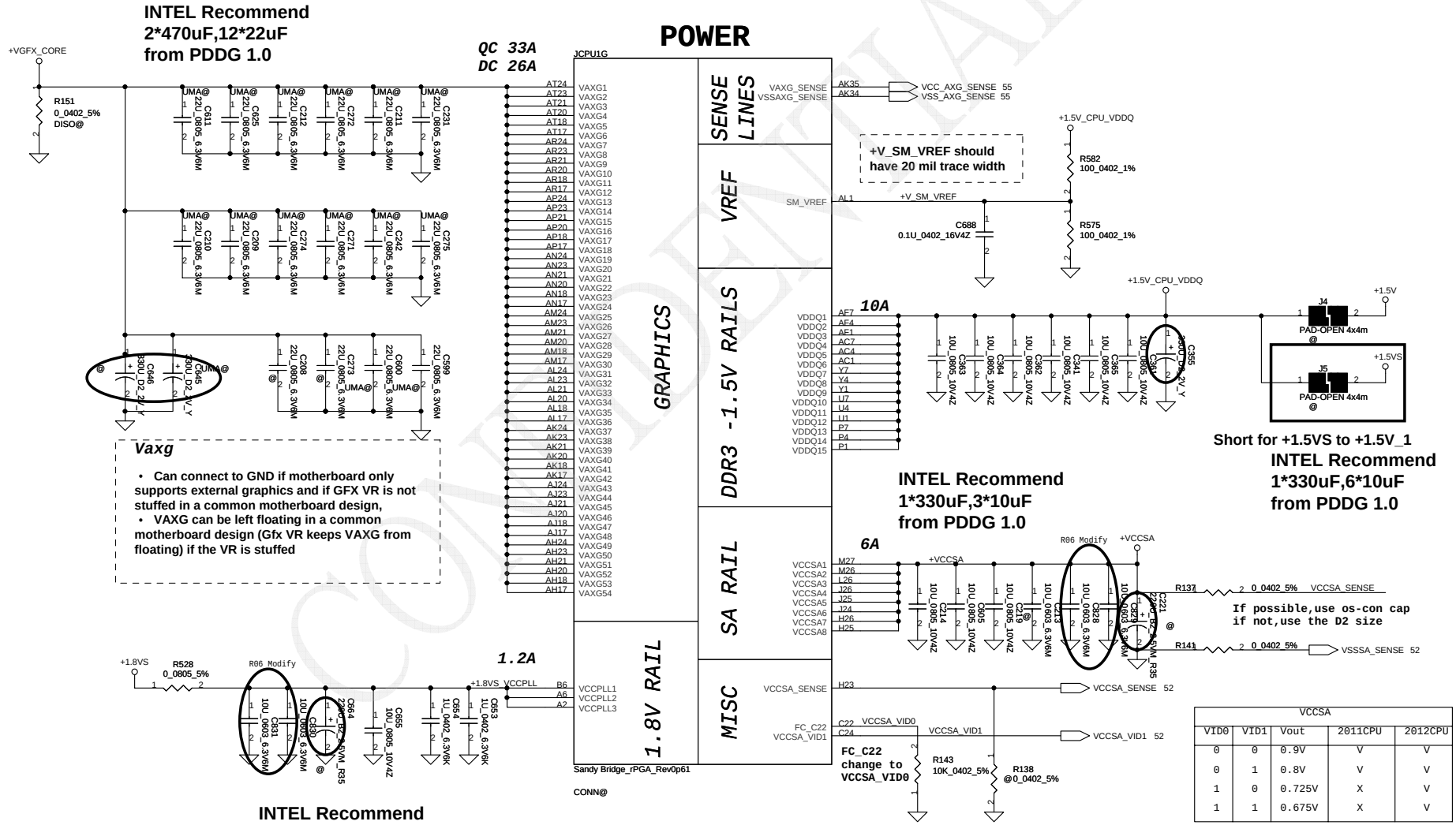
Compal Electronics, Inc.

Title: PROCESSOR(5/7) PWR,BYPASS

Size: Custom | Document Number: JE50-HR/SJV50-HR M/B Schematics | Rev: E

Date: Wednesday, June 08, 2011 | Sheet 8 of 61

POWER



VCCSA				
VID0	VID1	Vout	2011CPU	2012CPU
0	0	0.9V	V	V
0	1	0.8V	V	V
1	0	0.725V	X	V
1	1	0.675V	X	V

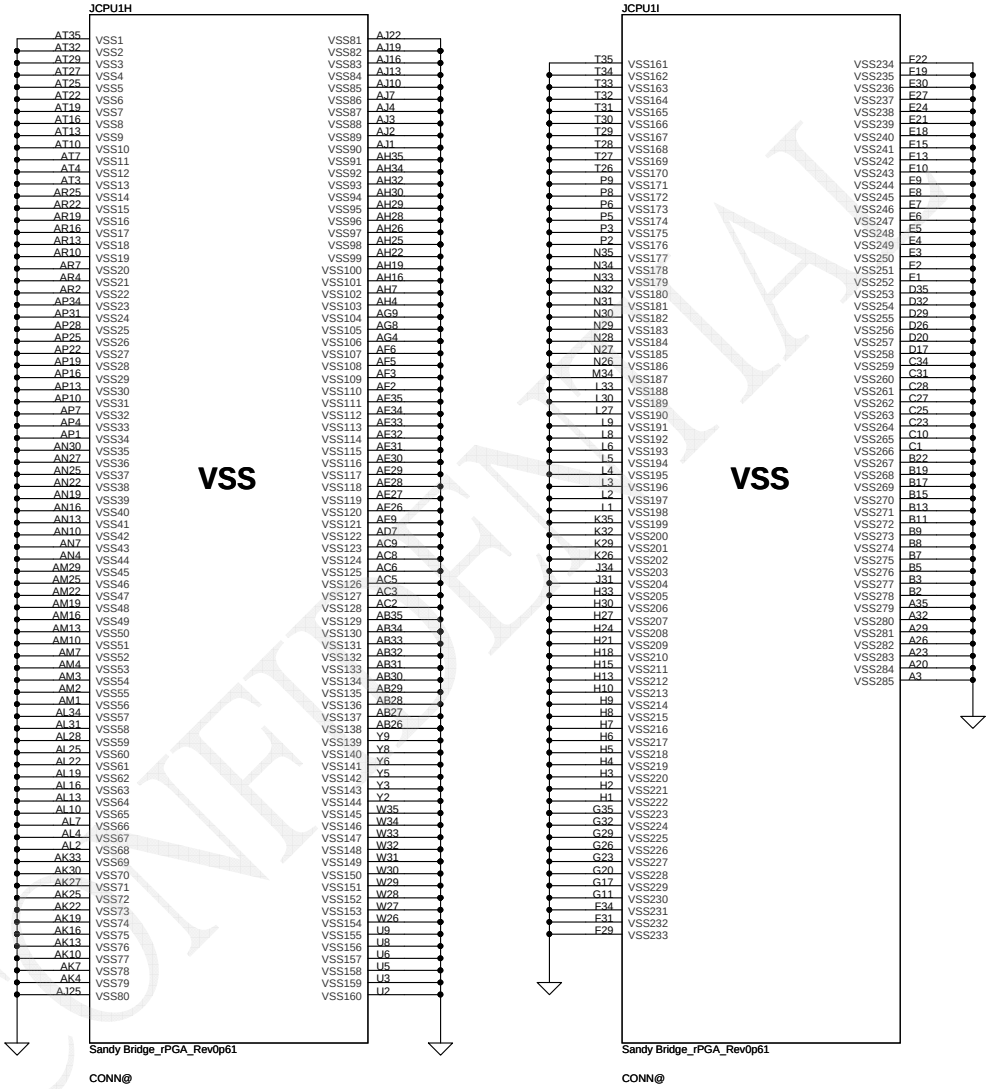
Security Classification	Compal Secret Data		
Issued Date	2011/02/08	Deciphered Date	2012/02/08

Compal Electronics, Inc.

Title: PROCESSOR(6/7) PWR

Size: Custom | Document Number: JE50-HR/SJV50-HR M/B Schematics | Rev: E

Date: Wednesday, June 08, 2011 | Sheet 9 of 61



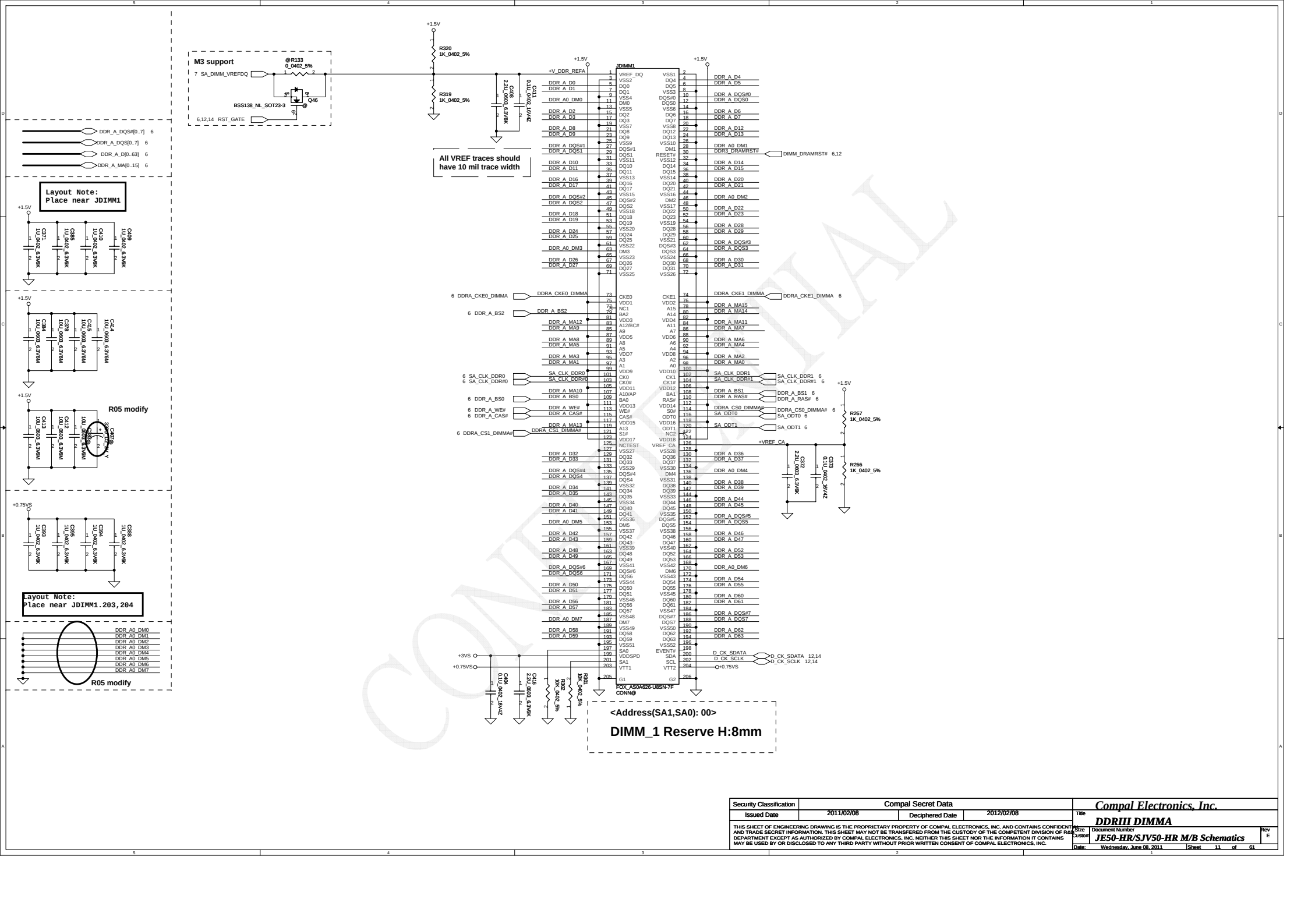
Security Classification	Compal Secret Data		
Issued Date	2011/02/08	Deciphered Date	2012/02/08

Compal Electronics, Inc.

Title: PROCESSOR(7/7) VSS

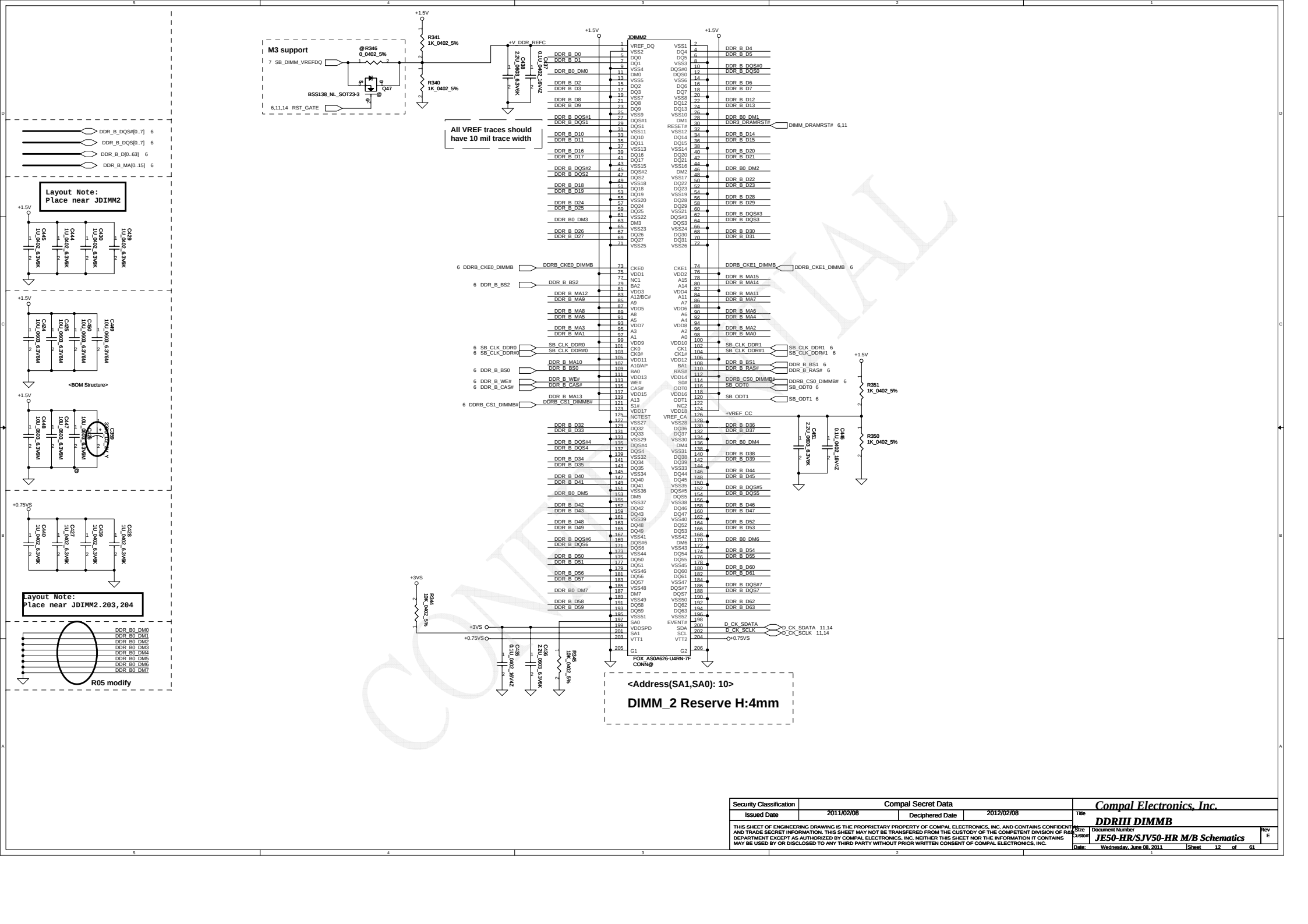
Size	Document Number	Rev
Custom	JE50-HR/SJV50-HR M/B Schematics	E

Date: Wednesday, June 08, 2011 | Sheet 10 of 61



Security Classification	Compal Secret Data		
Issued Date	2011/02/08	Deciphered Date	2012/02/08

Compal Electronics, Inc.		
Title: DDRIII DIMMA		
Size: Custom	Document Number: JE50-HR/SJV50-HR M/B Schematics	Rev: E
Date: Wednesday, June 08, 2011	Sheet 11 of 61	



Security Classification	Compal Secret Data		
Issued Date	2011/02/08	Deciphered Date	2012/02/08

Compal Electronics, Inc.			
Title: DDRIII DIMMB			
Size: Custom	Document Number: JE50-HR/SJV50-HR M/B Schematics		Rev: E
Date: Wednesday, June 08, 2011	Sheet 12 of 61		

PCH_RTCX1
R568 1 2 10M_0402_5%
PCH_RTCX2
Y3 OSC NC OSC NC 32.768KHZ_12.5PF_Q13MC1461000
18P_0402_50V8J C682
C686 18P_0402_50V8J

+RTCVCC
R567 1 2 1M_0402_5% SM_INTRUDER#
R585 1 2 330K_0402_5% PCH_INTVRMEN

INTVRMEN

* H : Integrated VRM enable
L : Integrated VRM disable

(INTVRMEN should always be pull high.)

+3VS
R294 1 @ 2 1K_0402_5% PCH_SPKR

HIGH= Enable (No Reboot)
* LOW= Disable (Default)

+3VALW_PCH
R556 1K_0402_5%
R557 @ 0_0402_5%
HDA_SDOUT_PCH
40 HDA_SDO

HDA_SDO as Capella ME override (GPIO33)

ME debug mode,this signal has a weak internal PD
* Low = Disabled (Default)
High = Enabled [Flash Descriptor Security Overide]

+3VALW_PCH
R539 1K_0402_5% HDA_SYNC_PCH

This signal has a weak internal pull-down

On Die PLL VR Select is supplied by
* 1.5V when smapled high
1.8V when sampled low
Needs to be pulled High for Huron River platfrom

R544 33_0402_5%
42 HDA_BITCLK_AUDIO — HDA_BITCLK_PCH
R542 33_0402_5%
42 HDA_SYNC_AUDIO — HDA_SYNC_PCH_R
R545 33_0402_5%
42 HDA_RST_AUDIO# — HDA_RST_PCH#
R555 33_0402_5%
42 HDA_SDOUT_AUDIO — HDA_SDOUT_PCH

+3VALW_PCH
R666 200_0402_1% PCH_JTAG_TDO
R637 200_0402_1% PCH_JTAG_TMS
R646 200_0402_1% PCH_JTAG_TDI
R671 100_0402_1%
R636 100_0402_1%
R648 100_0402_1%

+RTCBATT
+CHGRTC
R375 1K_0402_5%
+RTCBATT_R
D33 20mil
+RTCVCC
20mil
CHN202UPT_SC70-3
C471 0.1U_0402_16V4Z

RTCRST close RAM door
R05 modify
+RTCVCC
C360 1U_0603_10V6K
R248 20K_0402_1%
R243 20K_0402_1%
C356 1U_0603_10V6K
J1 0_0603_5% @
J2 0_0603_5% @
SRTCRST close RAM door

Prevent back drive issue.

+3VS
Q36 BSS138_NL_SOT23-3
HDA_SYNC_PCH
R540 @ 0_0402_5%
R792 1M_0402_5%
R03 modify

R674 51_0402_5%

PCH_SPI_CLK_1 — R681 0_0402_5% — PCH_SPI_CLK
PCH_SPI_CS0#_1 — R651 0_0402_5% — PCH_SPI_CS0#
PCH_SPI_MOSI_1 — R684 0_0402_5% — PCH_SPI_MOSI
PCH_SPI_MISO_1 — R652 0_0402_5% — PCH_SPI_MISO

+RTCBATT
JBATT1
CONN@ SUYIN_060003HA002G202ZL
20100416 add

U33A

PCH_RTCX1	A20	RTCX1	RTC	FWH0 / LAD0	C38 LPC_AD0
PCH_RTCX2	C20	RTCX2		FWH1 / LAD1	A38 LPC_AD1
PCH_RTCRST#	D20	RTCRST#		FWH2 / LAD2	B37 LPC_AD2
PCH_SRTCRST#	G22	SRTCRST#		FWH3 / LAD3	C37 LPC_AD3
SM_INTRUDER#	K22	INTRUDER#		FWH4 / LFRAME#	D36 LPC_FRAME#
PCH_INTVRMEN	C17	INTVRMEN		LDRQ0#	E36
				LDRQ1# / GPIO23	K36
				SERIRQ	V5 SERIRQ
HDA_BITCLK_PCH	N34	HDA_BCLK	IHDA		
HDA_SYNC_PCH	L34	HDA_SYNC			
42 PCH_SPKR	T10	SPKR			
HDA_RST_PCH#	K34	HDA_RST#			
42 HDA_SDIN0	E34	HDA_SDIN0			
	G34	HDA_SDIN1			
	C34	HDA_SDIN2			
	A34	HDA_SDIN3			
HDA_SDOUT_PCH	A36	HDA_SDO			
	C36	HDA_DOCK_EN# / GPIO33			
	N32	HDA_DOCK_RST# / GPIO13			
PCH_JTAG_TCK	J3	JTAG_TCK	JTAG		
PCH_JTAG_TMS	H7	JTAG_TMS			
PCH_JTAG_TDI	K5	JTAG_TDI			
PCH_JTAG_TDO	H1	JTAG_TDO			
PCH_SPI_CLK	T3	SPI_CLK	SPI		
PCH_SPI_CS0#	Y14	SPI_CS0#			
	T1	SPI_CS1#			
PCH_SPI_MOSI	V4	SPI_MOSI			
PCH_SPI_MISO	U3	SPI_MISO			
			SATA	SATA0RXN	AM3 SATA_PRX_DTX_N0 34
				SATA0RXP	AM1 SATA_PRX_DTX_P0 34
				SATA0TXN	AP7 SATA_PTX_DRX_N0 34
				SATA0TXP	AP5 SATA_PTX_DRX_P0 34
				SATA1RXN	AM10 SATA_PRX_DTX_N1 34
				SATA1RXP	AM8 SATA_PRX_DTX_P1 34
				SATA1TXN	AP11 SATA_PTX_DRX_N1 34
				SATA1TXP	AP10 SATA_PTX_DRX_P1 34
				SATA2RXN	AD7
				SATA2RXP	AD5
				SATA2TXN	AH5
				SATA2TXP	AH4
				SATA3RXN	AB8
				SATA3RXP	AB10
				SATA3TXN	AF3
				SATA3TXP	AF1
				SATA4RXN	Y7
				SATA4RXP	Y5
				SATA4TXN	AD3
				SATA4TXP	AD1
				SATA5RXN	Y3
				SATA5RXP	Y1
				SATA5TXN	AB3
				SATA5TXP	AB1
				SATAICOMPO	Y11
				SATAICOMPI	Y10 SATA_COMP
				SATA3RCOMPO	AB12
				SATA3COMPI	AB13 SATA3_COMP
				SATA3RBIAS	AH1 RBIAS_SATA3
				SATALED#	P3 PCH_SATALED#
				SATA0GP / GPIO21	V14 SGEN#
				SATA1GP / GPIO19	P1 PCH_GPIO19

COUGARPOINT_FCBGA989_D

HDD
ODD
R20 modify
change to port1 cause by intel SATA II issue (20110201)

R260 37.4_0402_1% +1.05VS_PCH
R241 49.9_0402_1% +1.05VS_PCH
R625 750_0402_1%
<BOM Structure>
PCH_SATALED# 41

R05 modify
+RTCBATT
JBATT2
CONN@ SUYIN_060003HA002G202ZL

SERIRQ R275 10K_0402_5%
PCH_SATALED# R640 10K_0402_5%
PCH_GPIO19 R624 4.7K_0402_5%
R02 modify

R259 10K_0402_5%
SGEN#
R258 10K_0402_5% @

	GPIO21 SGEN#
Switchable GPU	0
*Non-Switchable	1

U36
+3VS
R654 3.3K_0402_5% SPI_WP1#
R667 3.3K_0402_5% SPI_HOLD1#
PCH_SPI_CS0#_1
PCH_SPI_CLK_1
PCH_SPI_MOSI_1
PCH_SPI_MISO_1
EN25F32-100HIP SOP 8P
SA00003IN00
SPI ROM FOR ME (4MB)
Footprint 200mil

Boot BIOS Strap		
Boot BIOS	GPIO51	GPIO19
LPC	0	0
Reserved	0	1
-	1	0
* SPI	1	1

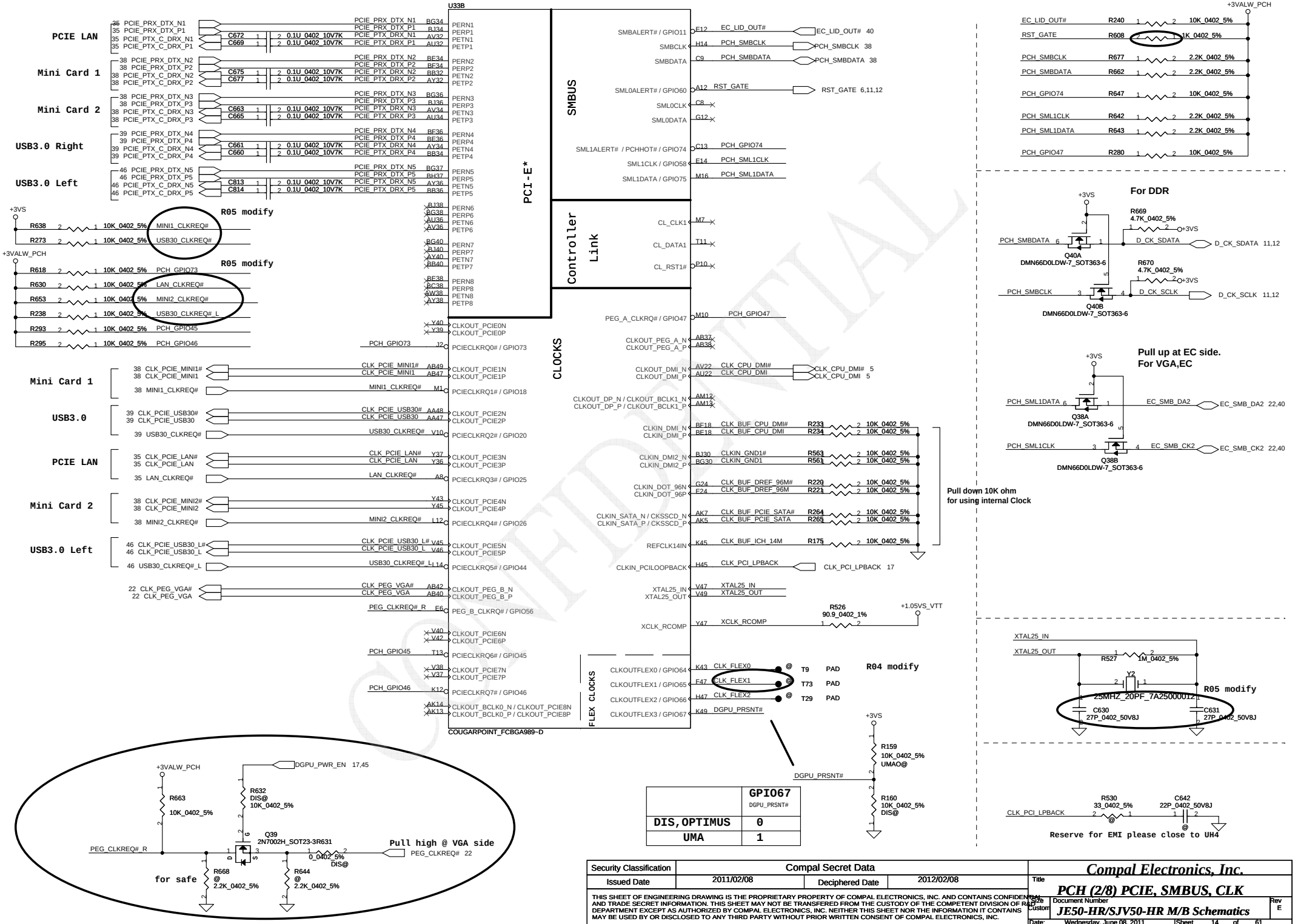
Security Classification	Compal Secret Data		
Issued Date	2011/02/08	Deciphered Date	2012/02/08

Compal Electronics, Inc.

Title: PCH (1/8) SATA,HDA,SPI, LPC, XDP

Size: Custom | Document Number: JE50-HR/SJV50-HR M/B Schematics | Rev: E

Date: Wednesday, June 08, 2011 | Sheet 13 of 61



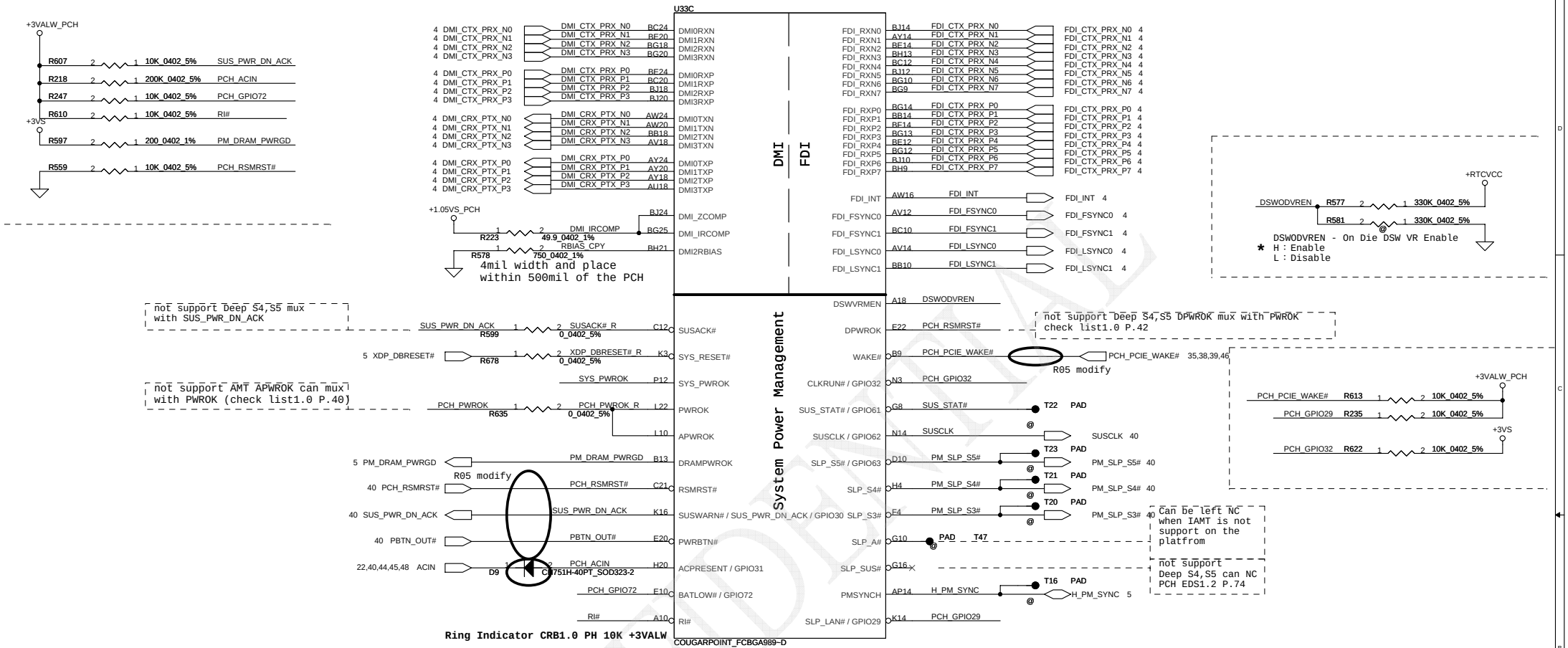
Security Classification	Compal Secret Data
Issued Date	2011/02/08
Deciphered Date	2012/02/08

Compal Electronics, Inc.

Title: PCH (2/8) PCIE, SMBUS, CLK

Size: Custom | Document Number: JE50-HR/SJV50-HR M/B Schematics | Rev: E

Date: Wednesday, June 08, 2011 | Sheet 14 of 61



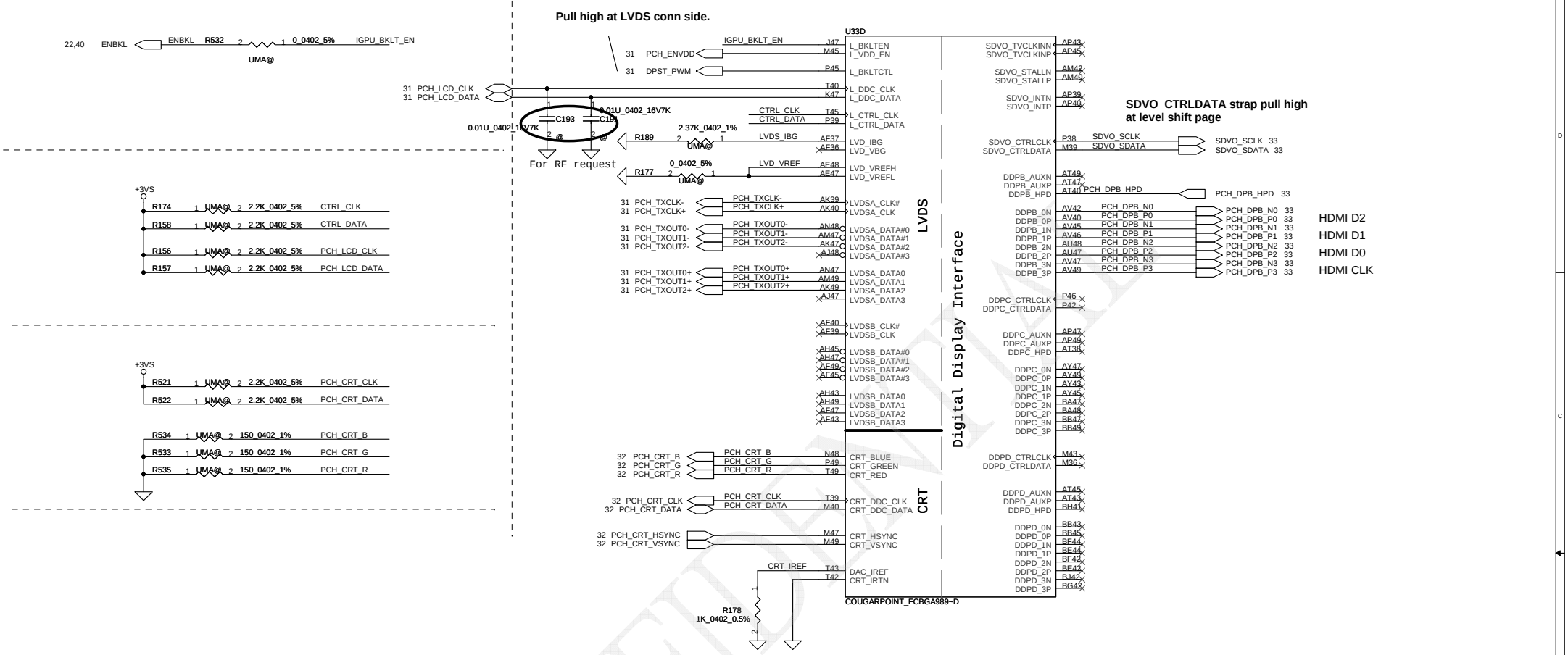
Security Classification	Compal Secret Data		
Issued Date	2011/02/08	Deciphered Date	2012/02/08

Compal Electronics, Inc.

Title: **PCH (3/8) DMI,FDI,PM,**

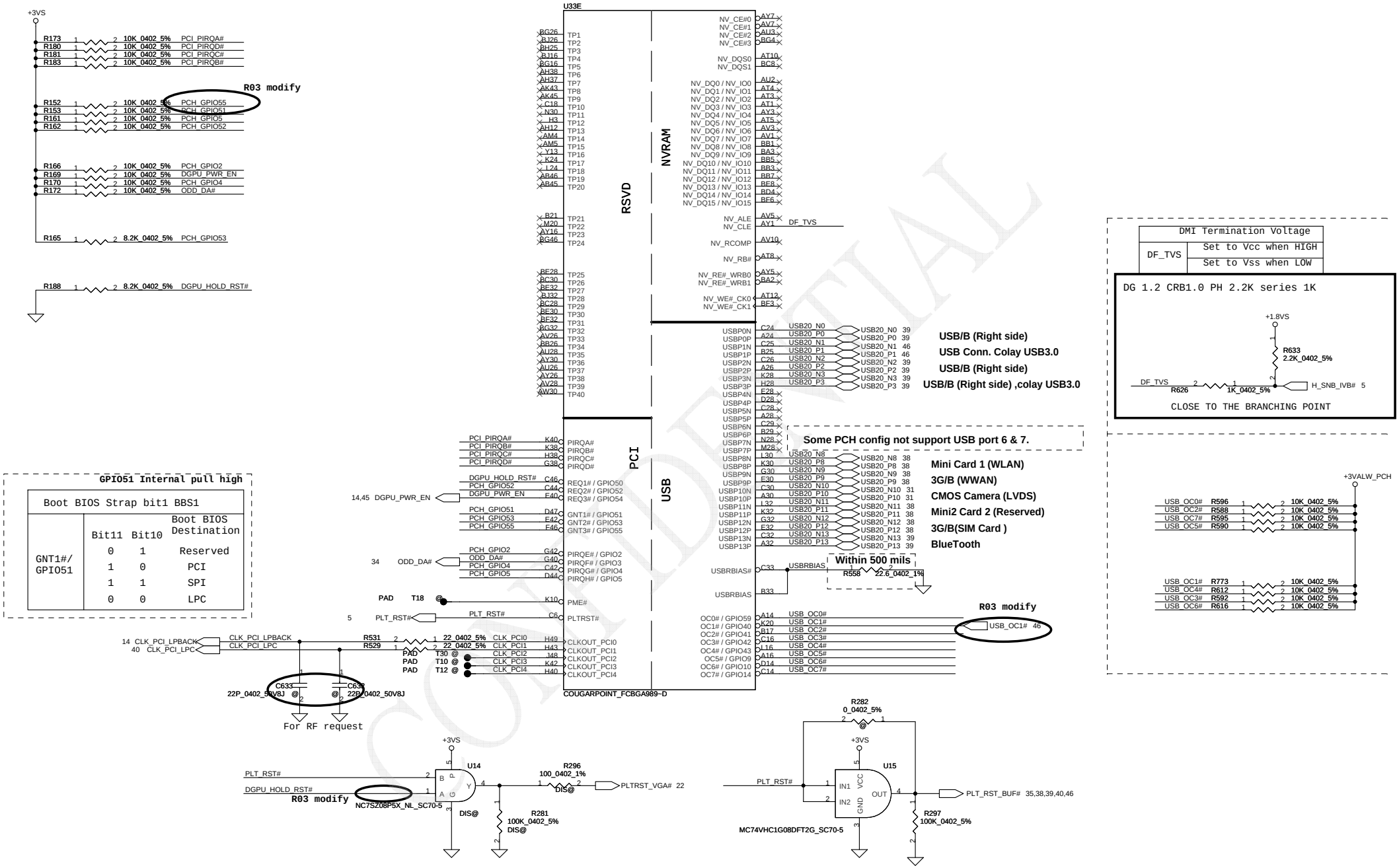
Size: Custom | Document Number: **JE50-HR/SJV50-HR M/B Schematics** | Rev: E

Date: Wednesday, June 08, 2011 | Sheet 15 of 61



Security Classification	Compal Secret Data		
Issued Date	2011/02/08	Deciphered Date	2012/02/08

Compal Electronics, Inc.			
Title: PCH (4/9) LVDS,CRT,DP,HDMI			
Size: Custom	Document Number: JE50-HR/SJV50-HR M/B Schematics		Rev: E
Date: Wednesday, June 08, 2011	Sheet 16 of 61		



Security Classification	Compal Secret Data		
Issued Date	2011/02/08	Deciphered Date	2012/02/08

Compal Electronics, Inc.			
Title: PCH (5/9) PCI, USB, NVRAM			
Size: Custom	Document Number: JE50-HR/SJV50-HR M/B Schematics		Rev: E
Date: Wednesday, June 08, 2011	Sheet 17 of 61		

HDA_SYNC PH(PLL =+1.5VS)

GPIO28
On-Die PLL Voltage Regulator
This signal has a weak internal pull up

* H : On-Die voltage regulator enable
  L : On-Die PLL Voltage Regulator disable

R272 1 @ 2 1K_0402_5% PCH_GPIO28
+3VALW_PCH R768 1 2 4.7K_0402_5%

Deep S4,S5 wake event signal
RTC alarm,Power BTN,GPIO27
PCH_GPIO27 (Have internal Pull-High)
Deep S4,S5 wake event signal
No use PD to GND Check list1.0 P.70

R661 1 2 10K_0402_5% PCH_GPIO27

+3VS
R623 1 NORT@ 2 10K_0402_5% OPTIMUS_EN#
R639 1 OPT@ 2 10K_0402_5%

	GPIO38 OPTIMUS_EN#
* OPTIMUS	0
Non-OPTIMUS	1

R04 modify
+3VS
R277 2 200K_0402_5% WWAN_OFF#
R276 10K_0402_5% PCH_GPIO0
R546 10K_0402_5% WL_EN#
R191 10K_0402_5% DGPU_HPD_INT#
R641 10K_0402_5% PCH_GPIO16
R194 10K_0402_5% DGPU_PWROK
R290 10K_0402_5% PCH_GPIO22
R649 10K_0402_5% PCH_GPIO39

R04 modify
R291 200K_0402_5% ODD_DETECT#
R619 10K_0402_5% BT_ON#
R292 10K_0402_5% PCH_GPIO48
R274 10K_0402_5% WL_OFF#

+3VALW_PCH
R262 10K_0402_5% PCH_GPIO24
R620 10K_0402_5% PCH_GPIO12
R672 1K_0402_5% SMIB
R263 10K_0402_5% PCH_GPIO57

GPIO24 Unmultiplexed
NOTE: GPIO24 configuration register bits are not cleared by CF9h reset event.

CRB1.0 PH10K to +3VALW

U33F

R05 modify
39 WL_EN# — PCH_GPIO0 T7 — WL_EN# A42
33 DGPU_HPD_INT# — DGPU_HPD_INT# H36
40 EC_SCI# — EC_SCI# E38
40 EC_SMI# — EC_SMI# C10
PCH_GPIO12 C4
39,46 SMIB — SMIB G2
PCH_GPIO16 U2
54 VGA_PWROK — R193 1 DIS@ 2 0_0402_5% — DGPU_PWROK D40
R05 modify
PCH_GPIO22 T5
PCH_GPIO24 F8
PCH_GPIO27 E16
PCH_GPIO28 P8
38,39 BT_ON# — BT_ON# K1
K4
34 ODD_DETECT# — ODD_DETECT# V8
R03 modify
38 WWAN_OFF# — WWAN_OFF# M5
OPTIMUS_EN# N2
PCH_GPIO39 M3
PCH_GPIO48 V13
R03 modify
38 WL_OFF# — WL_OFF# V3
PCH_GPIO57 D6

BMBUSY# / GPIO0
TACH1 / GPIO1
TACH2 / GPIO6
TACH3 / GPIO7
GPIO8
LAN_PHY_PWR_CTRL / GPIO12
GPIO15
SATA4GP / GPIO16
TACH0 / GPIO17
SCLOCK / GPIO22
GPIO24 / MEM_LED
GPIO27
GPIO28
STP_PCI# / GPIO34
GPIO35
SATA2GP / GPIO36
SATA3GP / GPIO37
SLOAD / GPIO38
SDATAOUT0 / GPIO39
SDATAOUT1 / GPIO48
SATA5GP / GPIO49
GPIO57

GPIO

TACH4 / GPIO68 C40 — ODD_EN# — ODD_EN# 34
TACH5 / GPIO69 B41 — PCH_GPIO69
TACH6 / GPIO70 C41 — PCH_GPIO70
TACH7 / GPIO71 A40 — PCH_GPIO71

CPU/MISC

A20GATE P4 — GATEA20 40
PECI AU16 — PCH_PECI_R 1 0_0402_5% @ R239 2 — H_PECI 5,40
RCIN# P5 — EC_KBRST# — EC_KBRST# 40
PROCPWRGD AY11 — H_CPUPWRGD 5
THRMTRIP# AY10 — PCH_THRMTRIP#_R 1 R627 2 390_0402_5% — H_THRMTRIP# — H_THRMTRIP# 5
INIT3_3V# T14

+3VS
R278 10K_0402_5%

PECI CPU-EC
CTRL+ALT+DEL
non CPU power ok
130 degree shut sown

INIT3_3V Checklist1.0 P.59
This signal has weak internal PU, can't pull low, leave NC

NC_1 AH8
NC_2 AK11
NC_3 AH10
NC_4 AK10
NC_5 P37

TS_VSS1~4
PD to GND

NCTF

PAD T61 @ A4 — VSS_NCTF_1
PAD T46 @ A44 — VSS_NCTF_2
PAD T44 @ A45 — VSS_NCTF_3
PAD T41 @ A46 — VSS_NCTF_4
PAD T52 @ A5 — VSS_NCTF_5
PAD T51 @ A6 — VSS_NCTF_6
PAD T64 @ B3 — VSS_NCTF_7
PAD T37 @ B47 — VSS_NCTF_8
PAD T55 @ BD1 — VSS_NCTF_9
PAD T34 @ BD49 — VSS_NCTF_10
PAD T56 @ BE1 — VSS_NCTF_11
PAD T35 @ BE49 — VSS_NCTF_12
PAD T57 @ BF1 — VSS_NCTF_13
PAD T36 @ BF49 — VSS_NCTF_14

VSS_NCTF_15 BG2 @ — T58 PAD
VSS_NCTF_16 BG48 @ — T39 PAD
VSS_NCTF_17 BH3 @ — T59 PAD
VSS_NCTF_18 BH47 @ — T40 PAD
VSS_NCTF_19 BJ4 @ — T60 PAD
VSS_NCTF_20 BJ44 @ — T45 PAD
VSS_NCTF_21 BJ45 @ — T43 PAD
VSS_NCTF_22 BJ46 @ — T42 PAD
VSS_NCTF_23 BJ5 @ — T50 PAD
VSS_NCTF_24 BJ6 @ — T49 PAD
VSS_NCTF_25 C2 @ — T65 PAD
VSS_NCTF_26 C48 @ — T38 PAD
VSS_NCTF_27 D1 @ — T63 PAD
VSS_NCTF_28 D49 @ — T32 PAD
VSS_NCTF_29 E1 @ — T54 PAD
VSS_NCTF_30 E49 @ — T33 PAD
VSS_NCTF_31 F1 @ — T53 PAD
VSS_NCTF_32 F49 @ — T31 PAD

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ODD_EN# R771 10K_0402_5%
EC_KBRST# R279 10K_0402_5%

+3VS
R554 10K_0402_5% @ PCH_GPIO69
R548 10K_0402_5% @ PCH_GPIO70
R553 10K_0402_5% PCH_GPIO69
R549 10K_0402_5% PCH_GPIO70

R02 modify
R550 10K_0402_5% X76@ PCH_GPIO71
R551 10K_0402_5% X76@

Project ID	GPIO69	GPIO70
* P5WE0	0	0
P7YE0	0	0
x	1	0
x	1	1

	GPIO71 PCH_GPIO71
*VRAM 800 MHz	0
VRAM 900 MHz	1

Security Classification	Compal Secret Data		
Issued Date	2011/02/08	Deciphered Date	2012/02/08

Compal Electronics, Inc.

Title: PCH (6/9) GPIO, CPU, MISC

Size: Custom | Document Number: JE50-HR/SJV50-HR M/B Schematics | Rev: E

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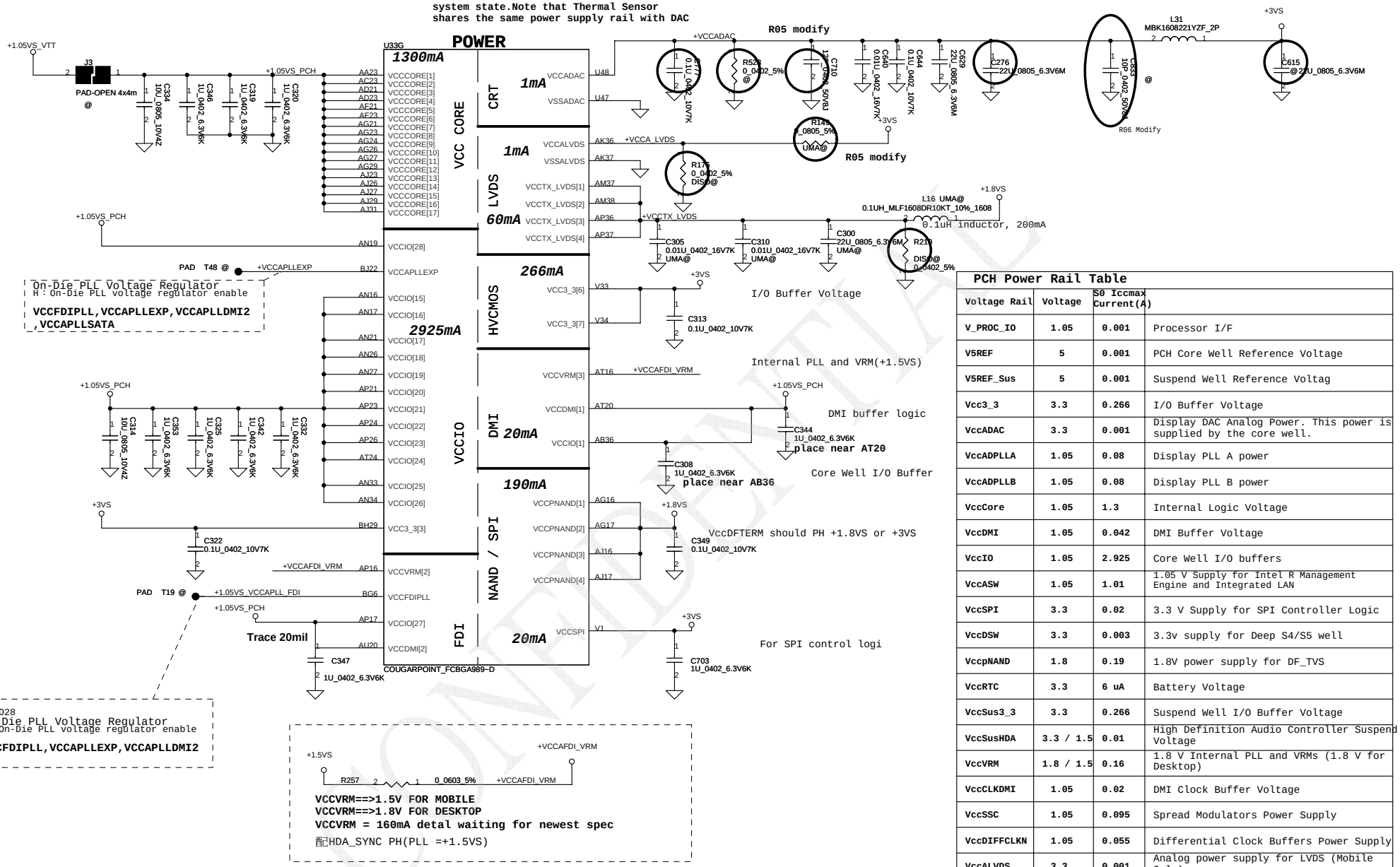

PCH Power Rail Table

Voltage Rail	Voltage	S0 Iccmax Current(A)	
V_PROC_IO	1.05	0.001	Processor I/F
V5REF	5	0.001	PCH Core Well Reference Voltage
V5REF_Sus	5	0.001	Suspend Well Reference Voltag
Vcc3_3	3.3	0.266	I/O Buffer Voltage
VccADAC	3.3	0.001	Display DAC Analog Power. This power is supplied by the core well.
VccADPLLA	1.05	0.08	Display PLL A power
VccADPLLB	1.05	0.08	Display PLL B power
VccCore	1.05	1.3	Internal Logic Voltage
VccDMI	1.05	0.042	DMI Buffer Voltage
VccIO	1.05	2.925	Core Well I/O buffers
VccASW	1.05	1.01	1.05 V Supply for Intel R Management Engine and Integrated LAN
VccSPI	3.3	0.02	3.3 V Supply for SPI Controller Logic
VccDSW	3.3	0.003	3.3v supply for Deep S4/S5 well
VccpNAND	1.8	0.19	1.8V power supply for DF_TVS
VccRTC	3.3	6 uA	Battery Voltage
VccSus3_3	3.3	0.266	Suspend Well I/O Buffer Voltage
VccSusHDA	3.3 / 1.5	0.01	High Definition Audio Controller Suspend Voltage
VccVRM	1.8 / 1.5	0.16	1.8 V Internal PLL and VRMs (1.8 V for Desktop)
VccCLKDMI	1.05	0.02	DMI Clock Buffer Voltage
VccSSC	1.05	0.095	Spread Modulators Power Supply
VccDIFFCLKN	1.05	0.055	Differential Clock Buffers Power Supply
VccALVDS	3.3	0.001	Analog power supply for LVDS (Mobile Only)
VccTX_LVDS	1.8	0.06	Analog power supply for LVDS (Mobile Only)

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Issued Date	2011/02/08	Deciphered Date	2012/02/08

Compal Electronics, Inc.

Title: PCH (7/9) PWR

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Have internal VRM

VCC3_3 = 266mA detal waiting for newest spec
VCCDMI = 42mA detal waiting for newest spec

POWER

U33J

+3VS
R150 0_0805_5% @
L14 10UH_LB2012T100MR_20%
+3VS_VCC_CLKF33
C227 10U_0805_10V4Z
C304 1U_0402_6.3V6K

+1.05V analog internal clock PLL Can NC
+1.05VS_PCH
R167 0_0603_5% @
+VCCACLK

Not support Deep S4,S5 connect to +3VALW
+3VALW_PCH
C340 0.1U_0402_10V7K

PAD T17 @ +PCH_VCCDSW
+3VS_VCC_CLKF33

suppied by internal 1.05V VR must NC
PAD T11 @ +VCCAPLL_CPY_PCH
+1.05VS_PCH
PAD T13 @ +VCCSUS1

GPIO28
On-Die PLL Voltage Regulator
H : On-Die PLL voltage regulator enable
VCCFDIPLL,VCCAPLLEXP,VCCAPLLDMI2 ,VCCAPLLSATA

AD49	VCCACLK		
T16	VCCDSW3_3		
V12	DCPSUSBYP	3mA	
T38	VCC3_3[5]		
BH23	VCCAPLLDMI2	119mA	USB
AL29	VCCIO[14]		
AL24	DCPSUS[3]		
AA19	VCCASW[1]	1010mA	Clock and Miscellaneous
AA21	VCCASW[2]		
AA24	VCCASW[3]		
AA26	VCCASW[4]		
AA27	VCCASW[5]		
AA29	VCCASW[6]		
AA31	VCCASW[7]		
AC26	VCCASW[8]		
AC27	VCCASW[9]		
AC29	VCCASW[10]		
AC31	VCCASW[11]		
AD29	VCCASW[12]		
AD31	VCCASW[13]		
W21	VCCASW[14]		
W23	VCCASW[15]		
W24	VCCASW[16]		
W26	VCCASW[17]		
W29	VCCASW[18]		
W31	VCCASW[19]		
W33	VCCASW[20]		
N16	DCPRTC		
Y49	VCCVRM[4]		
BD47	VCCADPLLA	80mA	SATA
BF47	VCCADPLLB	80mA	
AE17	VCCIO[7]	55mA	
AF33	VCCIO[8]		
AE34	VCCIO[9]		
AG34	VCCIO[11]		
AG33	VCCIO[10]	95mA	
V16	DCPSST		
T17	DCPSUS[1]		MISC
V19	DCPSUS[2]		
BJ8	V_PROC_IO	1mA	CPU
A22	VCCRTC		RTC
		10mA	VCCSUSHDA

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N26	VCCIO[29]	+1.05VS_PCH	C321 1U_0402_6.3V6K
P26	VCCIO[30]		
P28	VCCIO[31]		
T27	VCCIO[32]		
T29	VCCIO[33]		
T23	VCCSUS3_3[7]	+3VALW_PCH	C330 0.1U_0402_10V7K Place near P24 / C333 0.1U_0402_10V7K Place near P24
T24	VCCSUS3_3[8]		
V23	VCCSUS3_3[9]		
V24	VCCSUS3_3[10]		
P24	VCCSUS3_3[6]		
T26	VCCIO[34]	+1.05VS_PCH	
M26	V5REF_SUS	+PCH_V5REF_SUS	
AN23	DCPSUS[4]	+VCCA_USBSUS	@ T14 PAD
AN24	VCCSUS3_3[1]	+3VALW_PCH	suppied by internal 1.05V VR Must NC
P34	V5REF	+PCH_V5REF_RUN	
N20	VCCSUS3_3[2]	+3V_VCCPSUS	C352 1U_0402_6.3V6K
N22	VCCSUS3_3[3]		
P20	VCCSUS3_3[4]		
P22	VCCSUS3_3[5]		
AA16	VCC3_3[1]	+3VS	C704 0.1U_0402_10V7K Place near AJ2 / C343 0.1U_0402_10V7K Place near AA16,W16 / C309 0.1U_0402_10V7K Place near T34
W16	VCC3_3[8]		
T34	VCC3_3[4]		
AJ2	VCC3_3[2]	+1.05VS_PCH	C350 1U_0402_6.3V6K
AF13	VCCIO[5]		
AH13	VCCIO[12]		
AH14	VCCIO[13]		
AE14	VCCIO[6]		
AK1	VCCAPLLSATA	+VCCSATAPLL @ T62 PAD	
AE11	VCCVRM[1]	+VCCAFDI_VRM	
AC16	VCCIO[2]	+1.05VS_PCH	C351 1U_0402_6.3V6K
AC17	VCCIO[3]		
AD17	VCCIO[4]		
T21	VCCASW[22]	+VCCME_22	R237 0_0603_5%
V21	VCCASW[23]	+VCCME_23	R224 0_0603_5%
T19	VCCASW[21]	+VCCME_21	R236 0_0603_5%
P32	VCCSUSHDA	+VCCSUSHDA	R206 0_0603_5% Need +3VALW and 0.1U close PCH

GPIO28
On-Die PLL Voltage Regulator
H : On-Die PLL voltage regulator enable
VCCFDIPLL,VCCAPLLEXP,VCCAPLLDMI2 ,VCCAPLLSATA

C315 0.1U_0402_16V4Z Close P32

+1.05VS_PCH
L12 10UH_LB2012T100MR_20%
+1.05VS_VCCA_A_DPL
C270 220U_B2_2.5VM_R35
C296 1U_0402_6.3V6K
R806 0_0603_5% @ (R06 Modify)

L11 10UH_LB2012T100MR_20%
+1.05VS_VCCA_B_DPL
C271 220U_B2_2.5VM_R35
C295 1U_0402_6.3V6K

SGA00001700
220U 2.5V M B2
ESR 35mohm@100Khz

C336 22U_0805_6.3V6M
C335 22U_0805_6.3V6M
C326 1U_0402_6.3V6K
C327 1U_0402_6.3V6K
C316 1U_0402_6.3V6K

C348 0.1U_0402_10V7K
+VCCRTCEXT
+VCCAFDI_VRM
+1.05VS_VCCA_A_DPL
+1.05VS_VCCA_B_DPL

+1.05VS_PCH
C311 1U_0402_6.3V6K Place near AF17
C312 1U_0402_6.3V6K Place near AG33
C317 1U_0402_6.3V6K Place near AF33, AF34,AG34

C354 0.1U_0402_10V7K +VCCSST

PAD T15 @ +1.05VM_VCCSUS
suppied by internal 1.05V VR Must NC

+1.05VS_PCH
C700 4.7U_0603_6.3V6K
C694 0.1U_0402_10V7K
C693 0.1U_0402_10V7K
+RTCVCC
C331 1U_0402_6.3V6K
C685 0.1U_0402_10V7K
C687 0.1U_0402_10V7K
Place near BJ8

+5VALW_PCH +3VALW_PCH
R202 100_0402_1%
D8 CH751H-40PT_SOD323-2
+PCH_V5REF_SUS
C318 0.1U_0603_25V7K

+5VS +3VS
R148 100_0402_1%
D7 CH751H-40PT_SOD323-2
+PCH_V5REF_RUN
C244 1U_0603_10V6K

Security Classification	Compal Secret Data		
Issued Date	2011/02/08	Deciphered Date	2012/02/08

Compal Electronics, Inc.

Title: PCH (8/9) PWR

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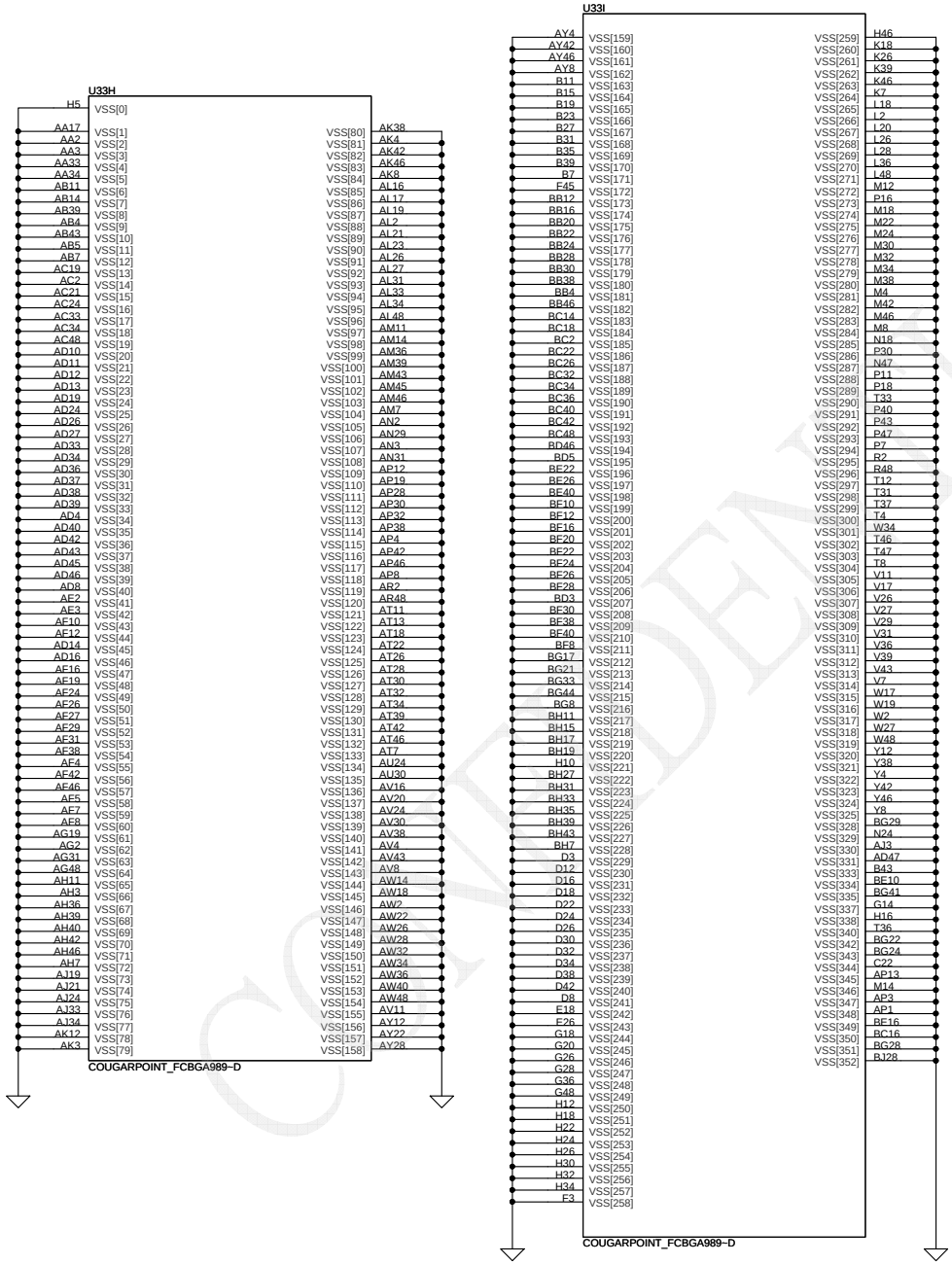

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Issued Date	2011/02/08	Deciphered Date	2012/02/08

Compal Electronics, Inc.

Title: ***PCH (9/9) VSS***

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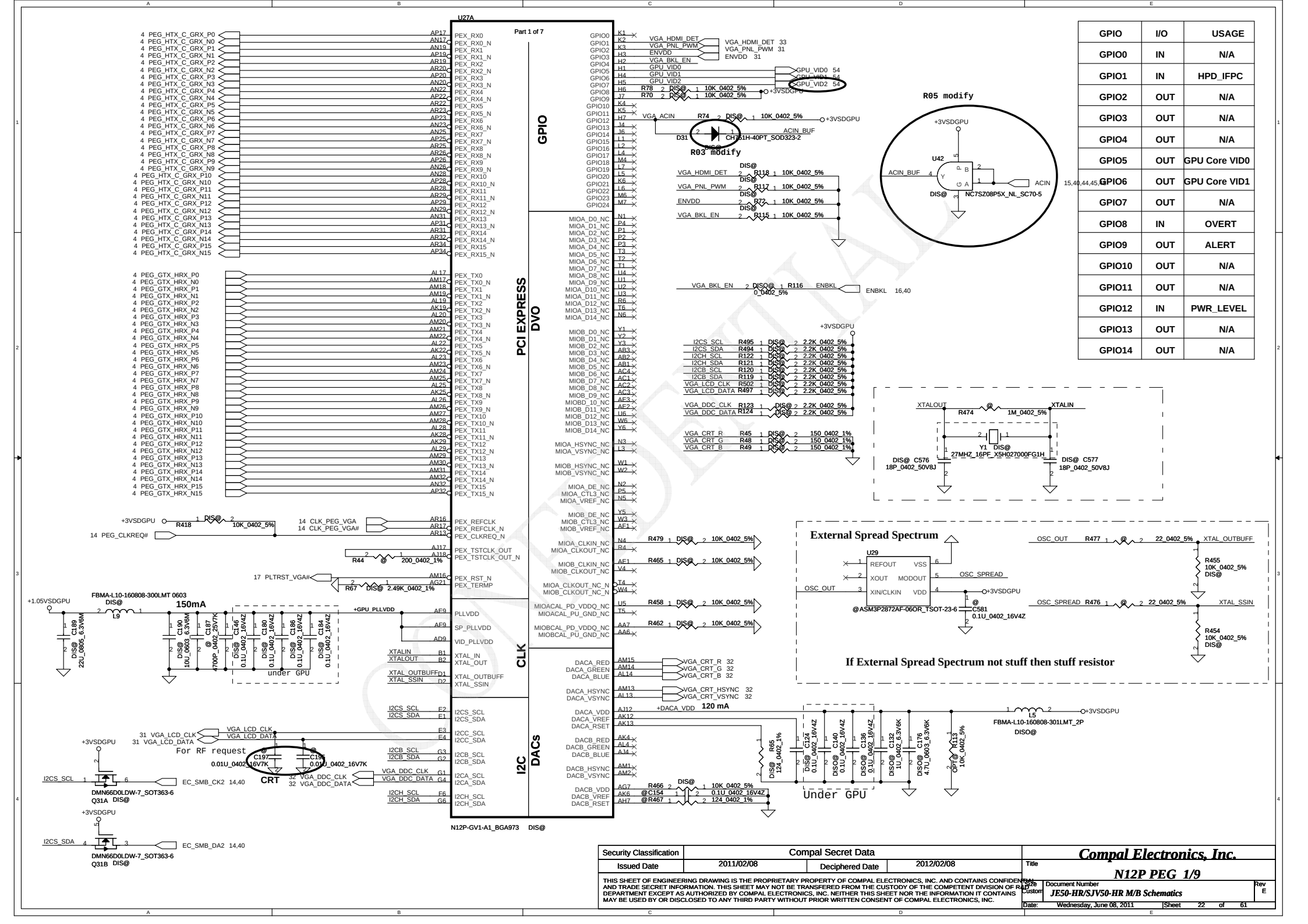
Date: Wednesday, June 08, 2011 | Sheet 21 of 61



GPIO	I/O	USAGE
GPIO0	IN	N/A
GPIO1	IN	HPD_IFPC
GPIO2	OUT	N/A
GPIO3	OUT	N/A
GPIO4	OUT	N/A
GPIO5	OUT	GPU Core VID0
GPIO6	OUT	GPU Core VID1
GPIO7	OUT	N/A
GPIO8	IN	OVERT
GPIO9	OUT	ALERT
GPIO10	OUT	N/A
GPIO11	OUT	N/A
GPIO12	IN	PWR_LEVEL
GPIO13	OUT	N/A
GPIO14	OUT	N/A

Security Classification	Compal Secret Data		
Issued Date	2011/02/08	Deciphered Date	2012/02/08

Compal Electronics, Inc.

Title: N12P PEG 1/9

Size: Custom | Document Number: JE50-HR/SJV50-HR M/B Schematics | Rev: E

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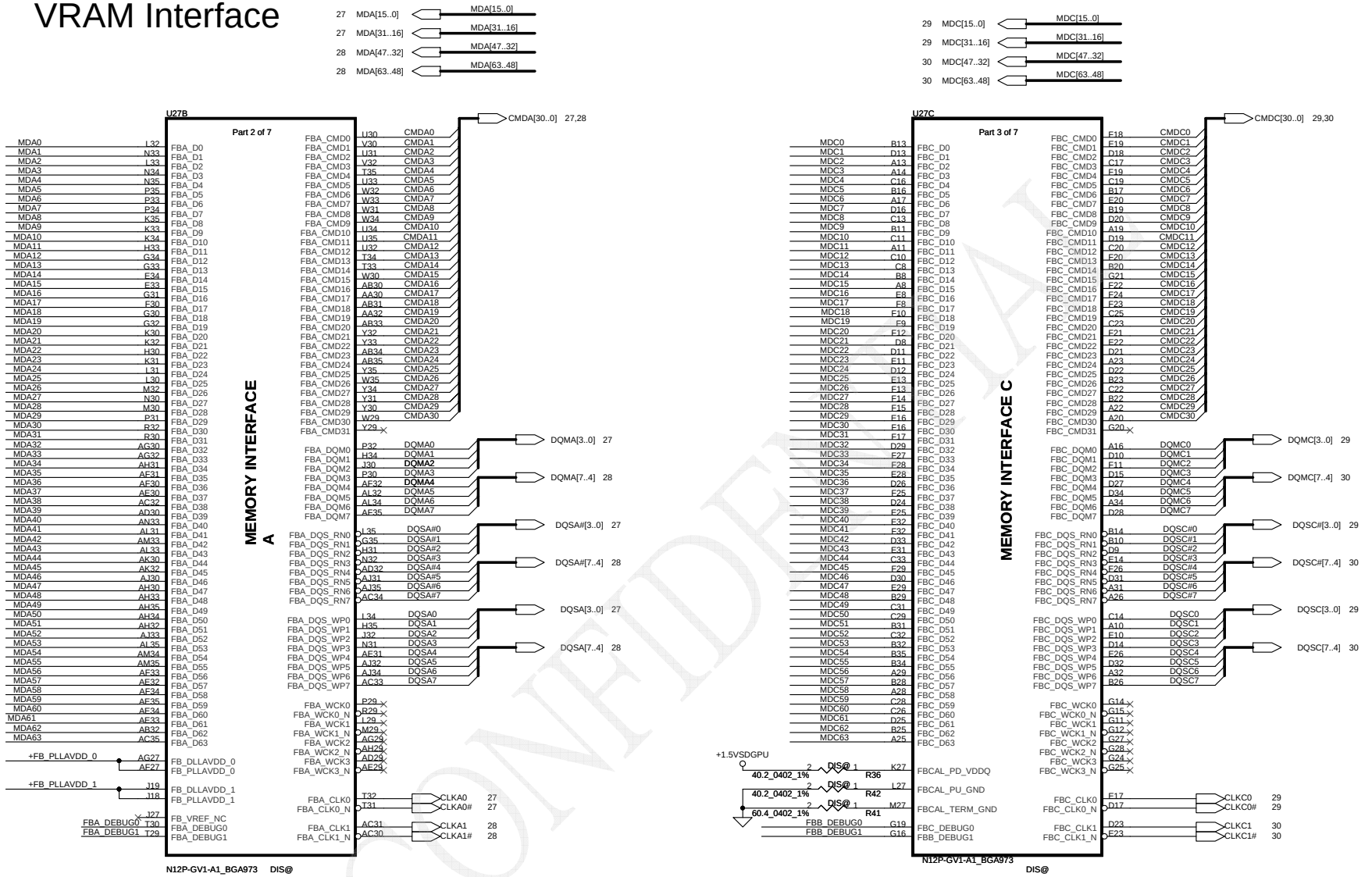
VRAM Interface



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Title: *N12P VRAM 2/9*

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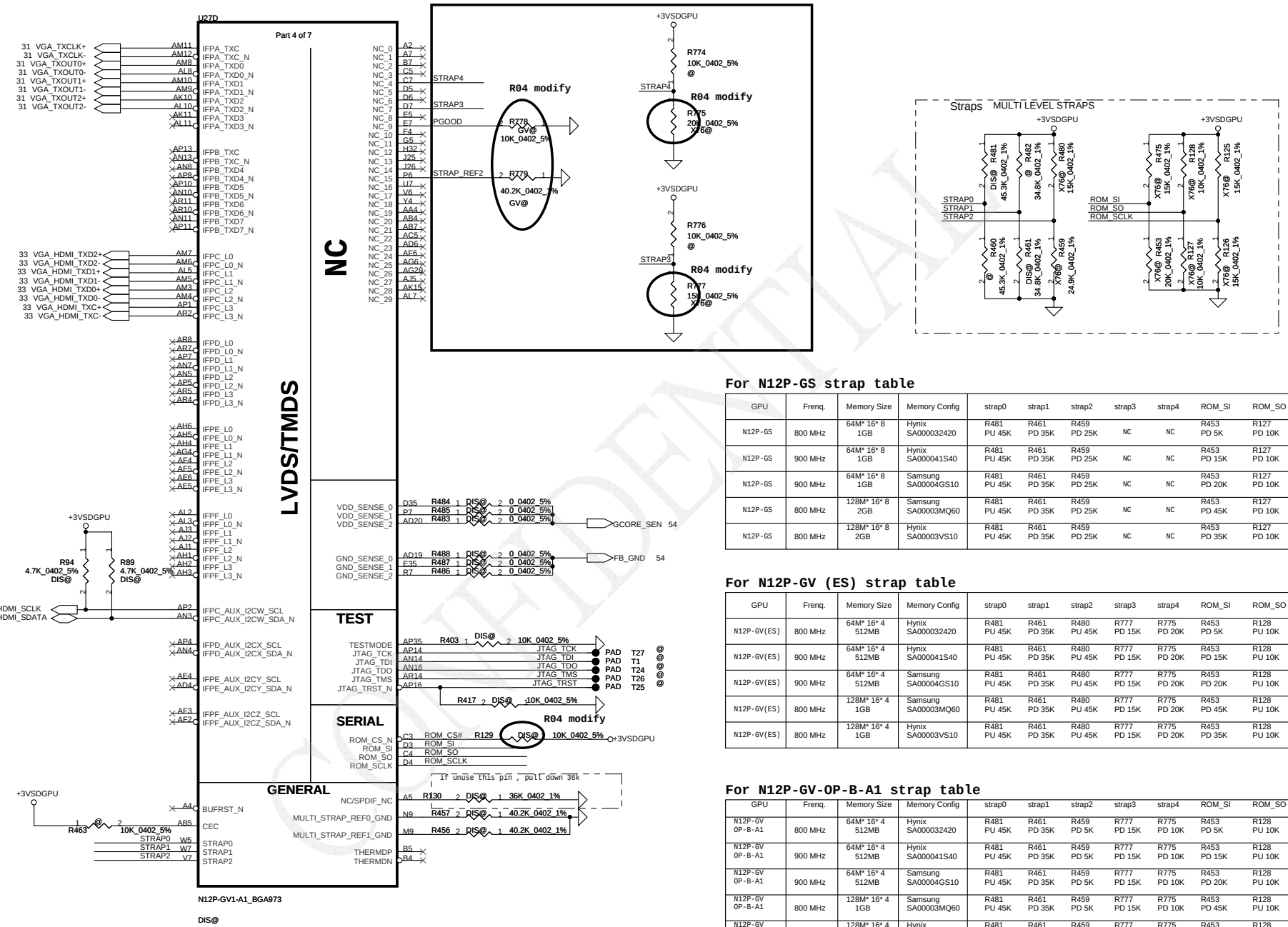
For GB2-128 & GB2b-128 colayout....



For N12P-GS strap table

GPU	Frenq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N12P-GS	800 MHz	64M* 16* 8 1GB	Hynix SA000032420	R481 PU 45K	R461 PD 35K	R459 PD 25K	NC	NC	R453 PD 5K	R127 PD 10K	R125 PU 15K
N12P-GS	900 MHz	64M* 16* 8 1GB	Hynix SA000041S40	R481 PU 45K	R461 PD 35K	R459 PD 25K	NC	NC	R453 PD 15K	R127 PD 10K	R125 PU 15K
N12P-GS	900 MHz	64M* 16* 8 1GB	Samsung SA00004GS10	R481 PU 45K	R461 PD 35K	R459 PD 25K	NC	NC	R453 PD 20K	R127 PD 10K	R125 PU 15K
N12P-GS	800 MHz	128M* 16* 8 2GB	Samsung SA00003MQ60	R481 PU 45K	R461 PD 35K	R459 PD 25K	NC	NC	R453 PD 45K	R127 PD 10K	R125 PU 15K
N12P-GS	800 MHz	128M* 16* 8 2GB	Hynix SA00003VS10	R481 PU 45K	R461 PD 35K	R459 PD 25K	NC	NC	R453 PD 35K	R127 PD 10K	R125 PU 15K

For N12P-GV (ES) strap table

GPU	Frenq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N12P-GV(ES)	800 MHz	64M* 16* 4 512MB	Hynix SA000032420	R481 PU 45K	R461 PD 35K	R480 PU 45K	R777 PD 15K	R775 PD 20K	R453 PD 5K	R128 PU 10K	R125 PU 15K
N12P-GV(ES)	900 MHz	64M* 16* 4 512MB	Hynix SA000041S40	R481 PU 45K	R461 PD 35K	R480 PU 45K	R777 PD 15K	R775 PD 20K	R453 PD 15K	R128 PU 10K	R125 PU 15K
N12P-GV(ES)	900 MHz	64M* 16* 4 512MB	Samsung SA00004GS10	R481 PU 45K	R461 PD 35K	R480 PU 45K	R777 PD 15K	R775 PD 20K	R453 PD 20K	R128 PU 10K	R125 PU 15K
N12P-GV(ES)	800 MHz	128M* 16* 4 1GB	Samsung SA00003MQ60	R481 PU 45K	R461 PD 35K	R480 PU 45K	R777 PD 15K	R775 PD 20K	R453 PD 45K	R128 PU 10K	R125 PU 15K
N12P-GV(ES)	800 MHz	128M* 16* 4 1GB	Hynix SA00003VS10	R481 PU 45K	R461 PD 35K	R480 PU 45K	R777 PD 15K	R775 PD 20K	R453 PD 35K	R128 PU 10K	R125 PU 15K

For N12P-GV-OP-B-A1 strap table

GPU	Frenq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N12P-GV OP-B-A1	800 MHz	64M* 16* 4 512MB	Hynix SA000032420	R481 PU 45K	R461 PD 35K	R459 PD 5K	R777 PD 15K	R775 PD 10K	R453 PD 5K	R128 PU 10K	R125 PU 5K
N12P-GV OP-B-A1	900 MHz	64M* 16* 4 512MB	Hynix SA000041S40	R481 PU 45K	R461 PD 35K	R459 PD 5K	R777 PD 15K	R775 PD 10K	R453 PD 15K	R128 PU 10K	R125 PU 5K
N12P-GV OP-B-A1	900 MHz	64M* 16* 4 512MB	Samsung SA00004GS10	R481 PU 45K	R461 PD 35K	R459 PD 5K	R777 PD 15K	R775 PD 10K	R453 PD 20K	R128 PU 10K	R125 PU 5K
N12P-GV OP-B-A1	800 MHz	128M* 16* 4 1GB	Samsung SA00003MQ60	R481 PU 45K	R461 PD 35K	R459 PD 5K	R777 PD 15K	R775 PD 10K	R453 PD 45K	R128 PU 10K	R125 PU 5K
N12P-GV OP-B-A1	800 MHz	128M* 16* 4 1GB	Hynix SA00003VS10	R481 PU 45K	R461 PD 35K	R459 PD 5K	R777 PD 15K	R775 PD 10K	R453 PD 35K	R128 PU 10K	R125 PU 5K

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Issued Date	2011/02/08	Deciphered Date 2012/02/08	Title N12P LVDS 3/9
			Size Custom; Document Number JE50-HR/SJV50-HR M/B Schematics; Rev E
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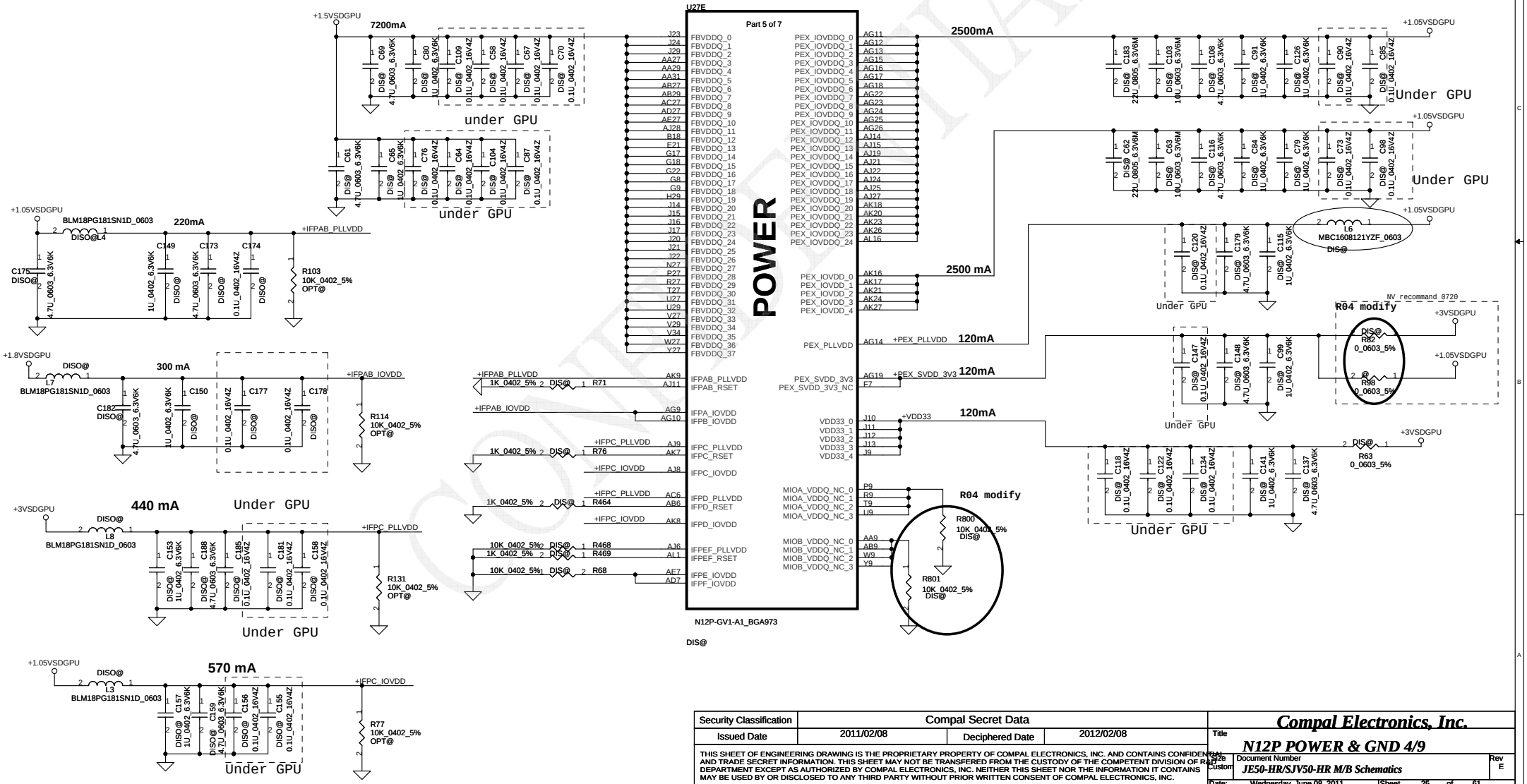

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Issued Date	2011/02/08	Deciphered Date	2012/02/08

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Title: N12P POWER & GND 4/9			
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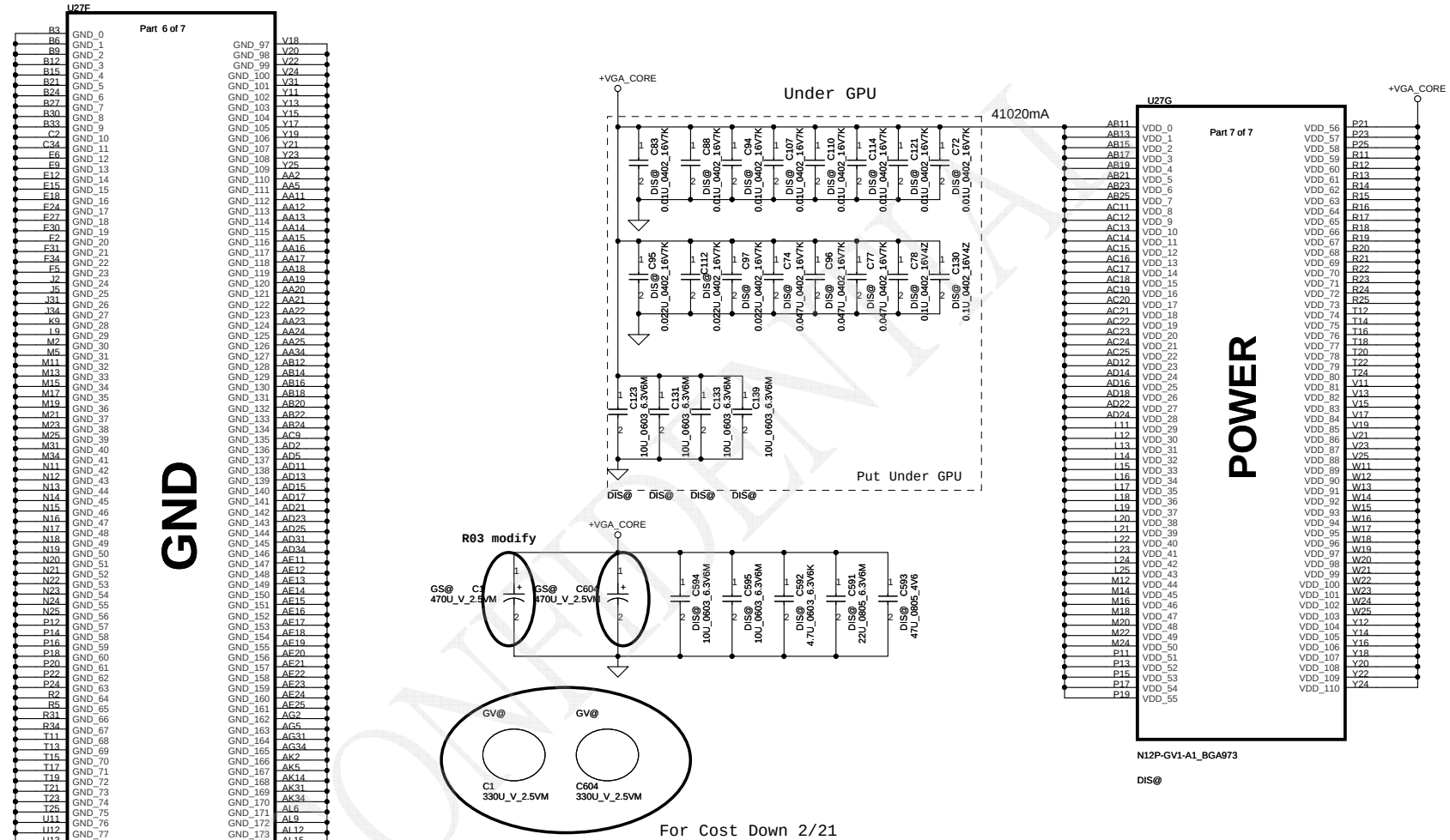

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Title: N12P POWER & GND 5/9			
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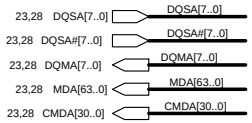
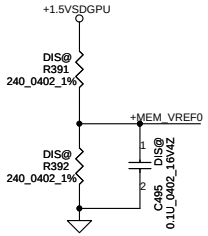
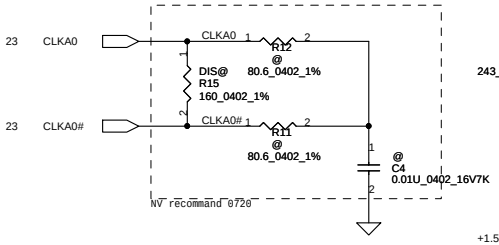
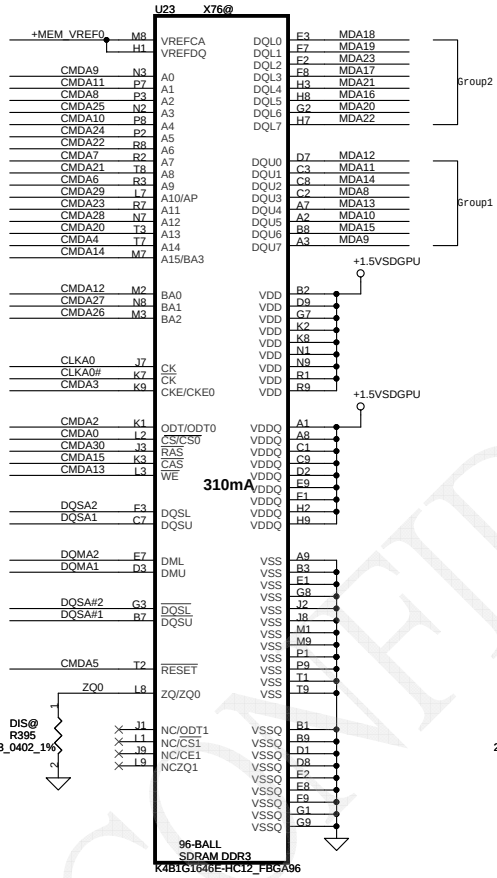
VRAM DDR3 chips (1GB)

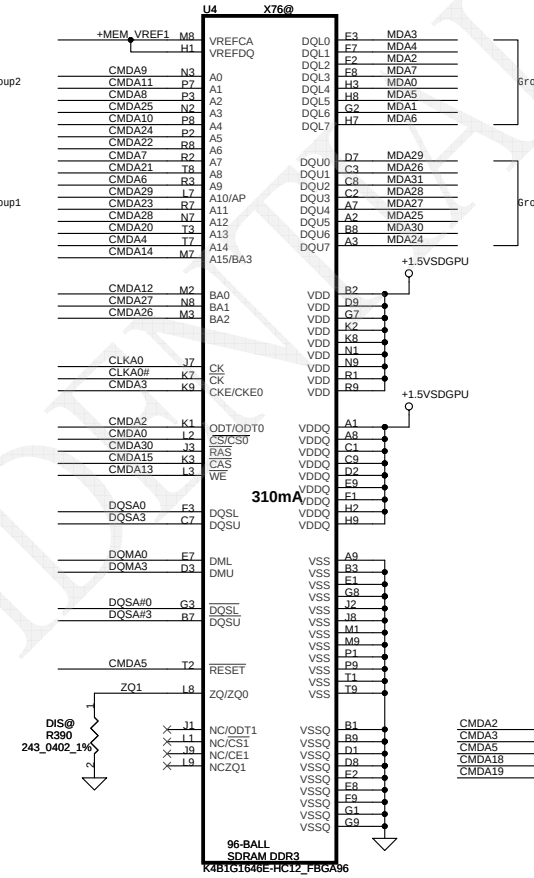
64Mx16 DDR3 *8==>1GB

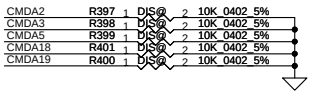




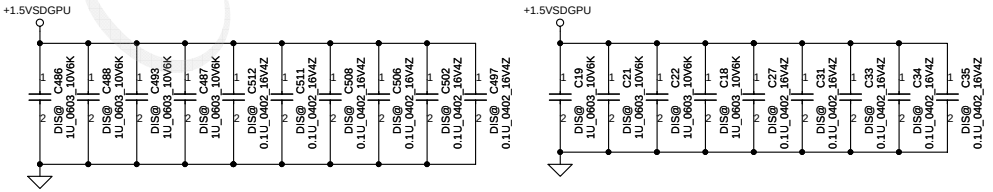








	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination



Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
	LOW	HIGH

Samsung : SA000035700 (S IC D3 64MX16 K4W1G1646E-HC12 FBGA 96P)
Hynix : SA000032400 (S IC D3 64MX16 H5TQ1G63BFR-12C FBGA 1.5V)
AMD :SA00003PF10
(S IC D3 64M16/800 23EY2387MB-12 PG-TFBGA 96P 1.5V)

Security Classification	Compal Secret Data		
Issued Date	2011/02/08	Deciphered Date	2012/02/08

Compal Electronics, Inc.

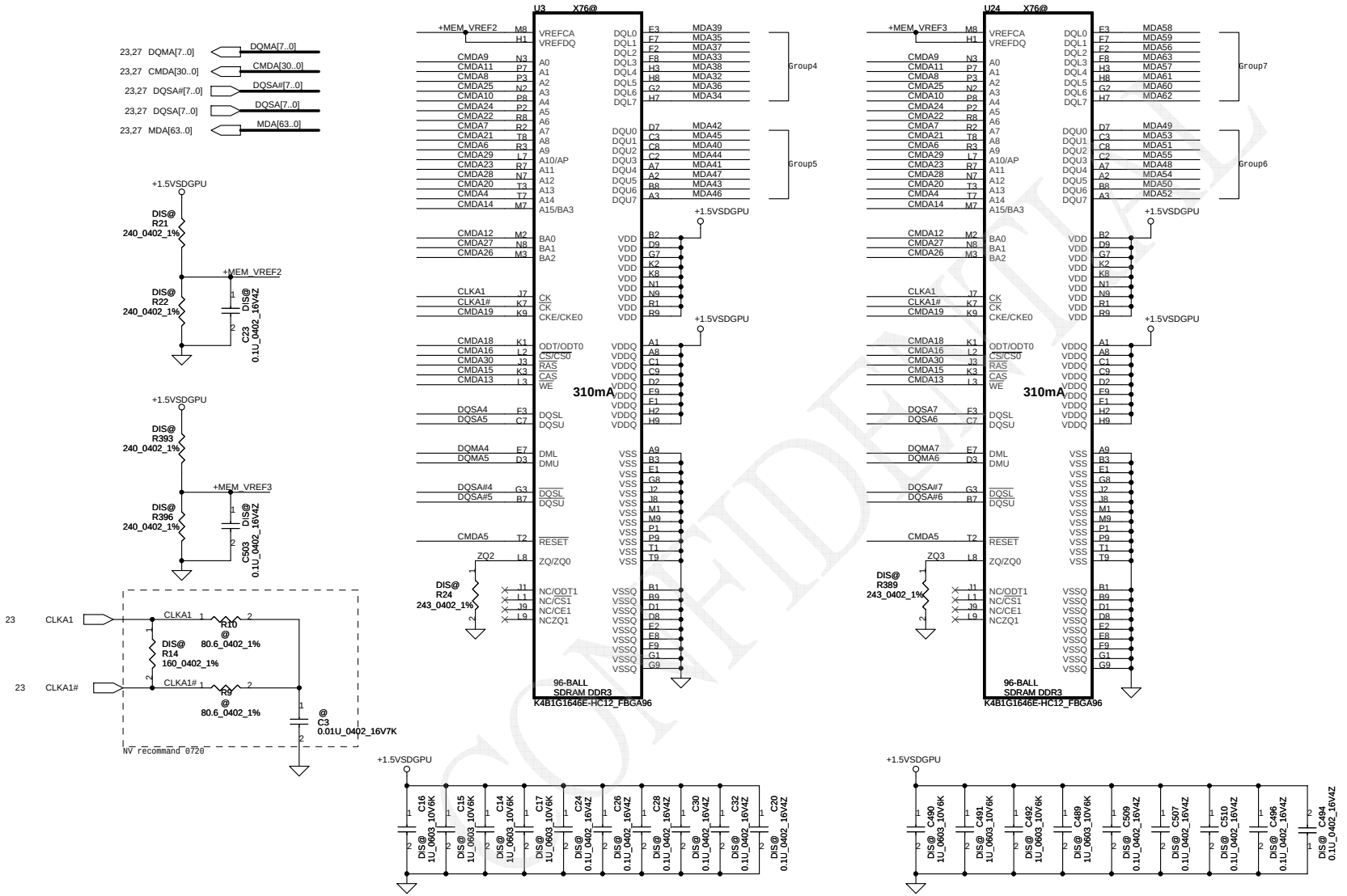
Title: N12P DDR3 6/9

Size: Custom | Document Number: JE50-HR/SJV50-HR M/B Schematics | Rev: E

Date: Wednesday, June 08, 2011 | Sheet 27 of 61

VRAM DDR3 chips (1GB)

64Mx16 DDR3 *8==>1GB

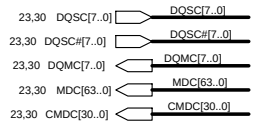


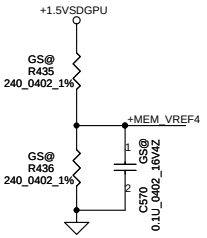
Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
	LOW	HIGH

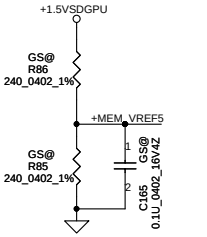
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/02/08	Deciphered Date 2012/02/08	Title: N12P DDR3 7/9
Size: Custom	Document Number: JE50-HR/SJV50-HR M/B Schematics		Rev: E
Date: Wednesday, June 08, 2011	Sheet 28 of 61		

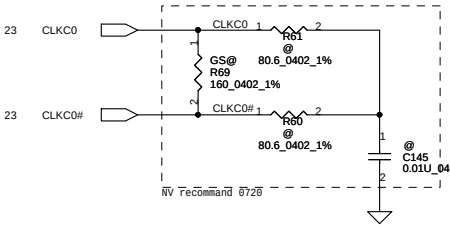
VRAM DDR3 chips (1GB)

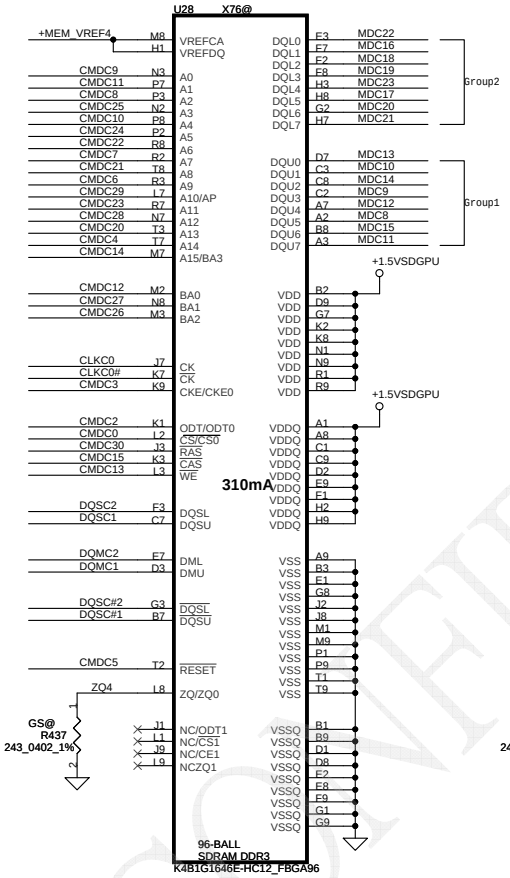
64Mx16 DDR3 *8==>1GB

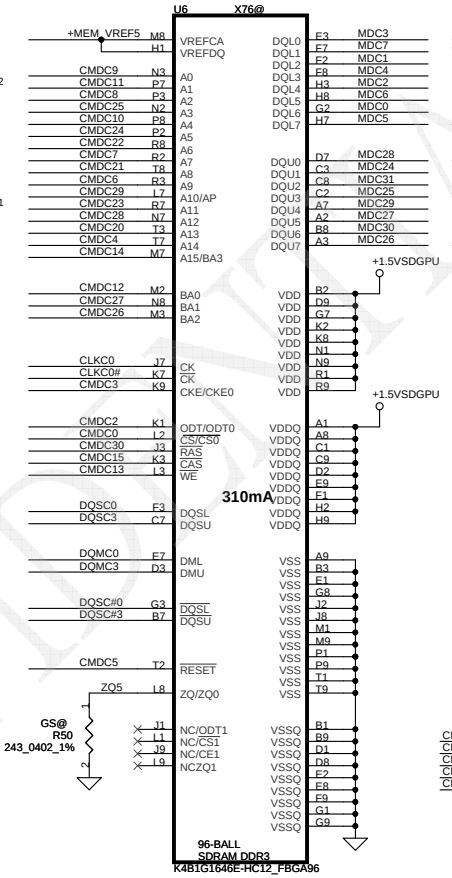


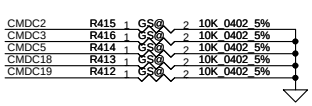






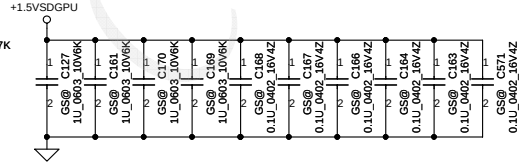


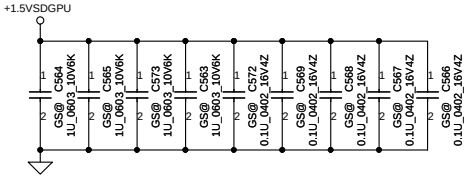




Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
	LOW	HIGH

	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination





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Size: Custom	Document Number: JE50-HR/SJV50-HR M/B Schematics		Rev: E
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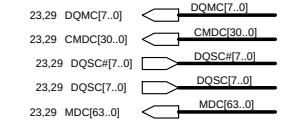
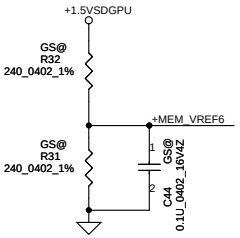
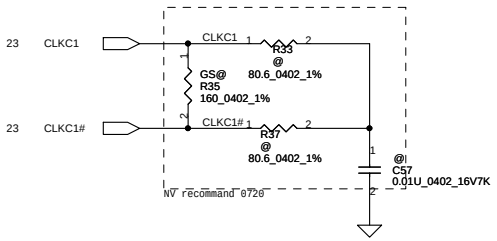
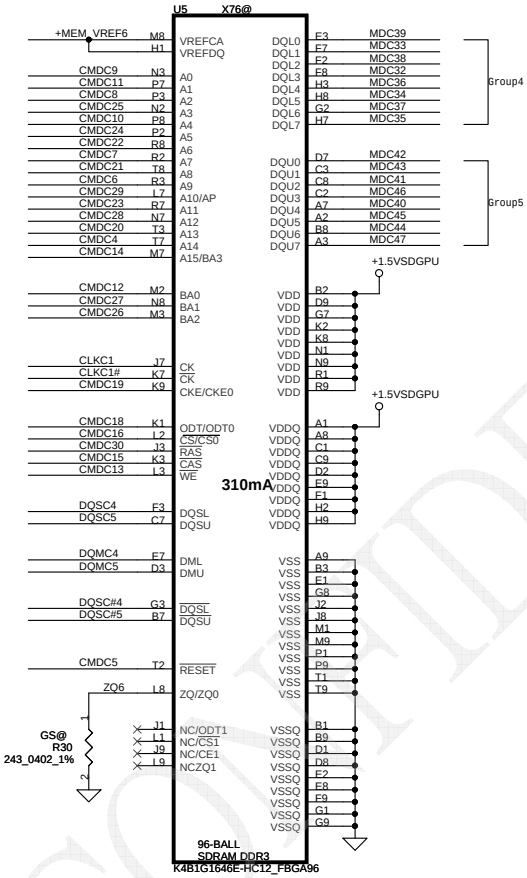
VRAM DDR3 chips (1GB)

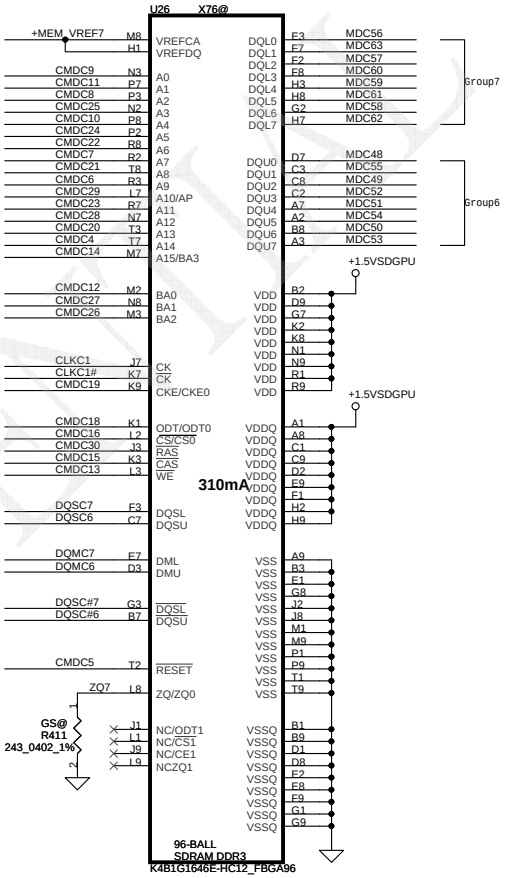
64Mx16 DDR3 *8==>1GB

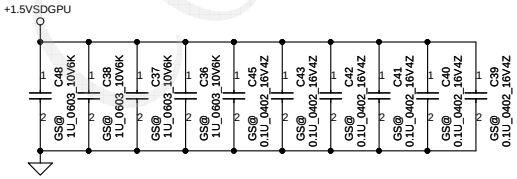


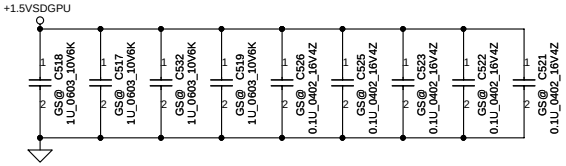












Mode D Address	0..31	32..63
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CMD5	RST	RST
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CMD7	A7	A7
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CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
	LOW	HIGH

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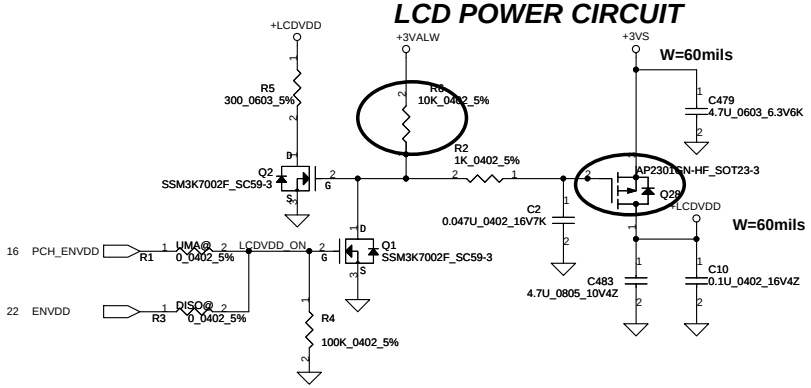
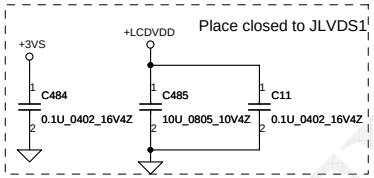
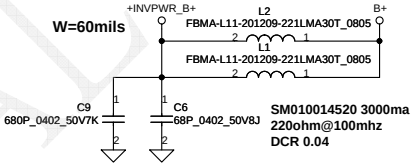
			Date: Wednesday, June 08, 2011 / Sheet 30 of 61

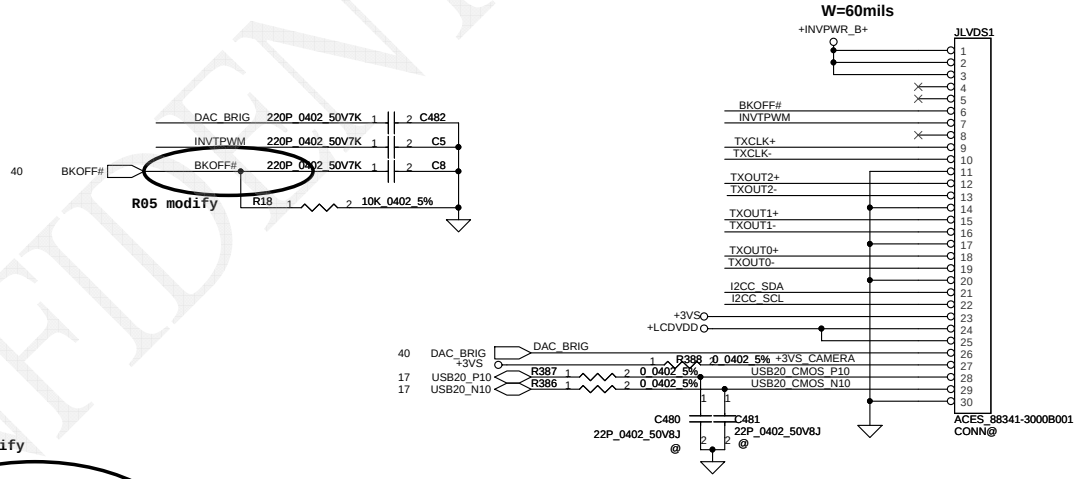
LCD POWER CIRCUIT



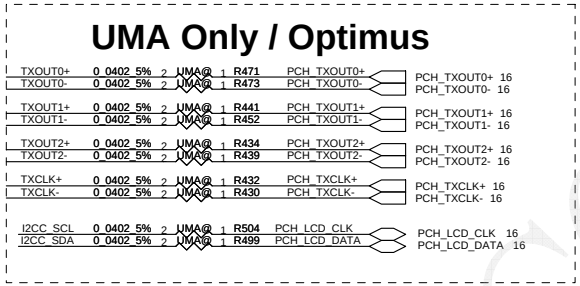




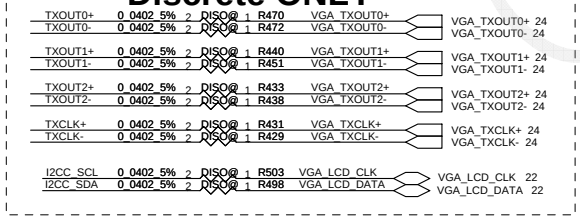
LCD/LED PANEL Conn.

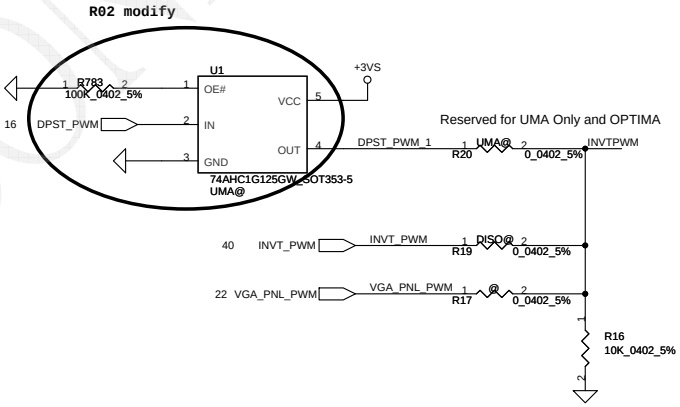


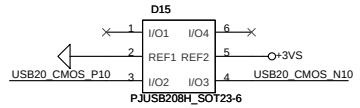
UMA Only / Optimus



Discrete ONLY







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Issued Date	2011/02/08	Deciphered Date	2012/02/08

Compal Electronics, Inc.	
Title	LVDS Connector
Size: Custom	Document Number: JE50-HR/SJV50-HR M/B Schematics
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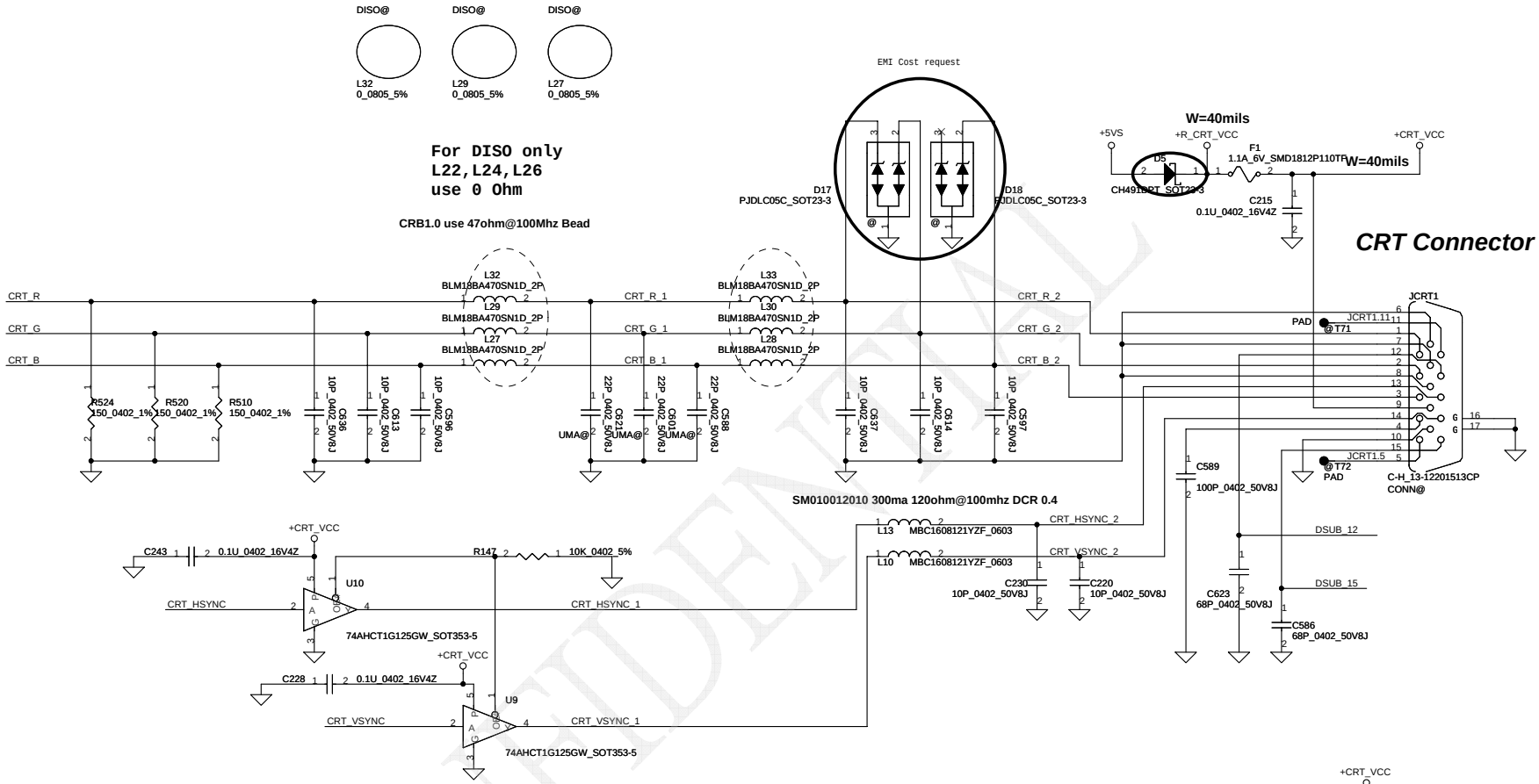
Date: Wednesday, June 08, 2011	Sheet 31 of 61



UMA Only / OPTIMUS

16	PCH_CRT_R	PCH_CRT_R	R420	UMA@	0_0402_5%	CRT_R
16	PCH_CRT_G	PCH_CRT_G	R424	UMA@	0_0402_5%	CRT_G
16	PCH_CRT_B	PCH_CRT_B	R422	UMA@	0_0402_5%	CRT_B
16	PCH_CRT_HSYNC	PCH_CRT_HSYNC	R428	UMA@	33_0402_5%	CRT_HSYNC
16	PCH_CRT_VSYNC	PCH_CRT_VSYNC	R426	UMA@	33_0402_5%	CRT_VSYNC
16	PCH_CRT_CLK	PCH_CRT_CLK	R506	UMA@	0_0402_5%	CRT_DDC_CLK
16	PCH_CRT_DATA	PCH_CRT_DATA	R501	UMA@	0_0402_5%	CRT_DDC_DATA

Discrete only

22	VGA_CRT_R	VGA_CRT_R	R419	DISO@	0_0402_5%	CRT_R
22	VGA_CRT_G	VGA_CRT_G	R423	DISO@	0_0402_5%	CRT_G
22	VGA_CRT_B	VGA_CRT_B	R421	DISO@	0_0402_5%	CRT_B
22	VGA_CRT_HSYNC	VGA_CRT_HSYNC	R427	DISO@	0_0402_5%	CRT_HSYNC
22	VGA_CRT_VSYNC	VGA_CRT_VSYNC	R425	DISO@	0_0402_5%	CRT_VSYNC
22	VGA_DDC_CLK	VGA_DDC_CLK	R505	DISO@	0_0402_5%	CRT_DDC_CLK
22	VGA_DDC_DATA	VGA_DDC_DATA	R500	DISO@	0_0402_5%	CRT_DDC_DATA

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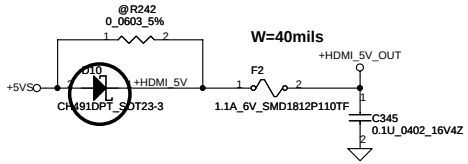
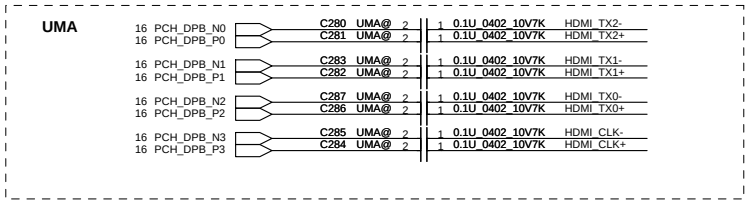
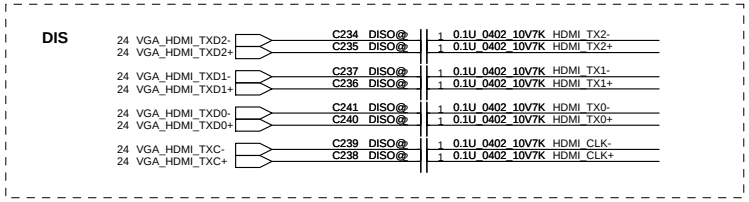
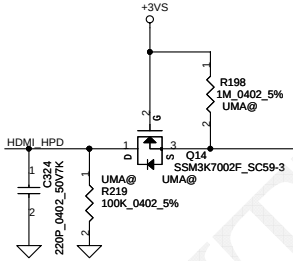
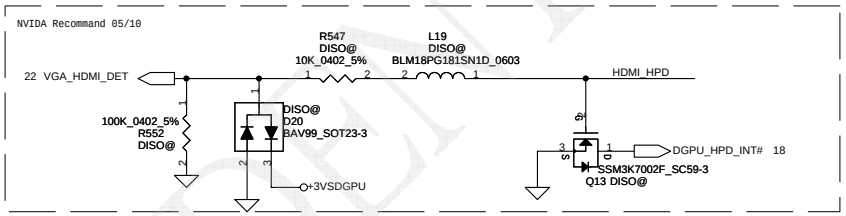
Issued Date	2011/02/08	Deciphered Date 2012/02/08	Title: CRT Connector
Size: Custom	Document Number: JE50-HR/SJV50-HR M/B Schematics		Rev: E
Date: Wednesday, June 08, 2011	Sheet 32 of 61		

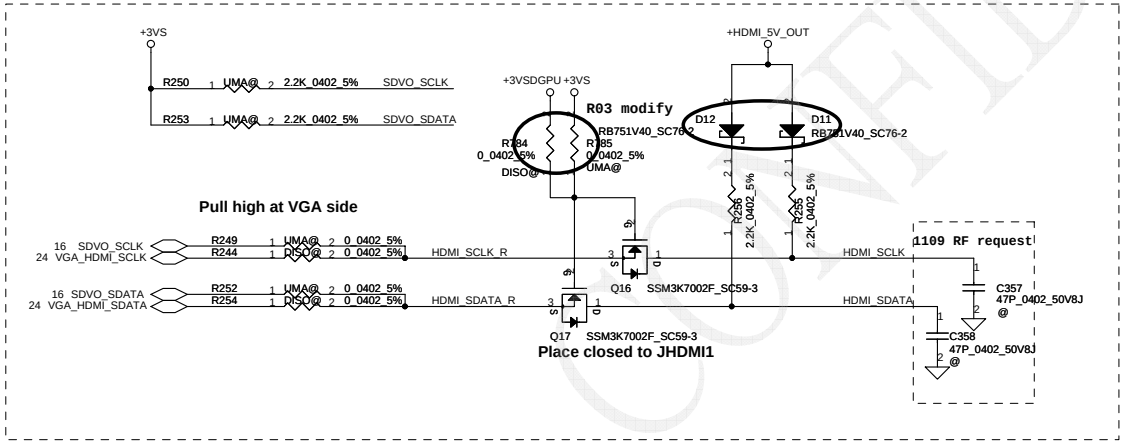


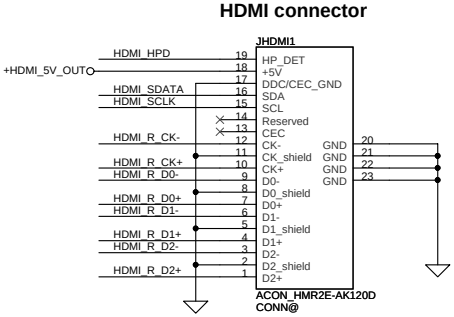


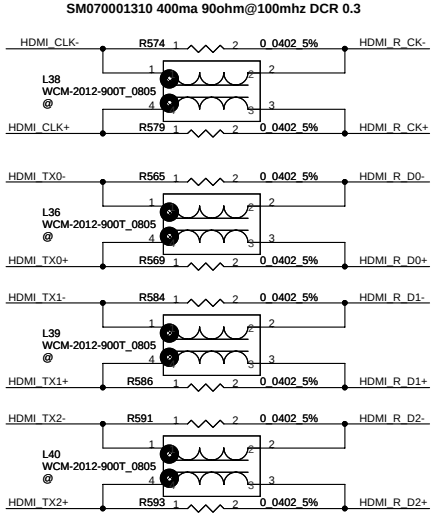


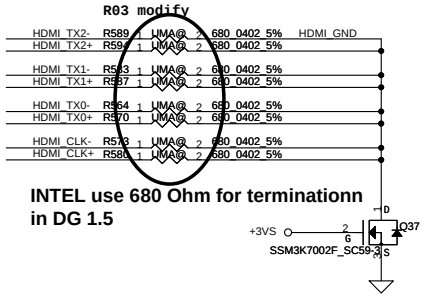


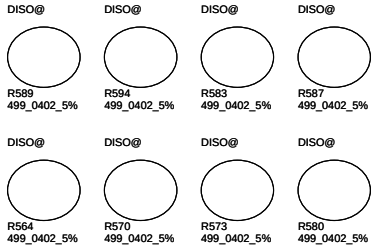












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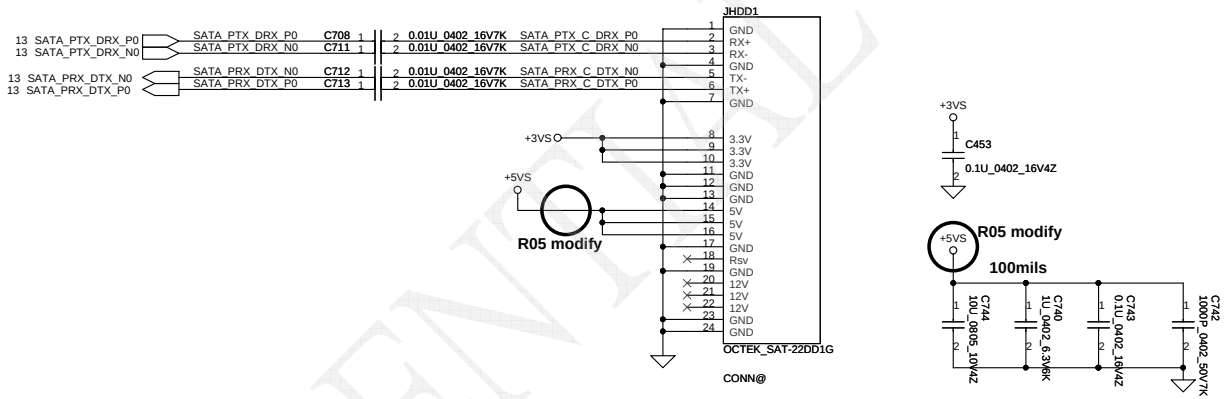
Issued Date	2011/02/08	Deciphered Date 2012/02/08	Title HDMI Conn
Size Custom	Document Number JE50-HR/SJV50-HR M/B Schematics		Rev 1.0
Date: Wednesday, June 08, 2011	Sheet 33 of 61		

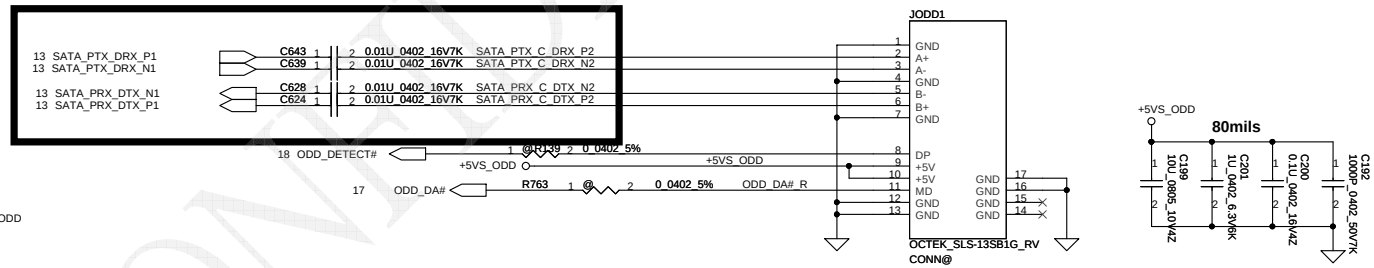
SATA HDD1 Conn.

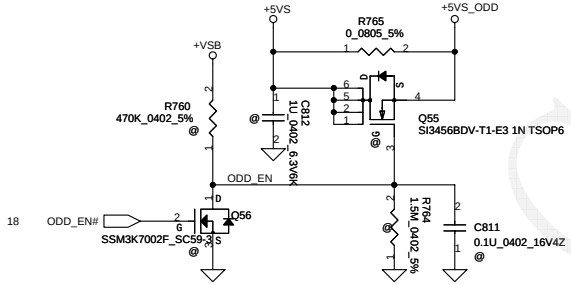
CL 4.0 mm



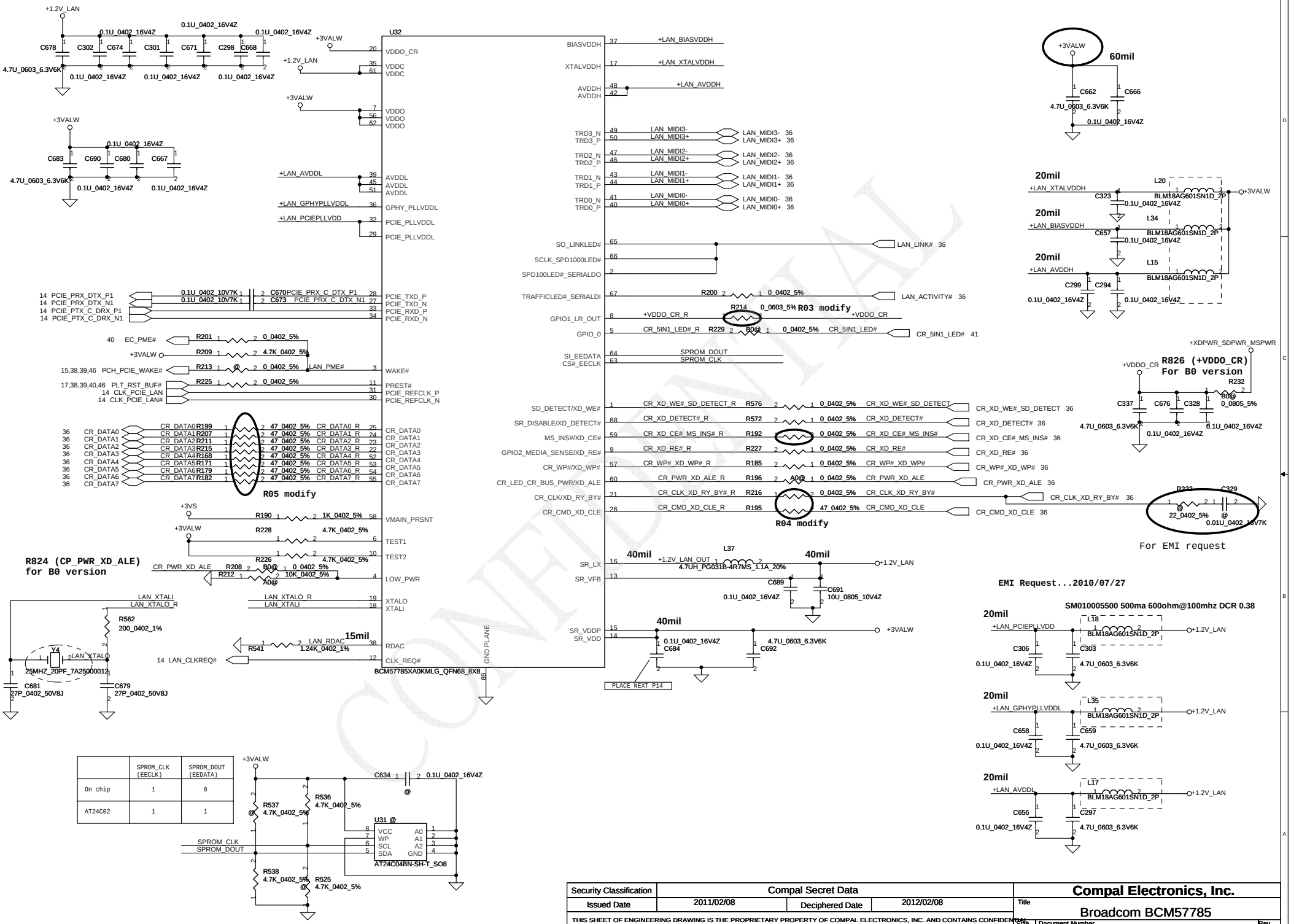
change to port1 cause by intel
SATA II issue (20110201)

SATA ODD Conn.





Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/02/08	Deciphered Date 2012/02/08	Title: HDD & ODD Connector
			Size: Custom; Document Number: JE50-HR/SJV50-HR M/B Schematics; Rev: E
			Date: Wednesday, June 08, 2011; Sheet 34 of 61



	SPROM_CLK (EECLK)	SPROM_DOUT (EEDATA)
On chip	1	0
AT24C02	1	1

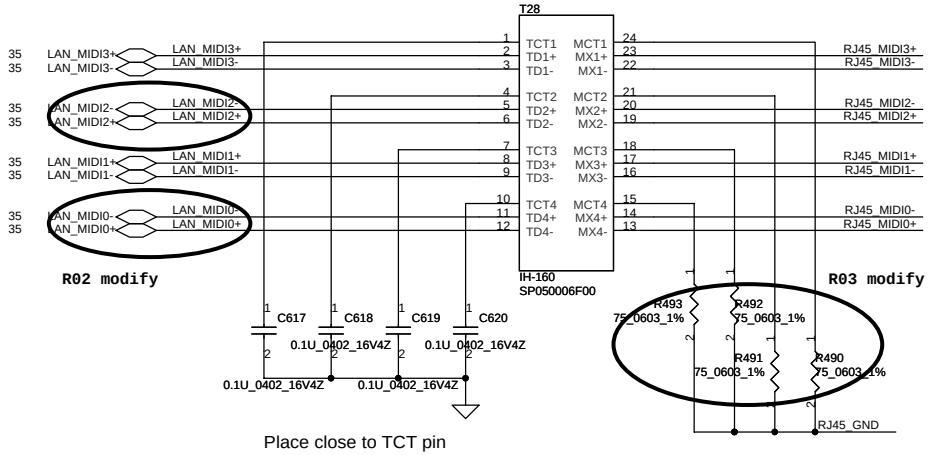
Security Classification	Compal Secret Data		
Issued Date	2011/02/08	Deciphered Date	2012/02/08

Compal Electronics, Inc.

Title: Broadcom BCM57785

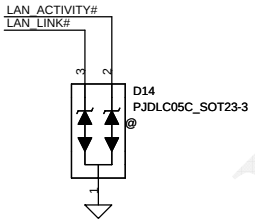
Size: Custom | Document Number: JE50-HR/SJV50-HR M/B Schematics | Rev: E

Date: Wednesday, June 08, 2011 | Sheet 35 of 61



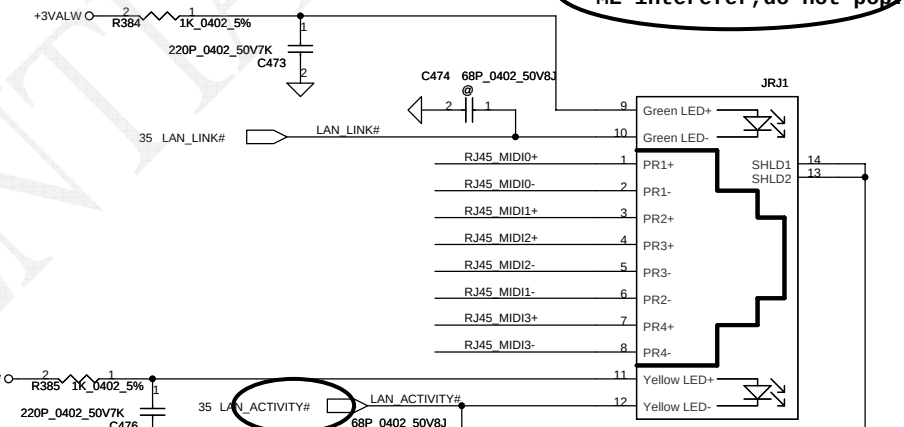
Place close to TCT pin

BOTHHAND: S X'FORM_ GST5009-D LF LAN, SP050006B00
TIMAG:S X'FORM_ IH-160 LAN , SP050006F00



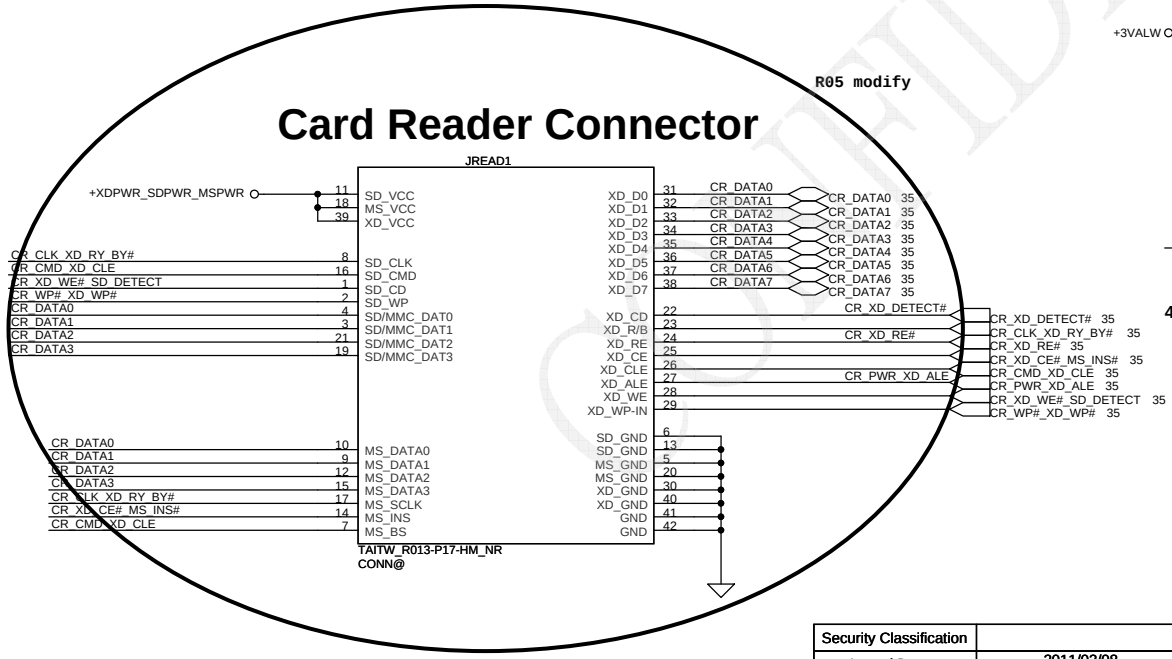
LAN Connector

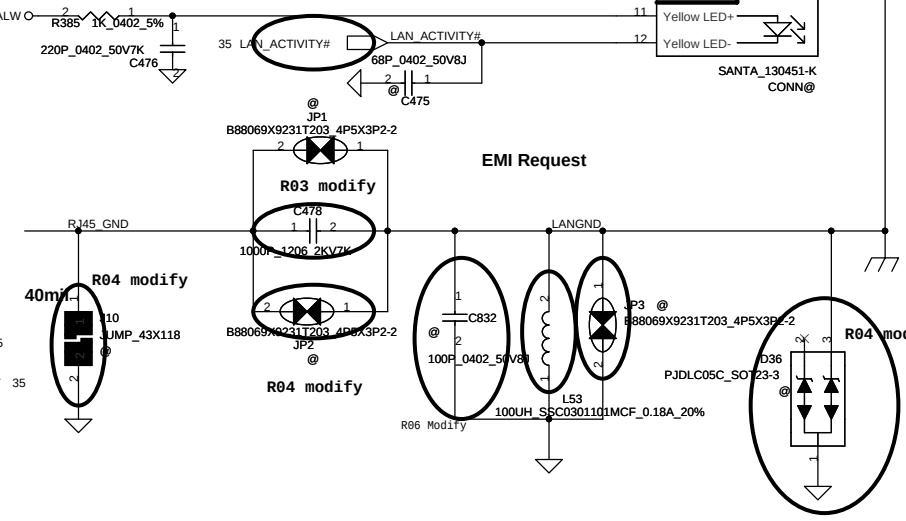
R03 modify
C474,C475 and D14
ME interefer,do not pop!



Card Reader Connector

R05 modify





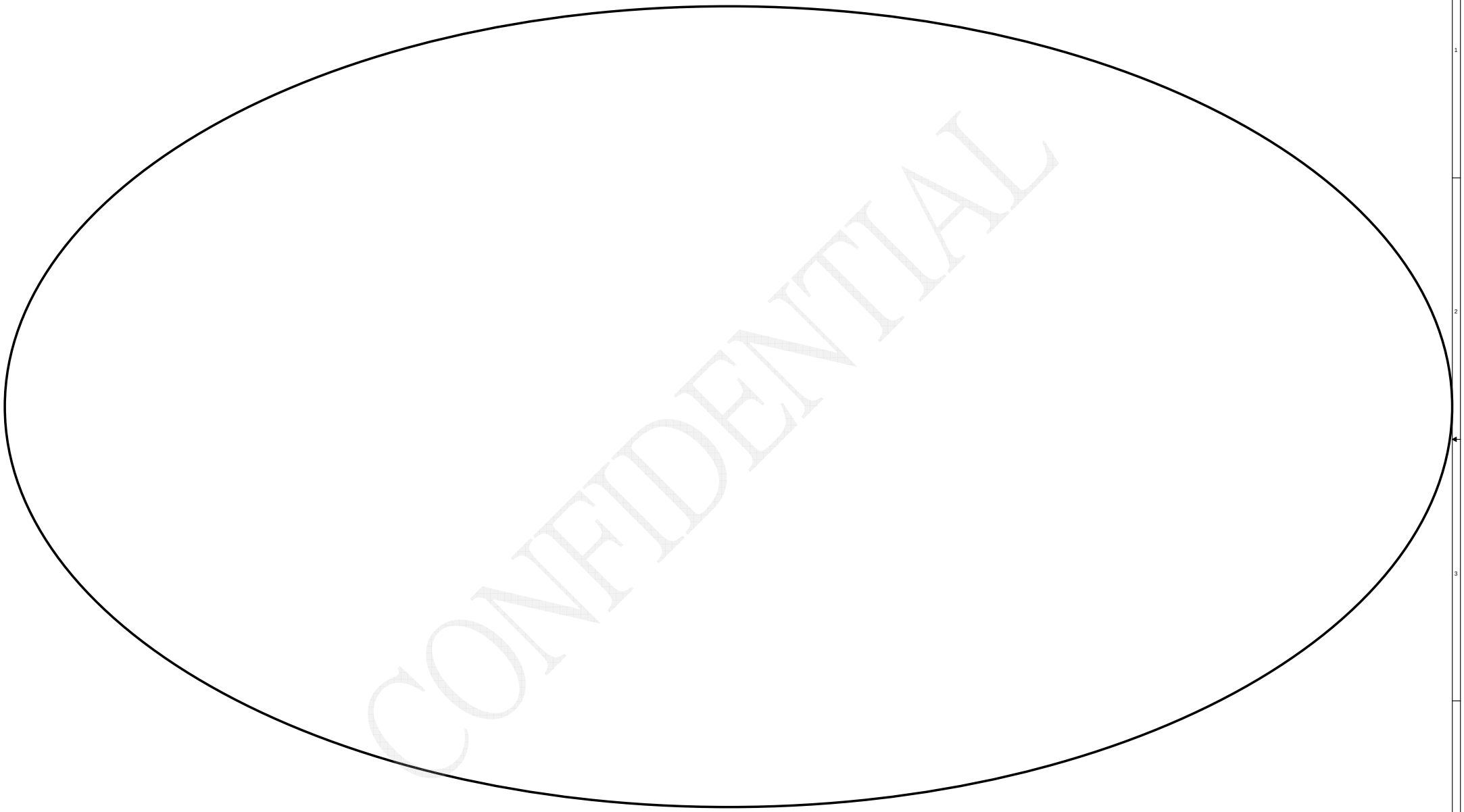
Security Classification	Compal Secret Data		
Issued Date	2011/02/08	Deciphered Date	2012/02/08

Compal Electronics, Inc.

Title: LAN Magnetic & RJ45

Size: Custom | Document Number: JE50-HR/SJV50-HR M/B Schematics | Rev: E

Date: Wednesday, June 08, 2011 | Sheet 36 of 61



Security Classification	Compal Secret Data		
Issued Date	2011/02/08	Deciphered Date	2012/02/08

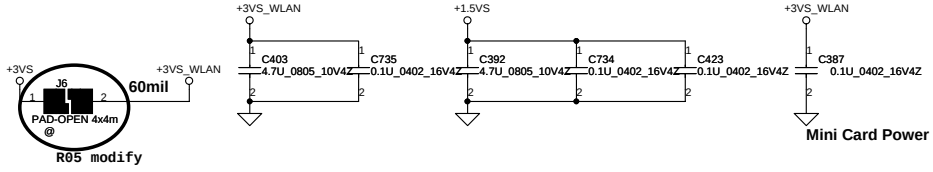
Compal Electronics, Inc.

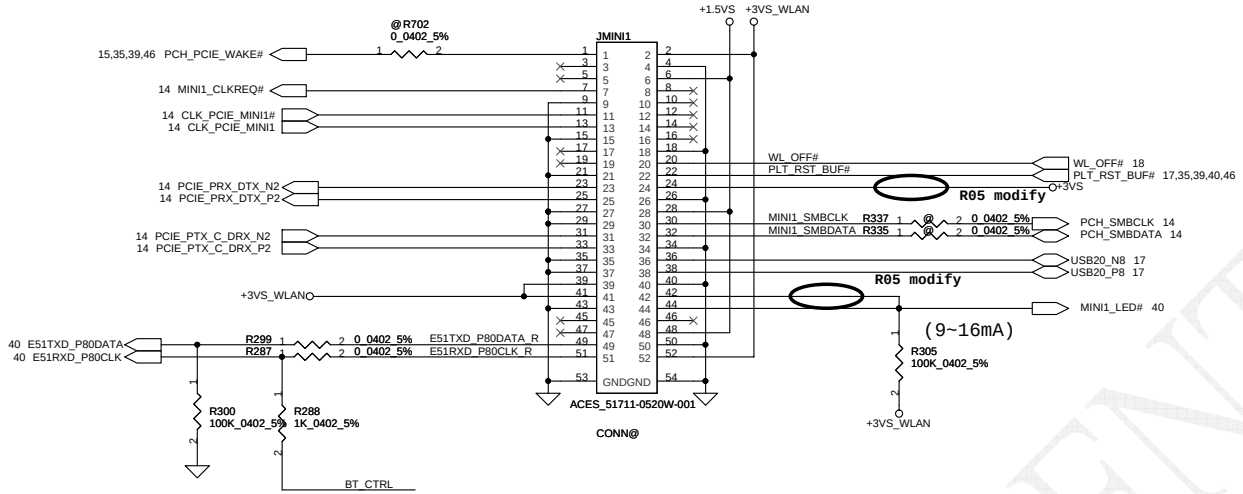
Title: RTS5138 Card Reader

Size	Document Number	Rev
Custom	JE50-HR/SJV50-HR M/B Schematics	E

Date: Wednesday, June 08, 2011 Sheet 37 of 61

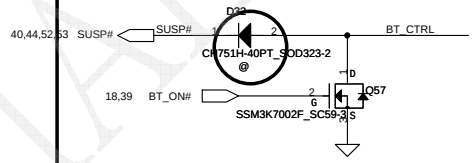
For Wireless LAN



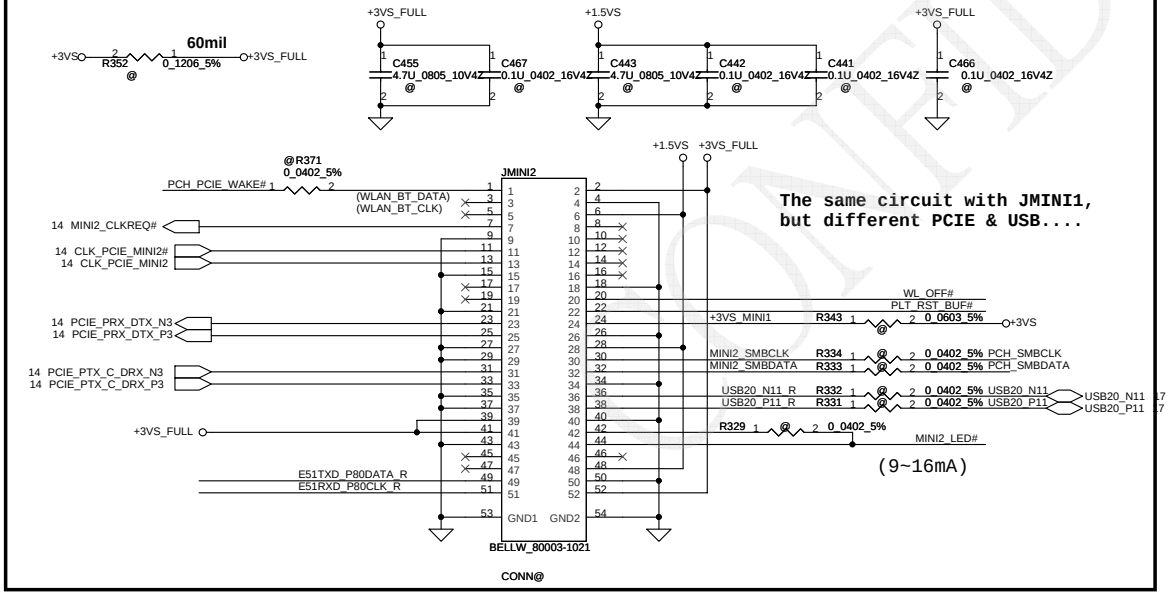


WLAN&BT Combo module circuits

	BT on module Enable	BT on module Disable
BT_CTRL	H	L
BT_ON#	L	H

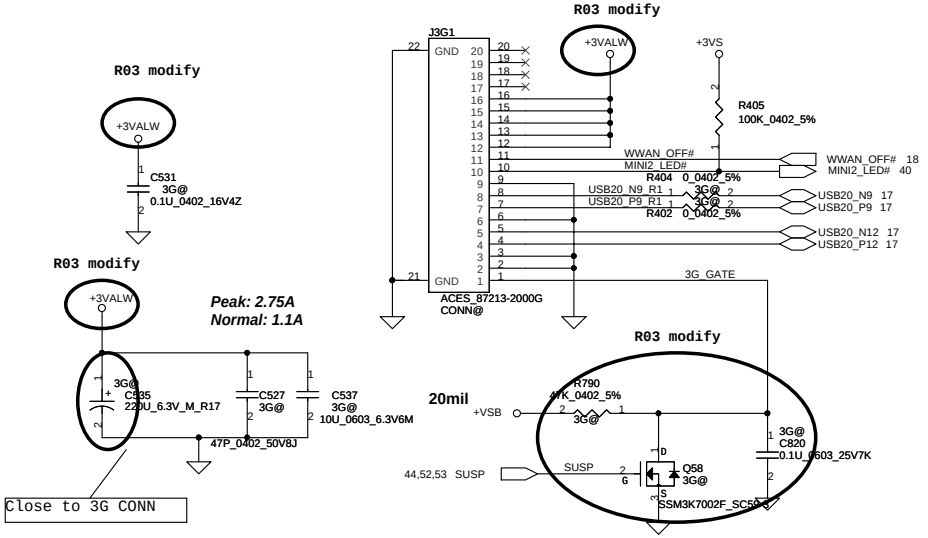


Reserve



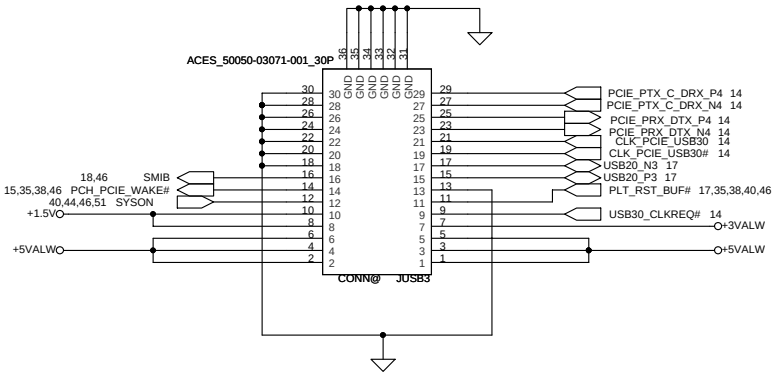
For 3G / GPS

To 3G Module Connect



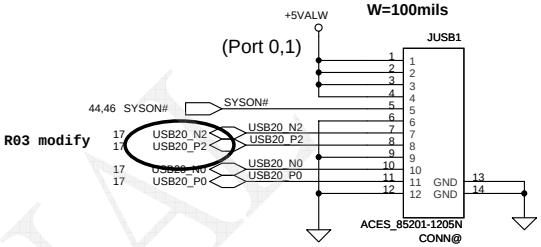
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/02/08	Deciphered Date 2012/02/08	Title: MINI CARD (WLAN & TV-Tuner)
			Size: Custom; Document Number: JE50-HR/SJV50-HR M/B Schematics; Rev: E
			Date: Wednesday, June 08, 2011; Sheet 38 of 61

USB3.0 Conn.

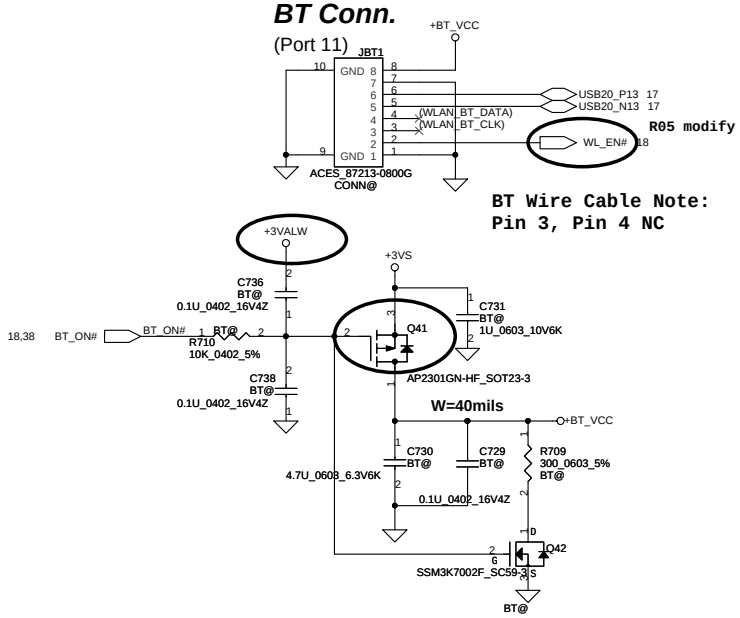


OD output

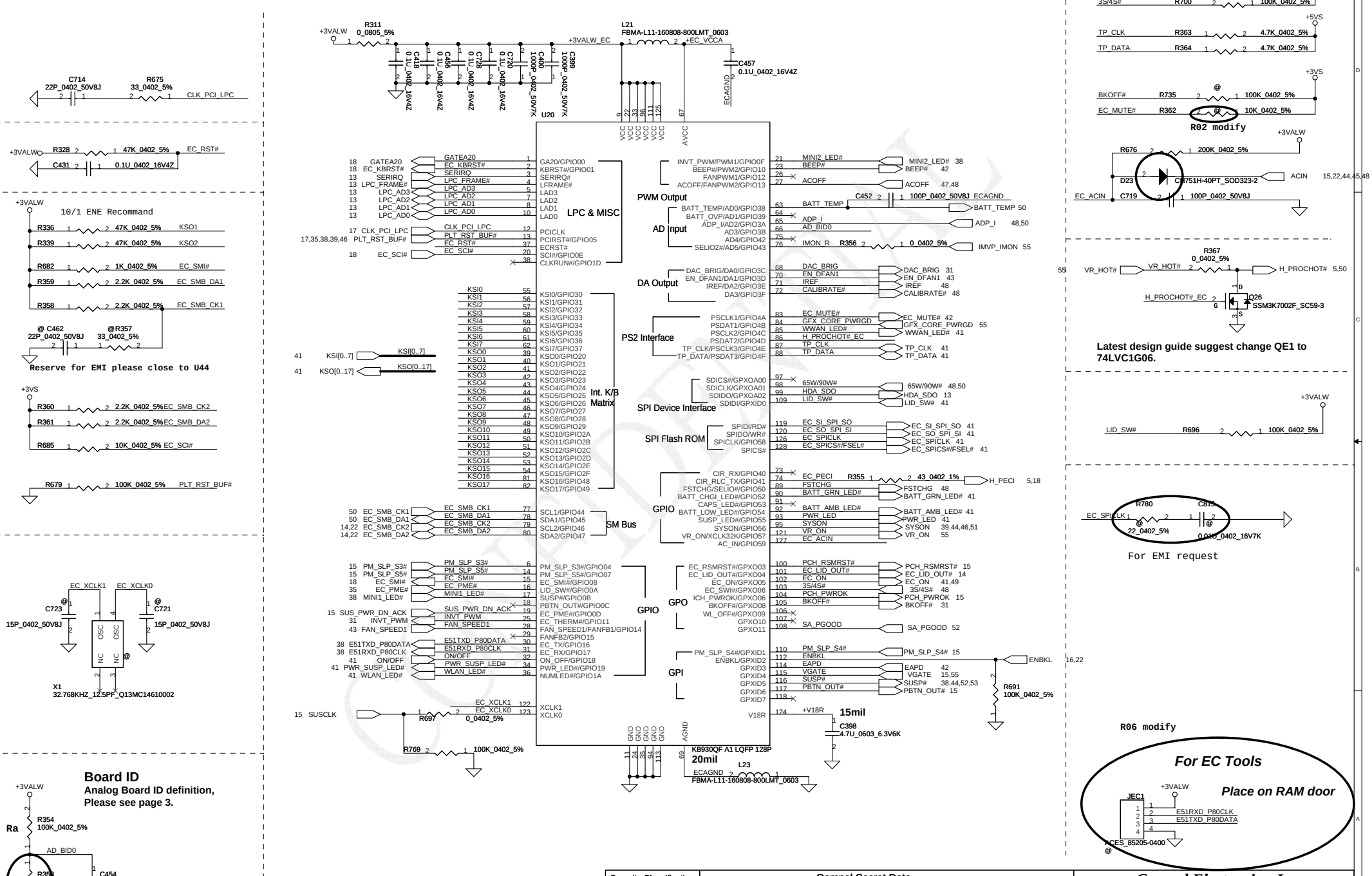
USB/B Conn.



BT Conn.



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/02/08	Deciphered Date 2012/02/08	Title: USB / BT / USBB
			Size: Custom; Document Number: JE50-HR/SJV50-HR M/B Schematics; Rev: E
			Date: Wednesday, June 08, 2011; Sheet 39 of 61



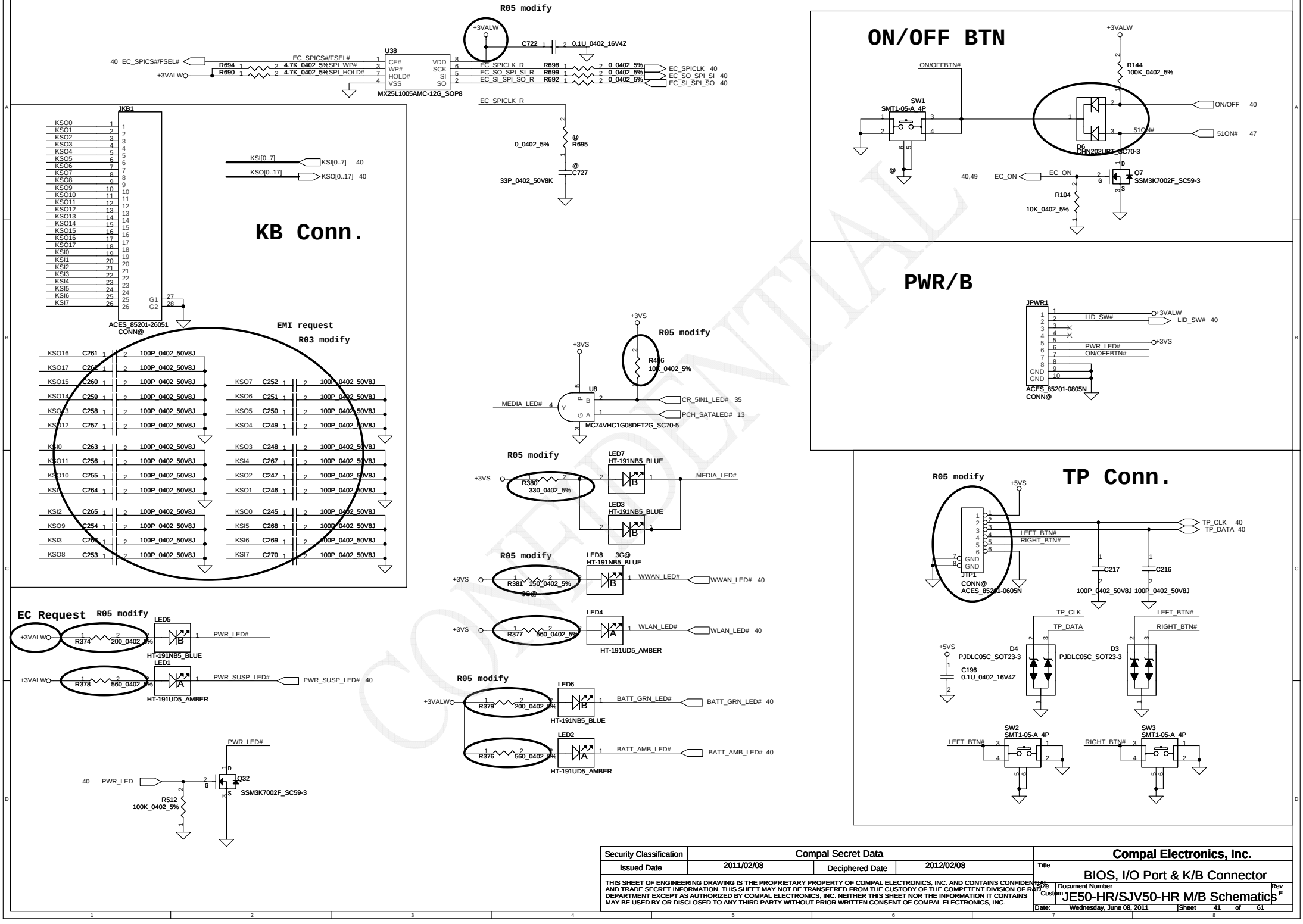
Security Classification	Compal Secret Data		
Issued Date	2011/02/08	Deciphered Date	2012/02/08

Compal Electronics, Inc.

Title: EC ENE-KB930

Size: Custom | Document Number: JE50-HR/SJV50-HR M/B Schematics | Rev: E

Date: Wednesday, June 08, 2011 | Sheet 40 of 61



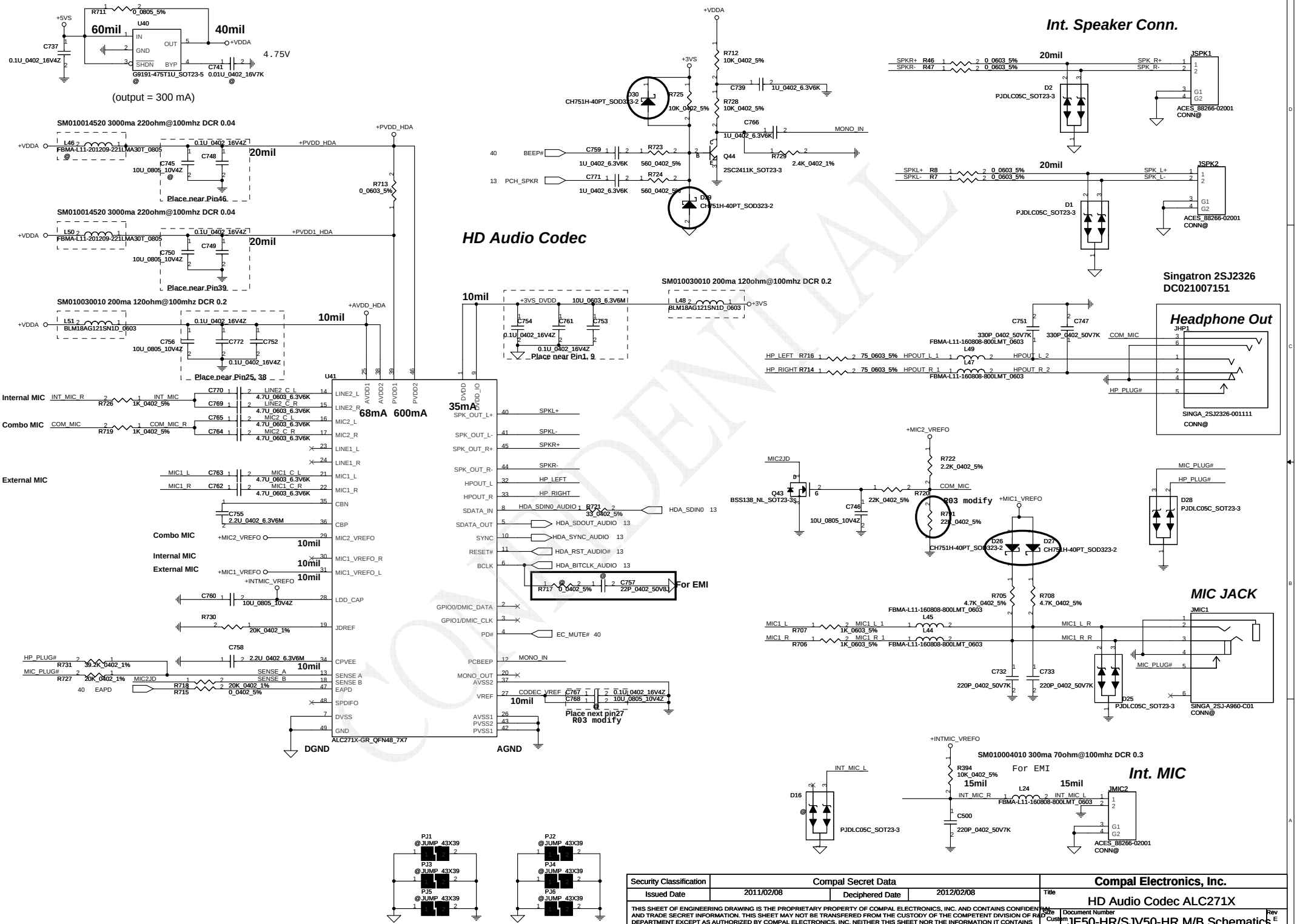
Security Classification	Compal Secret Data		
Issued Date	2011/02/08	Deciphered Date	2012/02/08

Compal Electronics, Inc.

Title: BIOS, I/O Port & K/B Connector

Size: Custom | Document Number: JE50-HR/SJV50-HR M/B Schematics | Rev: E

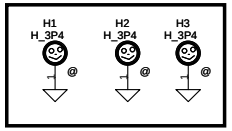
Date: Wednesday, June 08, 2011 | Sheet 41 of 61



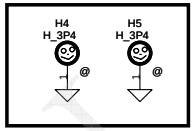
Security Classification	Compal Secret Data		
Issued Date	2011/02/08	Deciphered Date	2012/02/08

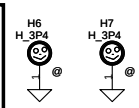
Compal Electronics, Inc.			
Title	HD Audio Codec ALC271X		
Size	Document Number		Rev
Custom	JE50-HR/SJV50-HR M/B Schematics		E
Date:	Wednesday, June 08, 2011	Sheet	42 of 61

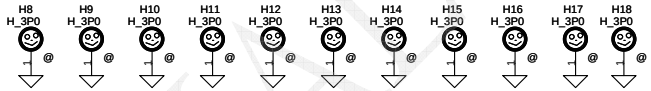
FAN Stand-Off

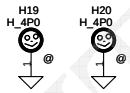


JUSB3 Stand-Off

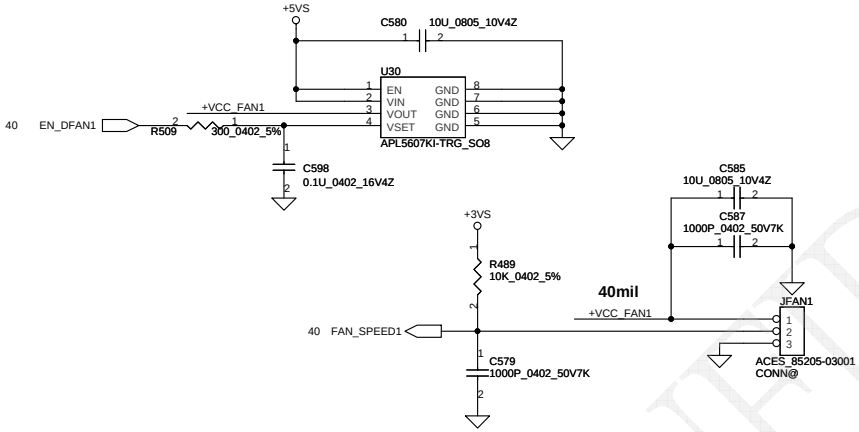


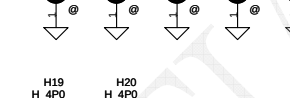


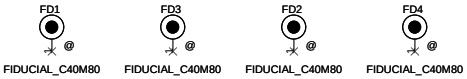




FAN1 Conn



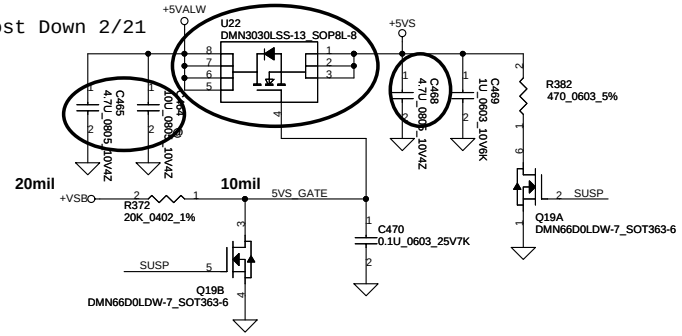




Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2011/02/08	Deciphered Date	2012/02/08	Title	FAN & Screw Hole
				Size: Custom	Document Number: JE50-HR/SJV50-HR M/B Schematics
				Date: Wednesday, June 08, 2011	Sheet 43 of 61

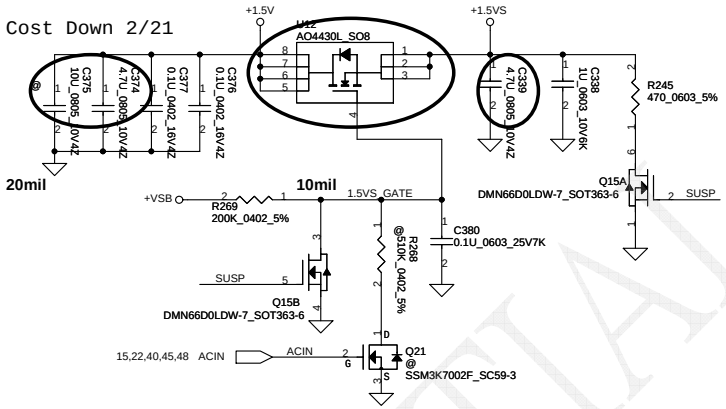
+5VALW TO +5VS

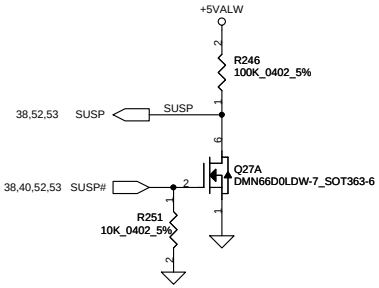
For Cost Down 2/21



+1.5V to +1.5VS

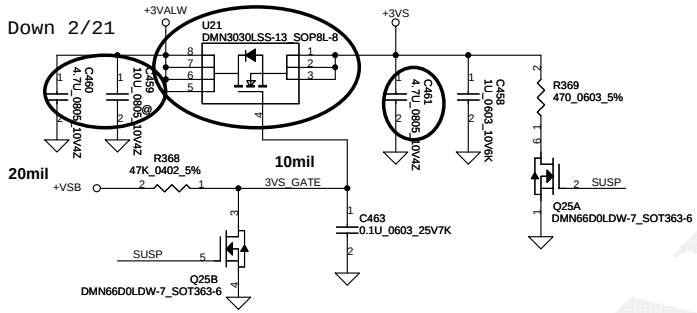
For Cost Down 2/21



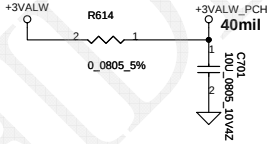


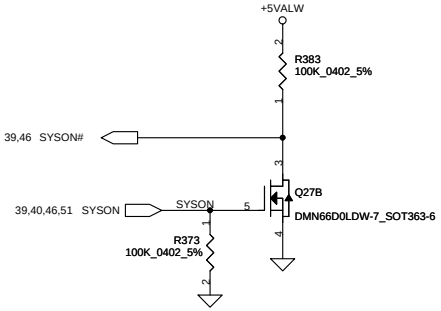
+3VALW TO +3VS

For Cost Down 2/21

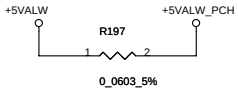


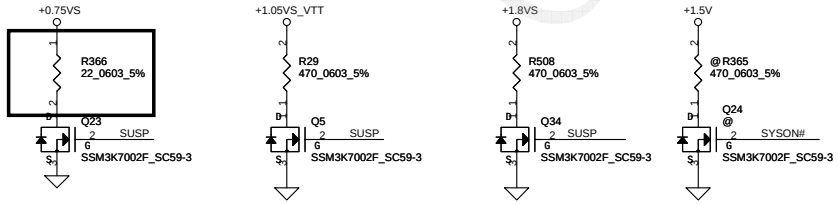
+3VALW TO +3VALW_PCH(PCH AUX Power)





+5VALW TO +5VALW_PCH(PCH AUX Power)





Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/02/08	Deciphered Date 2012/02/08	Title: DC Interface
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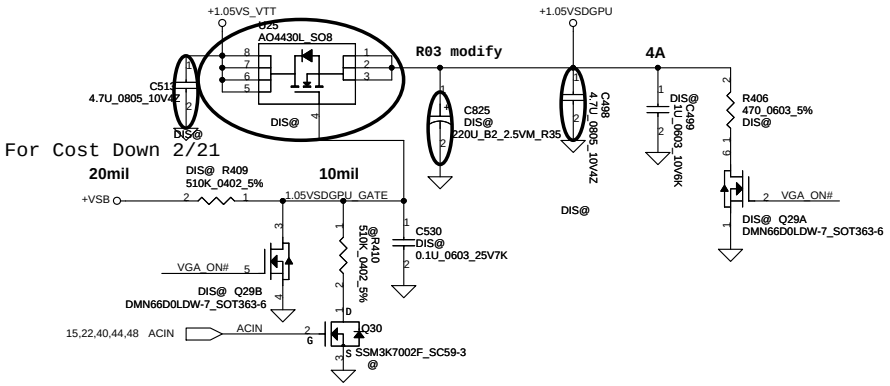
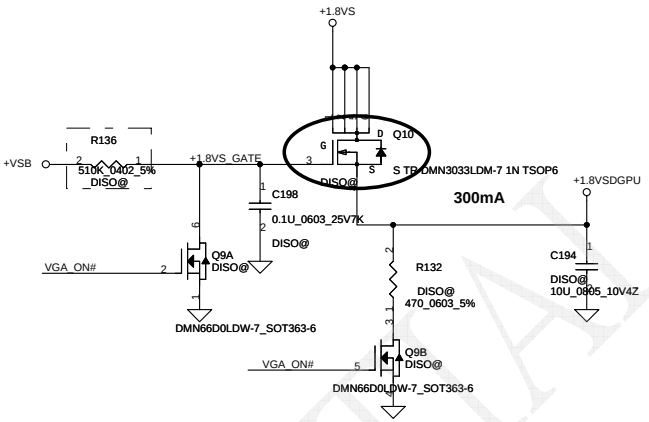
			Date: Wednesday, June 08, 2011; Sheet 44 of 61

+1.05VS_VTT to +1.05VSDGPU for GPU

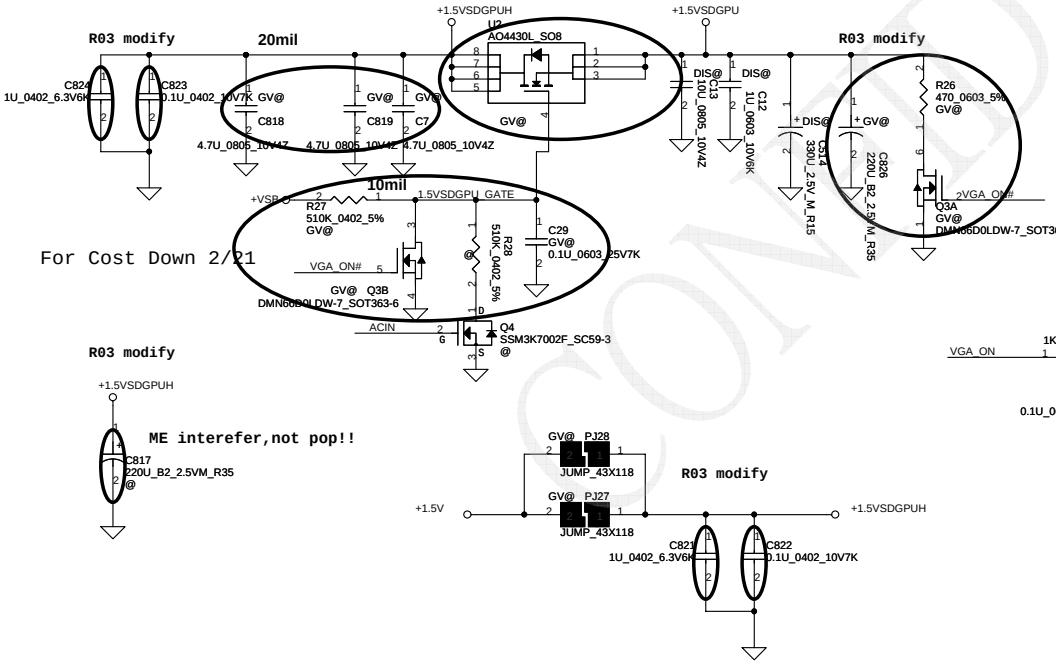


+1.8VS to +1.8VSDGPU for GPU

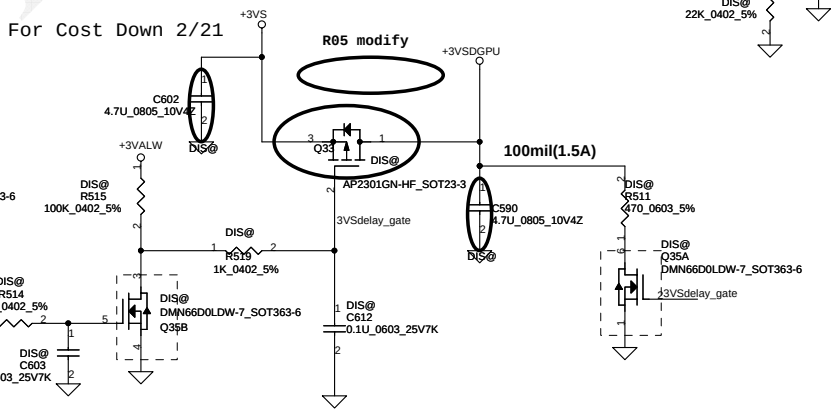


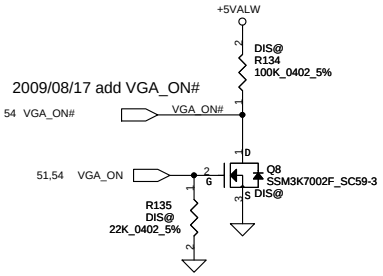
14,17 DGPU_PWR_EN — R140 0_0402_5% DIS@ — VGA_ON

+1.5VSDGPUH to +1.5VSDGPU for GPU

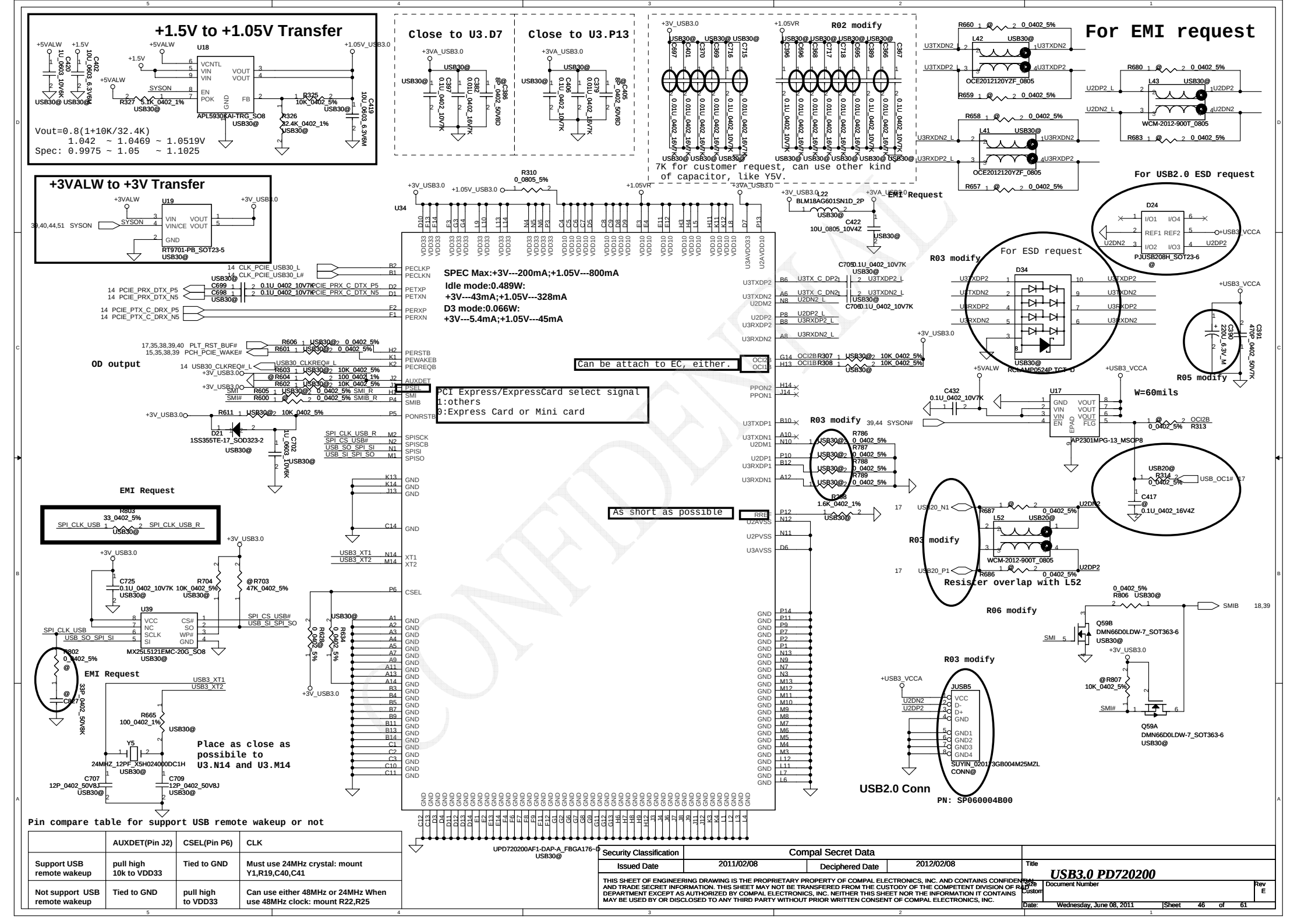


+3VS to +3VSDGPU for GPU

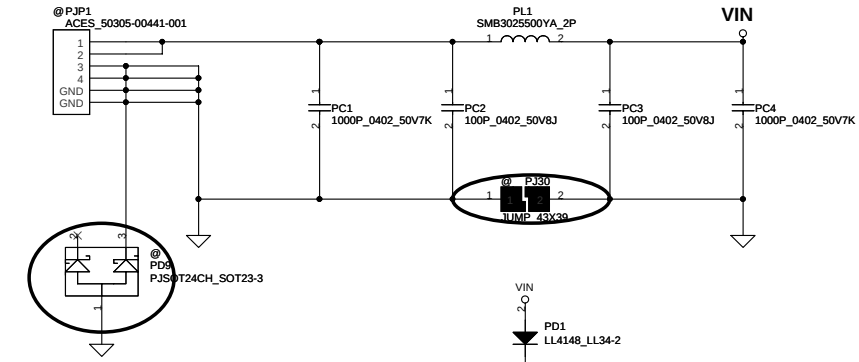


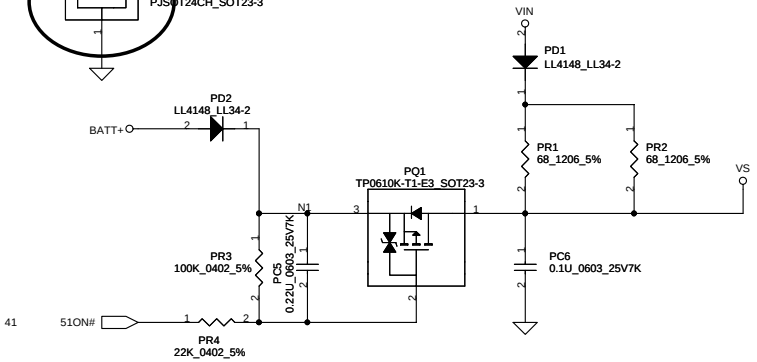


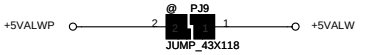
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/02/08	Deciphered Date 2012/02/08	Title: DC Interface
Size: Custom	Document Number: JE50-HR/SJV50-HR M/B Schematics		Rev: E
Date: Wednesday, June 08, 2011	Sheet 45 of 61		

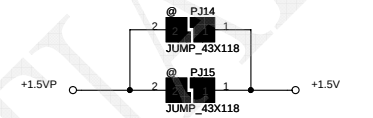


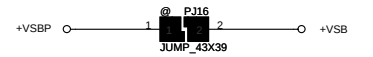
	AUXDET(Pin J2)	CSEL(Pin P6)	CLK
Support USB remote wakeup	pull high 10k to VDD33	Tied to GND	Must use 24MHz crystal: mount Y1,R19,C40,C41
Not support USB remote wakeup	Tied to GND	pull high to VDD33	Can use either 48MHz or 24MHz When use 48MHz clock: mount R22,R25

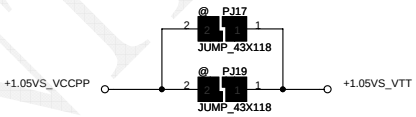


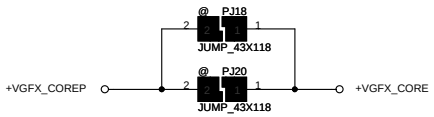


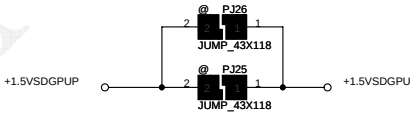


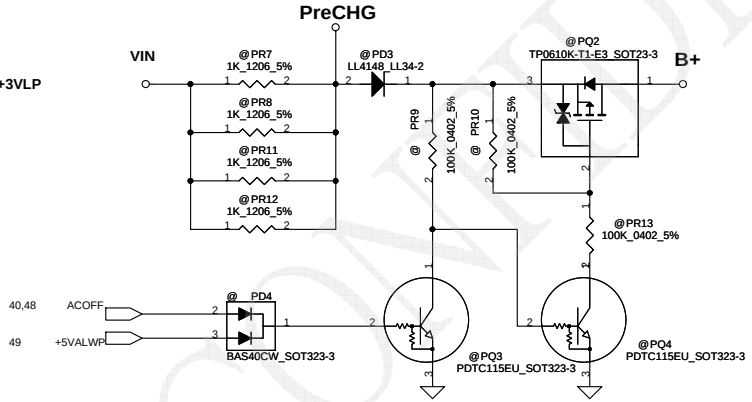












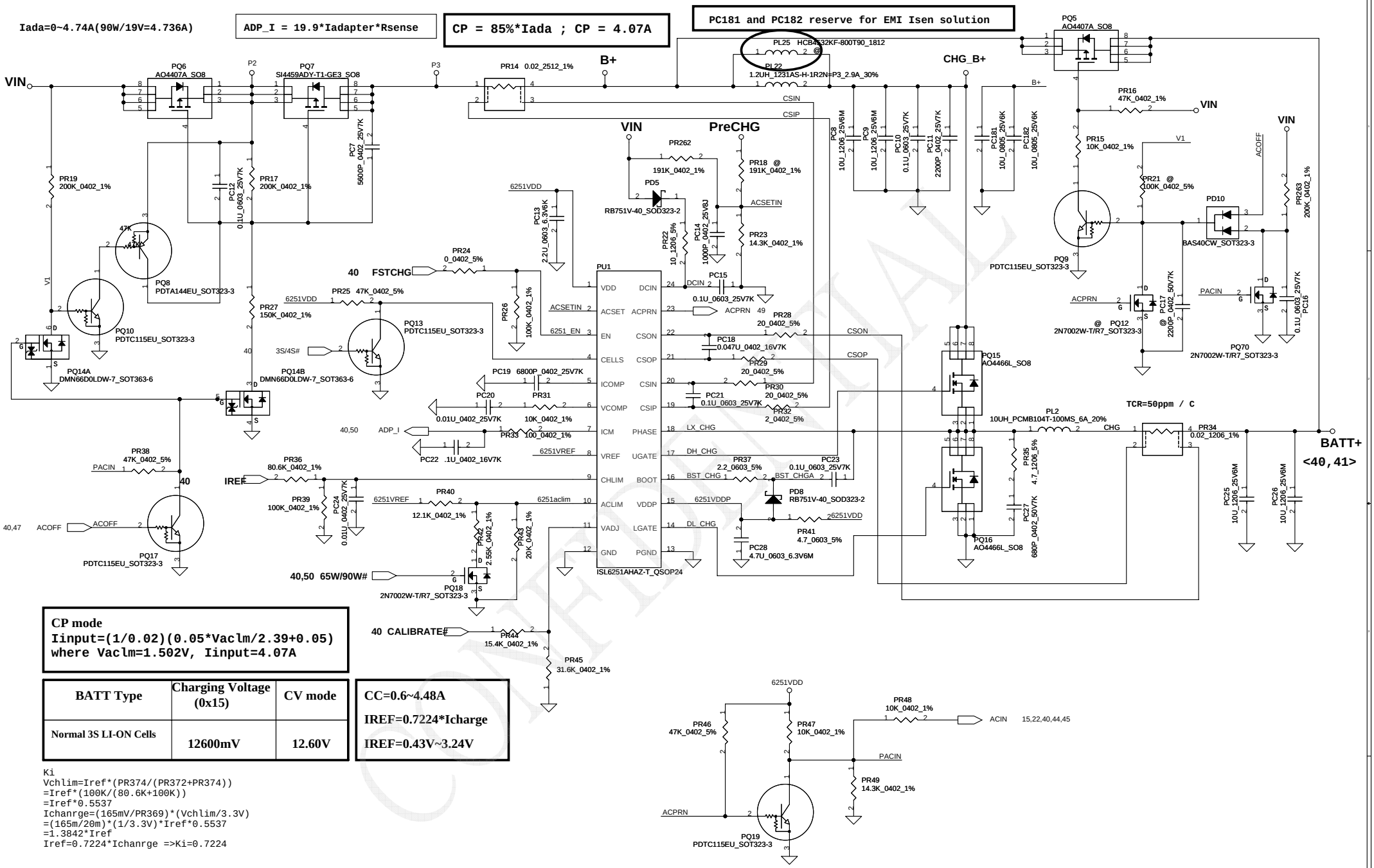
Security Classification	Compal Secret Data		
Issued Date	2011/02/08	Deciphered Date	2012/02/08

Compal Electronics, Inc.

Title: PWR DCIN / Pre-charge

Size: Custom | Document Number: JE50-HR/SJV50-HR M/B Schematics | Rev: E

Date: Wednesday, June 08, 2011 | Sheet 47 of 61



CP mode
Iinput=(1/0.02)(0.05*Vaclm/2.39+0.05)
where Vaclm=1.502V, Iinput=4.07A

BATT Type	Charging Voltage (0x15)	CV mode
Normal 3S LI-ON Cells	12600mV	12.60V

CC=0.6~4.48A
IREF=0.7224*Icharge
IREF=0.43V~3.24V

Ki
Vchlim=Iref*(PR374/(PR372+PR374))
=Iref*(100K/(80.6K+100K))
=Iref*0.5537
Ichanrge=(165mV/PR369)*(Vchlim/3.3V)
=(165m/20m)*(1/3.3V)*Iref*0.5537
=1.3842*Iref
Iref=0.7224*Ichanrge =>Ki=0.7224

Kv
Rinternal ic=514K Rec=3K R1=PR379=15.4K R2=PR381=31.6K
R=514K//31.6K//(15.4K+3k)=11.372K
r=514K//514K//31.6K=28.14K
Vcell=0.175*Vadj+3.99v
4.2V=0.175*Vadj+3.99V =>Vadj=1.2V
Vadj=Vref*(R/(R+514K))+CALIBRATE*(r/(r=514K))
1.1483=CALIBRATE*0.6046 =>CALIBRATE=1.899
1.899=(4.2-(Vcell+A*0.175))*Kv=(4.2-(4.2+A*0.175))*Kv
A=Vref*(R/(R+514K))=0.052
Kv=9.451

Security Classification	Compal Secret Data		
Issued Date	2011/02/08	Deciphered Date	2012/02/08

Compal Electronics, Inc.

Title: PWR-CHARGER

Size: Custom | Document Number: JE50-HR/SJV50-HR M/B Schematics | Rev: E

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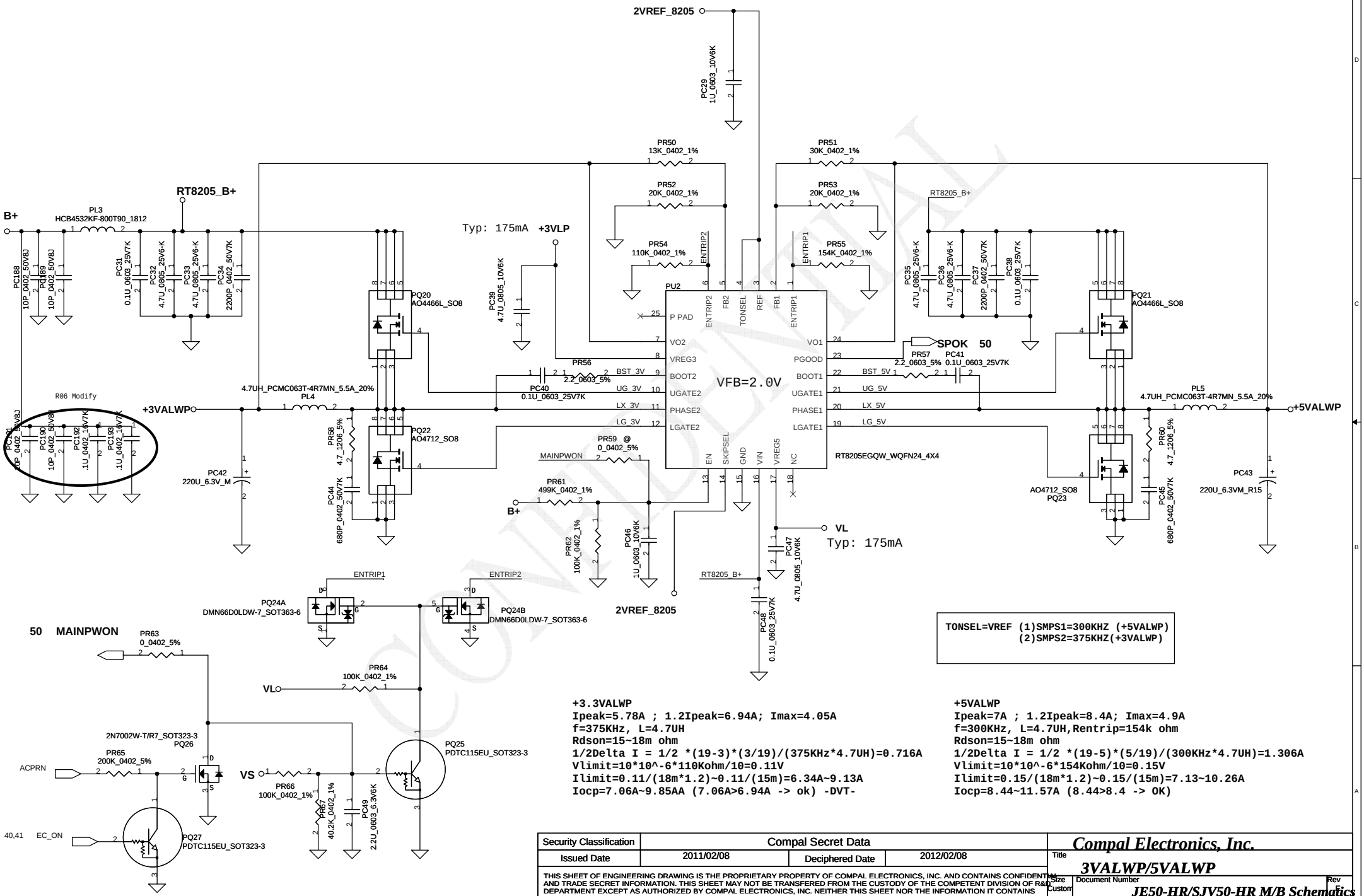

Security Classification	Compal Secret Data		
Issued Date	2011/02/08	Deciphered Date	2012/02/08

Compal Electronics, Inc.

Title: 3VALWP/5VALWP

Size: Custom | Document Number: JE50-HR/SJV50-HR M/B Schematics | Rev: F

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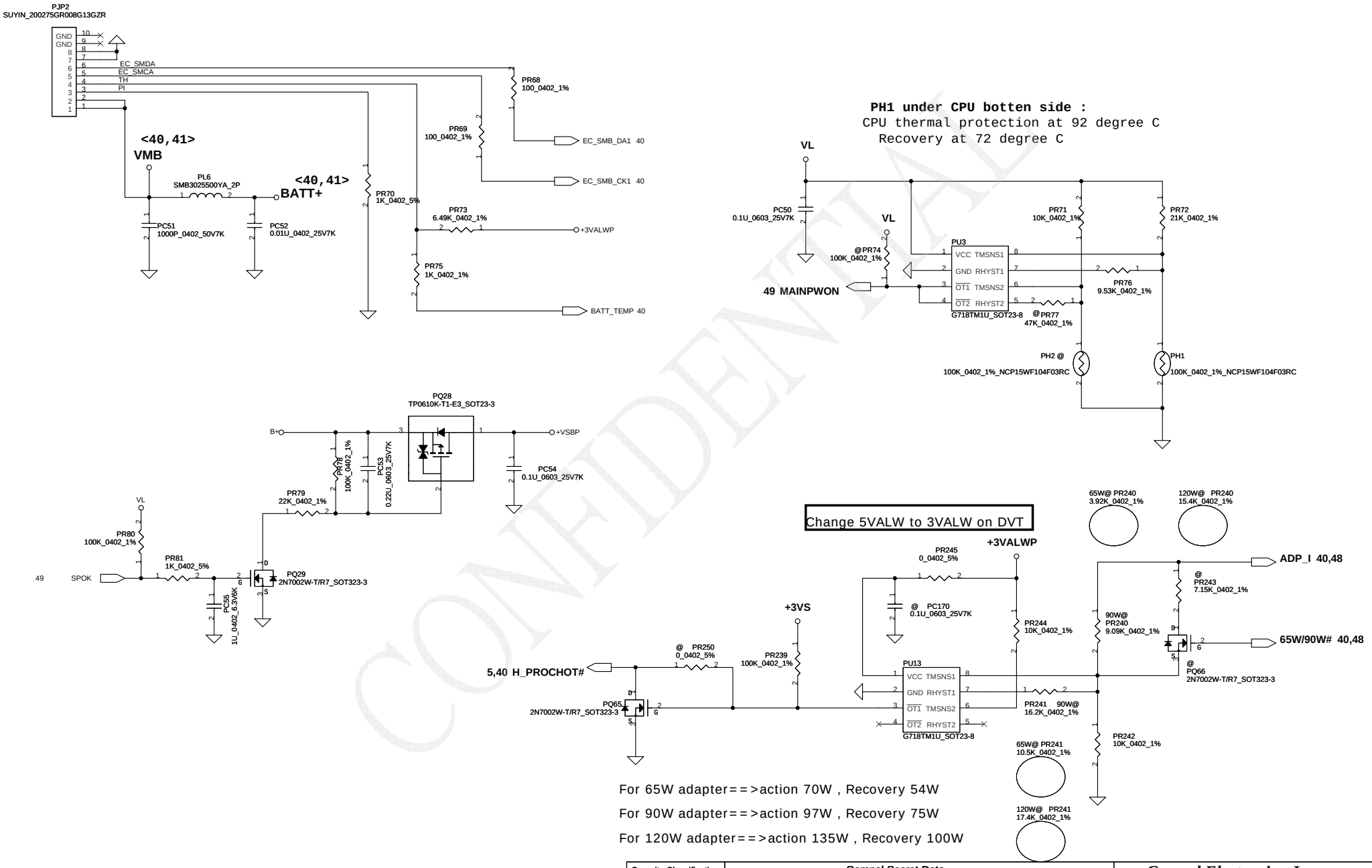
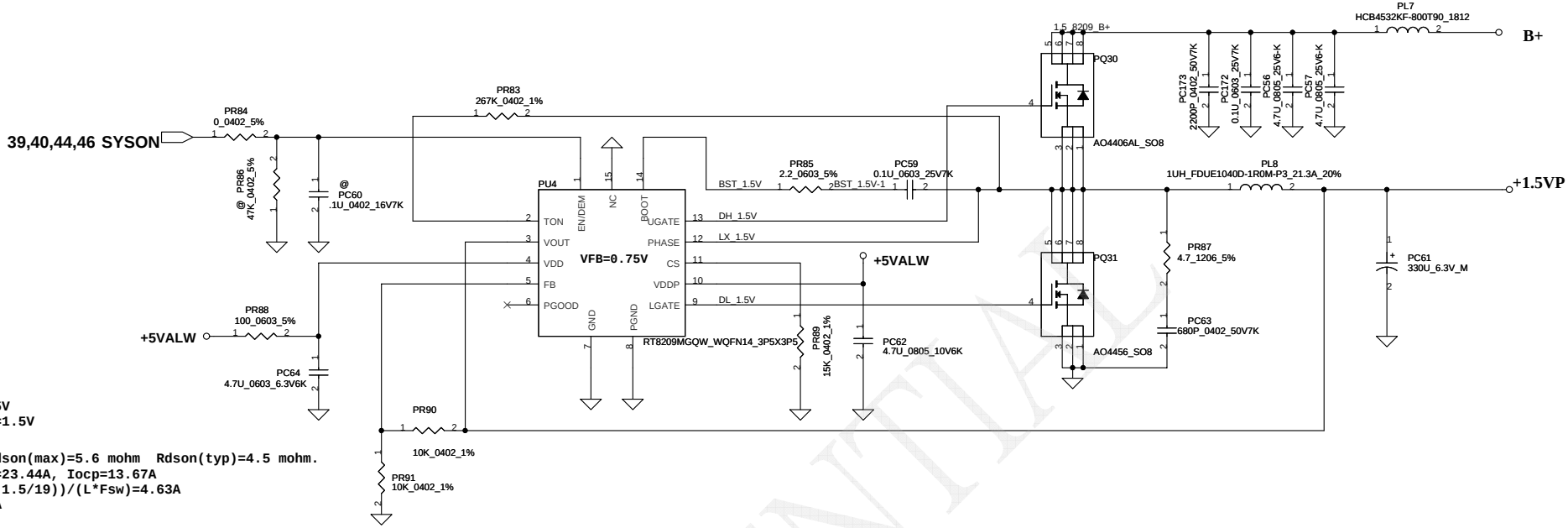


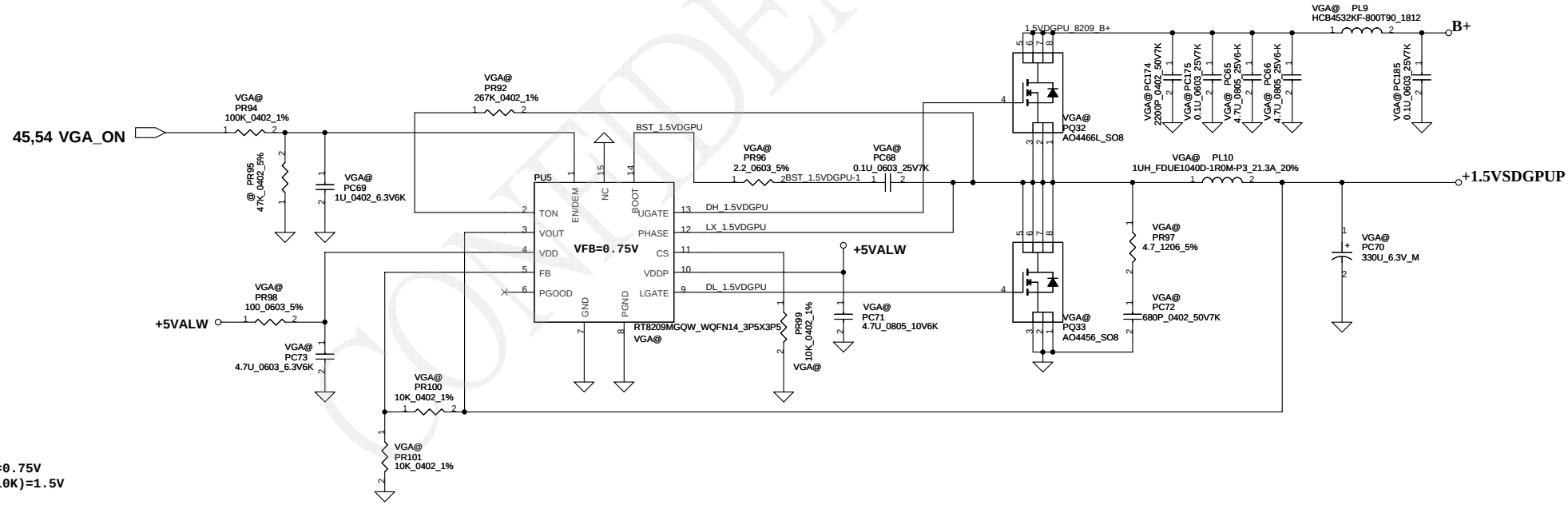
Security Classification	Compal Secret Data		
Issued Date	2011/02/08	Deciphered Date	2012/02/08

Compal Electronics, Inc.			
Title	PWR-BATTERY CONN/OTP		
Size: Custom	Document Number: JE50-HR/SJV50-HR M/B Schematics		Rev: E
Date: Wednesday, June 08, 2011	Sheet 50 of 61		



<Vo=1.5V> VFB=0.75V
V=0.75*(1+10K/10K)=1.5V
Fsw=298KHz

Cout ESR=15m ohm Rdson(max)=5.6 mohm Rdson(typ)=4.5 mohm.
Ipeak=19.53A, Imax=23.44A, Iocp=13.67A
Delta I=((19-1.5)*(1.5/19))/(L*Fsw)=4.63A
=>1/2Delta I=2.315A
choose Rcs=15K
Iocpmax=((15K*11uA)/0.0045)+2.315A=35.65A
Iocpmin=((15K*9uA)/(0.0056*1.3))+2.315A=23.06A
Iocp=23.06A~35.65A

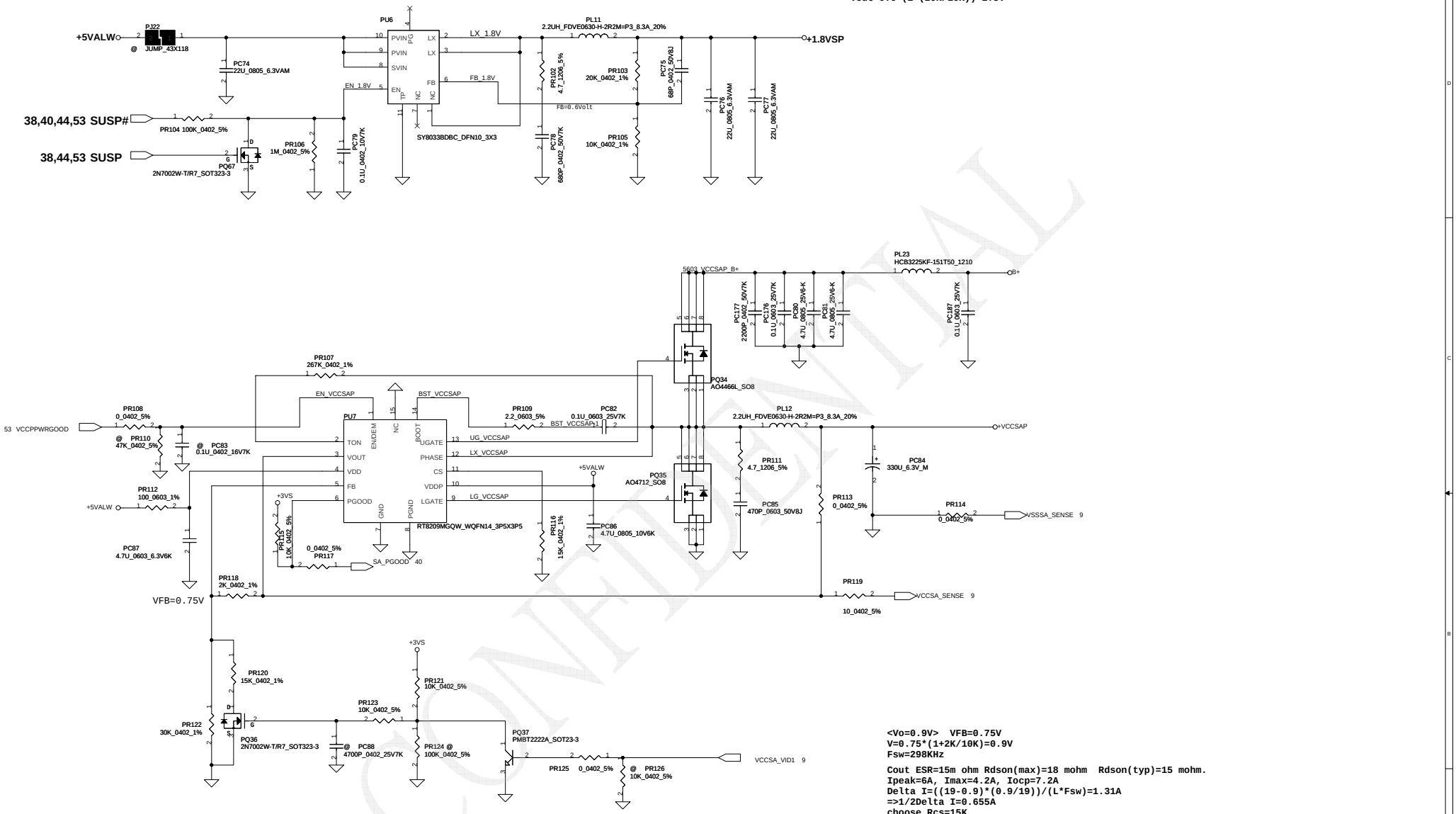


<Vo=1.5V> VFB=0.75V
V=0.75*(1+10K/10K)=1.5V
Fsw=298KHz

Cout ESR=15m ohm Rdson(max)=5.6 mohm Rdson(typ)=4.5 mohm.
Ipeak=10.4A, Imax=12.48A, Iocp=7.28A
Delta I=((19-1.5)*(1.5/19))/(L*Fsw)=4.63A
=>1/2Delta I=2.315A
choose Rcs=10K
Iocpmax=((10K*11uA)/0.0045)+2.315A=24.59A
Iocpmin=((10K*9uA)/(0.0056*1.3))+2.315A=15.95A
Iocp=15.95A~24.59A

Security Classification	Compal Secret Data		
Issued Date	2011/02/08	Deciphered Date	2012/02/08

Compal Electronics, Inc.			
Title: PWR-+1.5VP/+1.5VSDGPU			
Size: Custom	Document Number: JE50-HR/SJV50-HR M/B Schematics		Rev: E
Date: Wednesday, June 08, 2011	Sheet 51 of 61		



VID[0]	VID[1]	VCCSA Vout	Require on 2011/ 2012 Required
0	0	0.9 V	Yes/Yes
0	1	0.8 V	Yes/Yes
1	1	0.75V	No/Yes
1	1	0.65V	No/Yes

Note:Use VCCSA_SEL to switch High & Low Level for VID[1]
(ie. VCCSA_SEL) due to the VID[0] is don't care for this setting.

<Vo=0.9V> VFB=0.75V
V=0.75*(1+2K/10K)=0.9V
Fsw=298KHz

Cout ESR=15m ohm Rdson(max)=18 mohm Rdson(typ)=15 mohm.
Ipeak=6A, Imax=4.2A, Iocp=7.2A
Delta I=((19-0.9)*(0.9/19))/(L*Fsw)=1.31A
=>1/2Delta I=0.655A
choose Rcs=15K
Iocpmax=((15K*11uA)/0.015)+0.655A=11.48A
Iocpmin=((15K*9uA)/(0.018*1.2))+0.655A=7.27A
Iocp=7.27A~11.48A

Security Classification	Compal Secret Data		
Issued Date	2011/02/08	Deciphered Date	2012/02/08

Compal Electronics, Inc.

Title: PWR +VCCSAP

Size: C | Document Number: JE50-HR/SJV50-HR M/B Schematics | Rev: E

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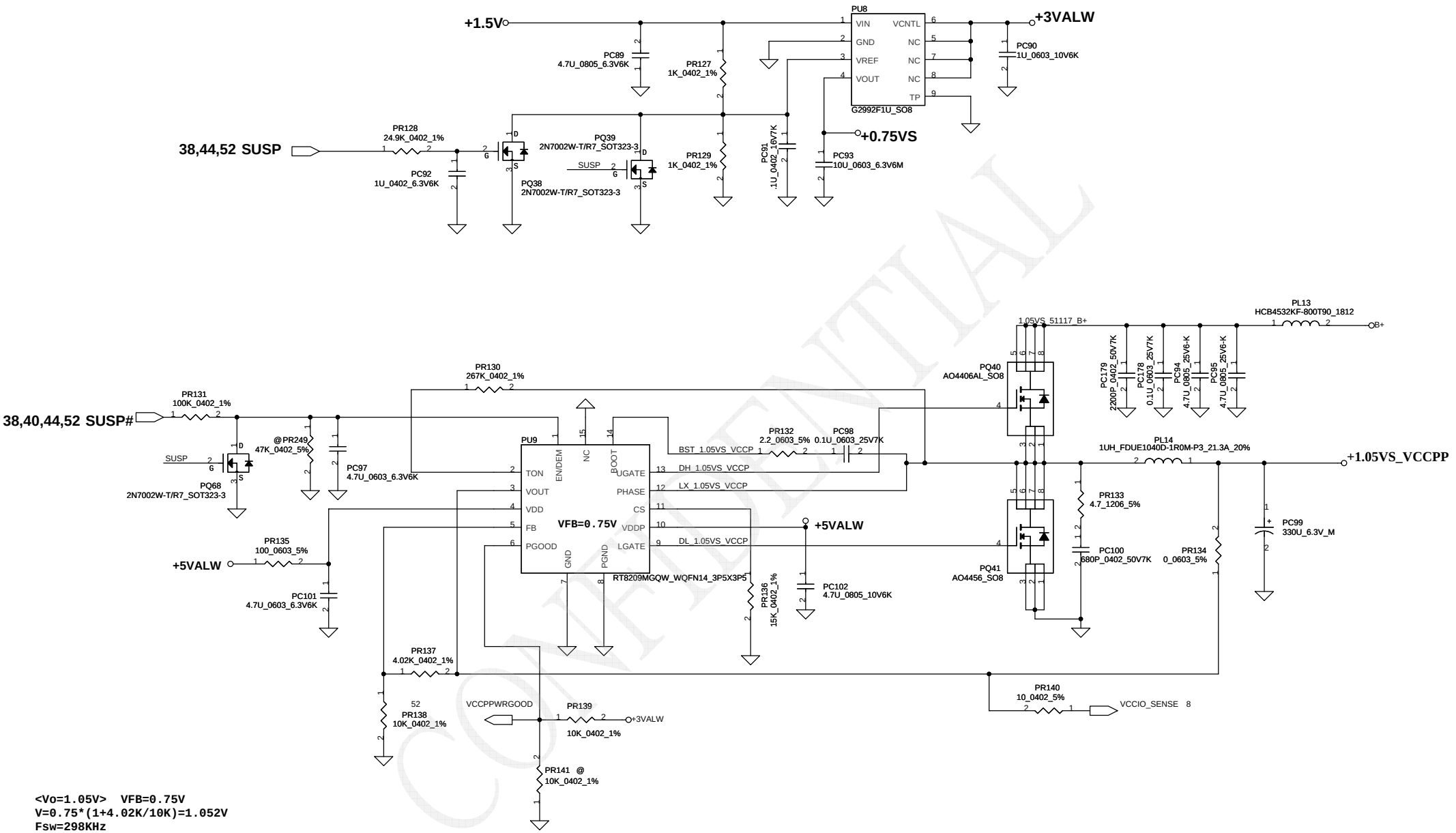


<Vo=1.05V> VFB=0.75V
V=0.75*(1+4.02K/10K)=1.052V
Fsw=298KHz

Cout ESR=15m ohm Rdson(max)=5.6 mohm Rdson(typ)=4.5 mohm.
Ipeak=12.866A, Imax=9A, Iocp=15.439A
Delta I=((19-1.05)*(1.05/19))/(L*Fsw)=3.33A
=>1/2Delta I=1.665A
choose Rcs=15K
Iocpmax=((15K*11uA)/0.0045)+1.665A=37.62A
Iocpmin=((15K*9uA)/(0.0056*1.3))+1.665A=23.02A
Iocp=23.02A~37.62A

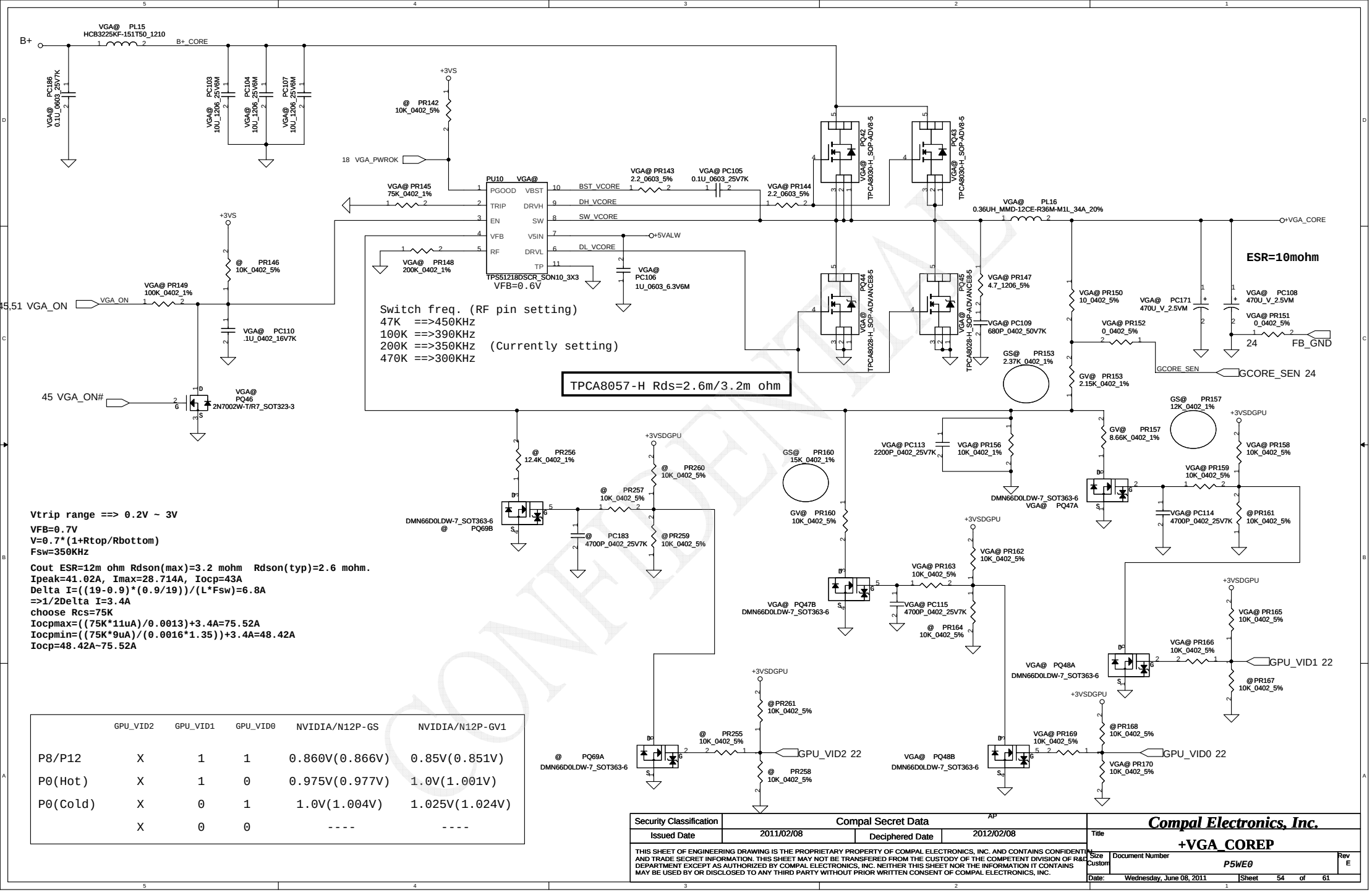
Security Classification	Compal Secret Data		
Issued Date	2011/02/08	Deciphered Date	2012/02/08

Compal Electronics, Inc.

Title: PWR +1.05VS_VCCPP/+0.75VSP

Size: Custom | Document Number: JE50-HR/SJV50-HR M/B Schematics | Rev: 1E

Date: Wednesday, June 08, 2011 | Sheet 53 of 61



Vtrip range ==> 0.2V ~ 3V

VFB=0.7V
V=0.7*(1+Rtop/Rbottom)
Fsw=350KHz

Cout ESR=12m ohm Rdson(max)=3.2 mohm Rdson(typ)=2.6 mohm.
Ipeak=41.02A, Imax=28.714A, Iocp=43A
Delta I=((19-0.9)*(0.9/19))/(L*Fsw)=6.8A
=>1/2Delta I=3.4A
choose Rcs=75K
Iocpmax=((75K*11uA)/0.0013)+3.4A=75.52A
Iocpmin=((75K*9uA)/(0.0016*1.35))+3.4A=48.42A
Iocp=48.42A~75.52A

	GPU_VID2	GPU_VID1	GPU_VID0	NVIDIA/N12P-GS	NVIDIA/N12P-GV1
P8/P12	X	1	1	0.860V(0.866V)	0.85V(0.851V)
P0(Hot)	X	1	0	0.975V(0.977V)	1.0V(1.001V)
P0(Cold)	X	0	1	1.0V(1.004V)	1.025V(1.024V)
	X	0	0	----	----

Security Classification	Compal Secret Data		
Issued Date	2011/02/08	Deciphered Date	2012/02/08

Compal Electronics, Inc.			
Title	+VGA_COREP		
Size: Custom	Document Number: P5WE0		Rev: E
Date: Wednesday, June 08, 2011	Sheet 54 of 61		

Alert# PU resister need close CPU,
so the PU resister in HW schematic.
but DAT and CLK need close PWM-IC,
so the PU resister in POWER schematic.

Parallel and tune length

change from 43P to 47P
for shortage problem
2010-03-15

*Iccmax in Turbo Mode for SV (35W) is 53A

+CPU_CORE

Icc-max=53A
Rdson=3.6~4.5m ohm
DCR=1.1m ohm
HW output cap:
(1)10U_0805_4V *10
(2)22U_0805_6.3V *15
(3)470U_D2_2V *4(ESR=4.5m ohm)

*OCP setting value=71.5A

+VGFX_COREP

Ipeak=26A , Imax=18.2A , 1.2Ipeak=31.2A
Rdson=3.6~4.5m ohm
DCR=1.1m ohm
HW output cap:
(1)22U_0805_6.3V *12
(2)470U_D2_2V *2(ESR=4.5m ohm)

*OCP setting value=37A

Security Classification	Compal Secret Data		
Issued Date	2011/02/08	Deciphered Date	2012/02/08

Compal Electronics, Inc.

Title: PWR +CPU_CORE/+VGFX_CORE

Size: Custom | Document Number: JE50-HR/SJV50-HR M/B Schematics | Rev: 1.0

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Version change list (P.I.R. List)

for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Add snubber R=4.7 ohm and C 680 pF	EMI solution	0.2	---	Add SD001470B80 for PR35,PR58,PR60,PR87,PR111, PR133,PR202,PR216,PR234 Add SE074681K80 for PC27,PC44,PC45,PC63,PC85, PC100,PC140,PC154,PC169	2010/10/20	DVT_P5WE0
2	Change boost R from 0 to 2.2 ohm	EMI solution	0.2	---	Change R to SD013220B80 forPR37,PR56,PR57,PR85, PR109,PR132,PR186,PR214,PR233	2010/10/20	DVT_P5WE0
3	Change PL11 and PL12 from SH00000F800 to SH00000M700	Cost saving	0.2	52	Change PL11 and PL12 from SH00000F800 to SH00000M700	2010/10/20	DVT_P5WE0
4	Change PL18,PL19,PL20,PL21 from SH000005680 to SH00000HK00	Change DCR tolerance to 5%	0.2	55	Change PL18,PL19,PL20,PL21 from SH000005680 to SH00000HK00	2010/10/20	DVT_P5WE0
5	CPU CORE transient compensation	CPU CORE transient compensation	0.2	55	Add PR248, PC160, PC180	2010/10/20	DVT_P5WE0
6	Fixed adapter plug in will cause could not transitiion to AC mode when system was on battery mode	disable pre-charge circuit and don't use 連動線路	0.5	---	Del PR7, PR8, PR9, PR10, PR11, PR12, PR13, PD3, PD4, PQ2, PQ3, PQ4, PR18, PR21, PQ12, PC17	2010/11/20	PVT_P5WE0
7	Fixed adapter plug in will cause could not transitiion to AC mode when system was on battery mode	disable pre-charge circuit and don't use 連動線路	0.5	---	Add PR262, PD10, PQ70, PR263, PC16 Change PQ7 to AO4459	2010/11/20	PVT_P5WE0
8	Add 0.1UF on B+ input power	EMI solution	0.5	---	Add PC184, PC185, PC186, PC187	2010/11/20	PVT_P5WE0
9	Adjust VGA CORE power sequesce	for NV request	0.5	---	Change PR149 to 100K	2010/11/20	PVT_P5WE0
10	Adjust 1.5VSDGPU power sequesce	for NV request	0.5	---	Change PR94 to 510K and add PC69	2010/11/20	PVT_P5WE0
11	Adjust VID table	for NV request	0.5	---	Change PR153, PR157, PR160	2010/11/20	PVT_P5WE0
12							
13							
14							
15							

Security Classification	Compal Secret Data		
Issued Date	2011/02/08	Deciphered Date	2012/02/08

Compal Electronics, Inc.

Title: PIR (PWR)

Size: Custom | Document Number: JE50-HR/SJV50-HR M/B Schematics | Rev: 5

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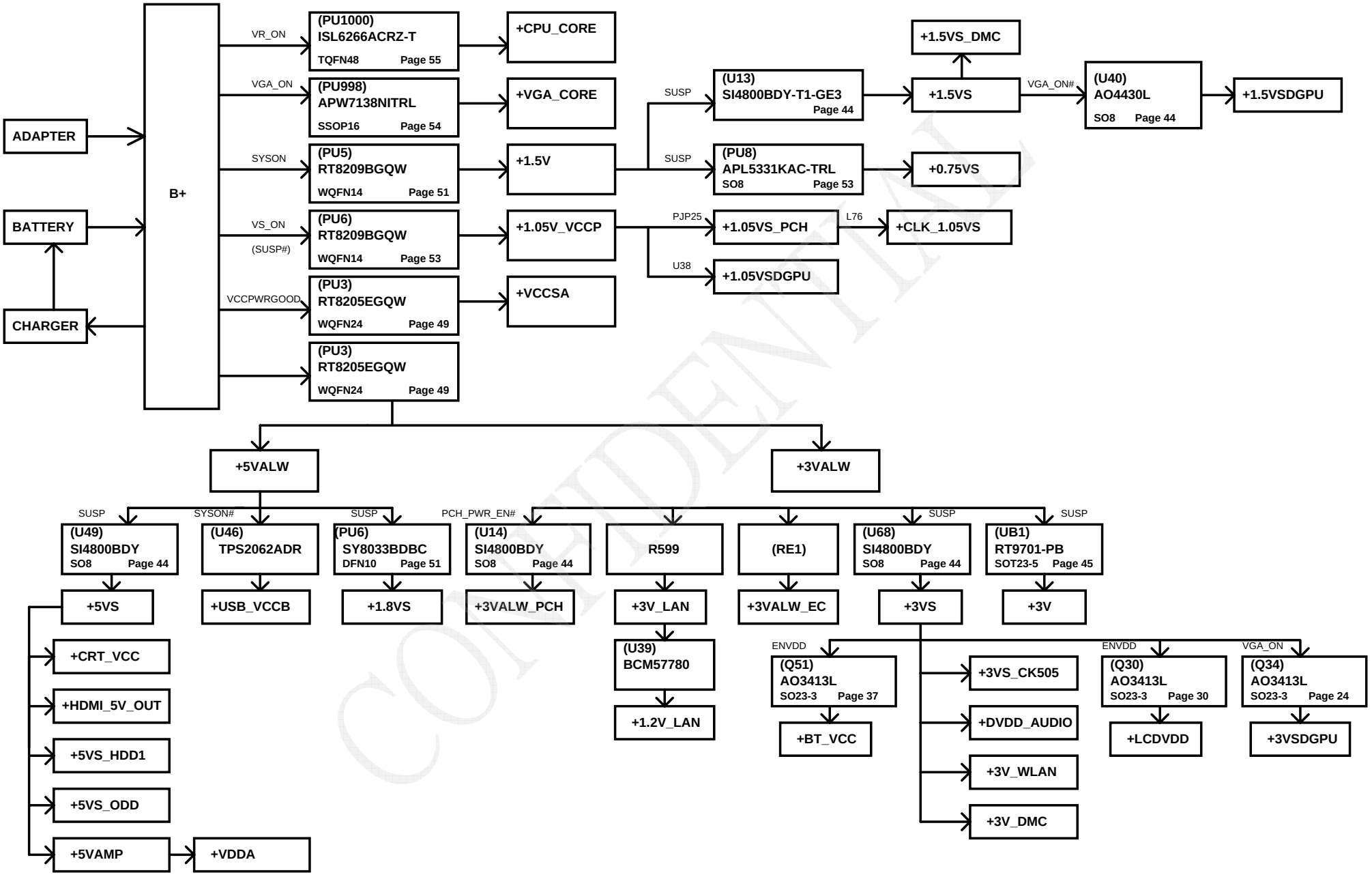
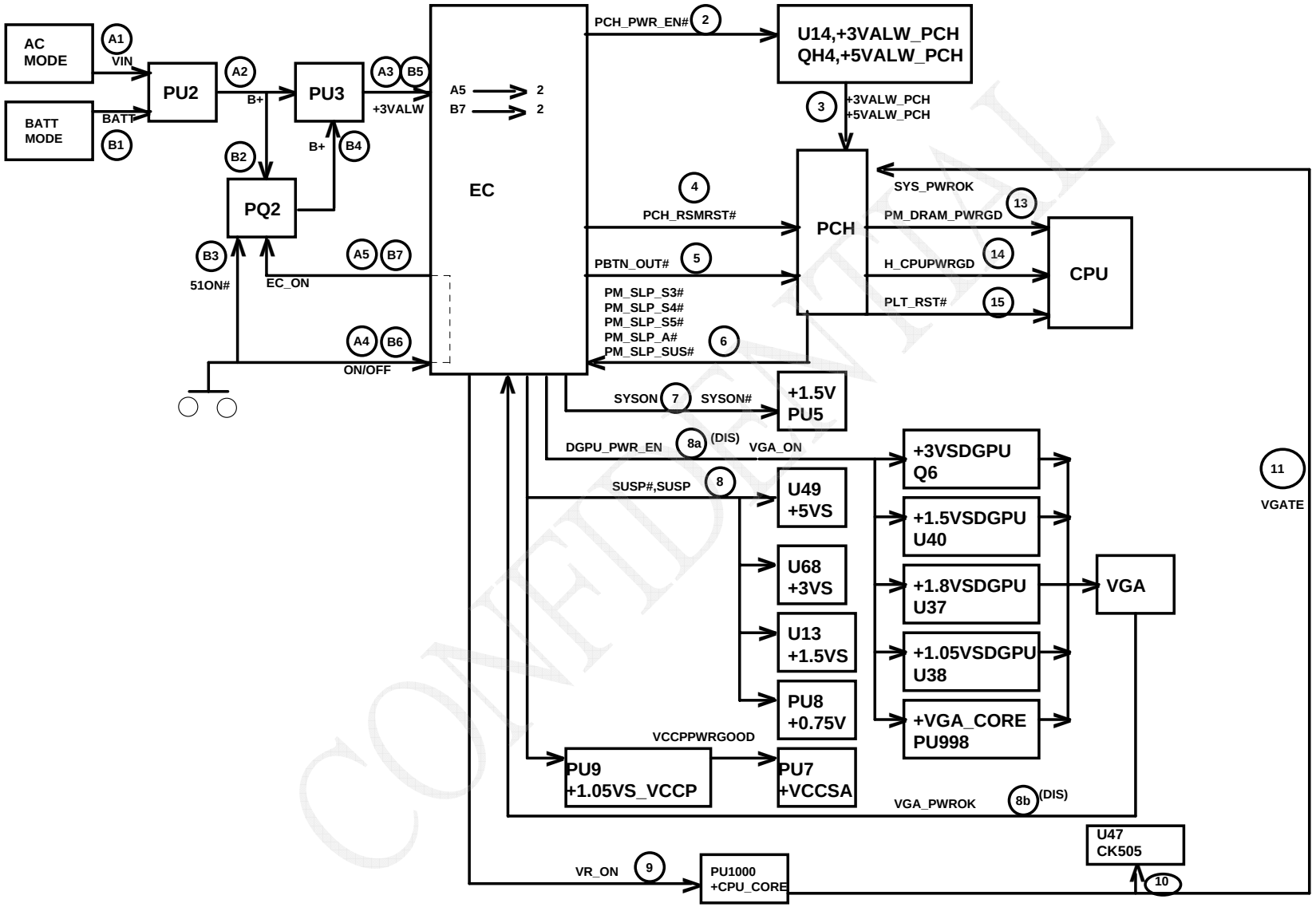


Security Classification	Compal Secret Data		
Issued Date	2011/02/08	Deciphered Date	2012/02/08

Compal Electronics, Inc.			
Title: Power Rail			
Size: Custom	Document Number: JE50-HR/SJV50-HR M/B Schematics		Rev: A
Date: Wednesday, June 08, 2011	Sheet 57 of 61		



Security Classification	Compal Secret Data		
Issued Date	2011/02/08	Deciphered Date	2012/02/08

Compal Electronics, Inc.

Title: Power sequence

Size: Custom | Document Number: JE50-HR/SJV50-HR M/B Schematics | Rev: E

Date: Wednesday, June 08, 2011 | Sheet 58 of 61

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	P.18	PCH_GPIO71	09/01	SW	For identofy VRAM 900 or 800 MHz		0.2
2	P.31	DPST buffer	09/03	HW	Change U1 from NOT gate to Buffer		0.2
3	P.39	EC_MUTE# pull high	09/03	HW	Change EC_MUTE# Pull high from +3VALW to +3VS		0.2
4	P.40	TP Conn. Reverse	09/03	HW	TP Mudule change,so reverse TP pin		0.2
5	P.13	R624 pop @	09/03	HW	Already pull high R655~		0.2
6	P.45	Change Cap from 0.1u to 0.01u	09/03	HW	C696,C368,C717,C718,C695,C366,C697, C401,C370,C369,C715 change to 0.01U Follow Vendor Suggest ..		0.2
7	P.35	Change 0 Ohm to 47 Ohm	09/04	Broadcom	R199,R207,R211,R215,R168,R171,R179, R182,R195,R216,R192 change to 47 Ohm Follow Vendor Suggest ..		0.2
8	P.5		09/17	HW	CPU XDP socket take off		0.2
9	P.40		09/17	HW	TP pin reverse		0.2
10	P.13		09/17	HW	R624 change to 4.7K		0.2
11	P.45		09/17	HW	OCI2B(R313) place @ for BOM		0.2
12	P.33		09/17	HW	HDMI output from PCH (by UMA)		0.2
13	P.35		09/17	HW	switch the LAN MIDI0 and MIDI2 pin		0.2
14	P.17,35 ,37,38, 39,45		09/17	HW	Change IO port PLT_RST# to PLT_RST_BUF#		0.2
15	P.18		09/17	HW	OPTIMUS_EN# pull high, pull low resistor value both change to 10K		0.2
16	P.24		09/20	HW	modify the VRAM strap pin ROM_SI pull low resistor for implement VRAM 900MHz		0.3
17	P.33		09/23	HW	Add R784 and R785 for DDC pull high...		0.3
18	P.44		09/23	HW	Add C818 and C819 for coupling noise from other spare trace...		0.3
19	P.45		09/23	HW	Add R786,R787,R788 and R789 pull down from vendor's suggestion..		0.3
20	P.37		09/23	HW	Add C820,R790 and Q58 for 3G/B and change source voltage from +3VS to +3VALW..		0.3
21	P.45		09/23	HW	Add C821,C822,C823,C824 for +1.5V... and move the PJ26 & PJ27 between 1.5V to 1.5VSDGPUH		0.3
22	P.46		09/24	HW	Change JUSB5 to USB2.0 Conn. Add D34 as ESD Diode for USB3.0		0.3

Security Classification	Compal Secret Data		
Issued Date	2011/02/08	Deciphered Date	2012/02/08

Compal Electronics, Inc.

Title: EE P.I.R (1)

Size: Custom | Document Number: JE50-HR/SJV50-HR M/B Schematics | Rev: E

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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
23	P.41		09/24	HW	Add R791 pull down 22k Ohm to ground Vendor's request...		0.3
24	P.22		09/24	HW	Add D31 to connect to ACIN Vendor's request...		0.3
25	P.36		09/29	HW	Add JP1,JP2 and JP3 for 家電下鄉 ESD protection		0.3
26	P.36		09/29	ME	Update the JREAD1 symbol		0.3
27	P.13		09/29	HW	Add R792 follow DG1.5		0.3
28	P.33		09/29	HW	Change HDMI termination R to 680 Ohm		0.3
29	P.44		09/29	HW	Add C825 fro +1.05VSDGPU		0.3
30	P.17,38 ,45		09/30	HW	Change the M/B to USB port to port 1 Sub/B to port 0 and port 2		0.3
31	P.5		10/04	HW	Add test point for TCK,TMS, TRST#,TDO,TDI		0.3
32	P.17,18		10/04	HW	WWAN_OFF# from GPIO51 to GPIO37 WL_OFF# from GPIO55 to GPIO49		0.3
33	P.17,45		10/04	HW	M/B USB port from port 2 change to port1		0.3
34	P.26		10/04	HW	C1 and C604 chaneg to 470uF		0.3
35	P.36		10/04	HW	Add C827 as DGND and RJ45_GND bridge		0.3
36	P.36		10/04	HW	Change R490,R491,R492 and R493 to 0603 package		0.3
37	P.35		10/04	HW	Chaneg R214 to 0603 package		0.3
38	P.35		10/04	HW	Chaneg R192,R195,R199,R207,R211 ,R215,R168,R171,R179,R182 to 0 Ohm		0.3
39	P.40		10/04	HW	follow broadcom suggestion,add R496		0.3
40	P.40		10/04	HW	Add keyboard cap for EMI		0.3
41	P.44		10/04	HW	Add C826 for +1.5VSDGPU		0.3
42	P.37		10/05	HW	Add RTS5138 circuit		0.4
43	P.13		10/12	HW	Add D35 ,R799 and C838 for changing the RTC to samll size... and can be charged!!		0.4
44	P.14		10/12	HW	Add CLK_SD_48M for Card Reader 5138		0.4
45	P.24		10/12	HW	Pop R129 follow NV suggestion		0.4
46	P.25		10/12	HW	Pop R82 and De-pop R92 follow NV suggestion		0.4
47	P.25		10/12	HW	Add R800 and R801 10K Ohm pull down follow NV suggestion		0.4
48	P.24		10/12	HW	Change R775,R777,R778 and R779 to GV@		0.4

Security Classification	Compal Secret Data		
Issued Date	2011/02/08	Deciphered Date	2012/02/08

Compal Electronics, Inc.

Title: EE P.I.R (2)

Size: Custom | Document Number: JE50-HR/SJV50-HR M/B Schematics | Rev: E

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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
49	9		11/12	HW	+1,8VS add C830,C831 10U_0603 +VCCSA add C828,C829 10U_0603		
50	20		11/12	HW	+1.05VS_PCH add R808 0_0603		
51	36		11/15	HW	LANGND add C808 0.1n_0402		
52	19		11/15	HW	+VCCADAC add C832 10p_0402		
53	40		11/15	HW	EC Board ID change to 56K add EC debug port		
54	32		11/25	HW	EMI cost down request D17,D18 @		
55	36		11/25	HW	EMI cost down request D36 @		
56	13 & 34		0208	HW	Change Odd sata port from port 2 to port 1 cause by intel sata II port issue		Rev 2.0

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