

MODEL NAME : VAW11
 PROJECT CODE : ANRVAW1100
 PCB NO : LA-9102P (Mars Pro)

DA60000UU00 LA-9102P M/B
 DA40001G400 LS-9105P POWER BUTTON/B
 DA40001FP00 LS-9102P USB/B
 DA40001FQ00 LS-9103P TP BUTTON/B
 DA40001FR00 LS-9104P ODD/B

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Schematic Document

Intel Chief River Ivy Bridge (BGA) + Panther Point OAK 17" UMA/DIS AMD Mars Pro

2012-09-25
 Rev: 1.0

46@ : for 46 level

@ : Nopop Component

CONN@ : Connector Component

KB9012@ : ENE KB9012 Implemented

UMA@ : Only for UMA

EMC@ : EMI/ESD parts

GCLK@ : Green CLK implemented

GCLKUMA@ : Green CLK for UMA

GCLKDIS@ : Green CLK for DIS

XTAL@ : X'tal implemented

XTALDIS@ : X'tal with DIS implemented

R1@ : R1 P/N

R3@ : R3 P/N

i3R1@ : CPU i3-3217 1.8G

i3VOSR1@ : CPU i3-2365 1.4G

i5R1@ : CPU i5-3317 1.7G

i7R1@ : CPU i7-3517 1.9G

CEL1@ : CPU Celeron 887 1.5G

PENR1@ : CPU Pentium 997 1.6G

DIS@ : Only for Discrete

TH@/THR1@ : Thames-XT

MS@/MSR1@ : Mars Pro

X76@ :

SPI-ROM & VRAM Group

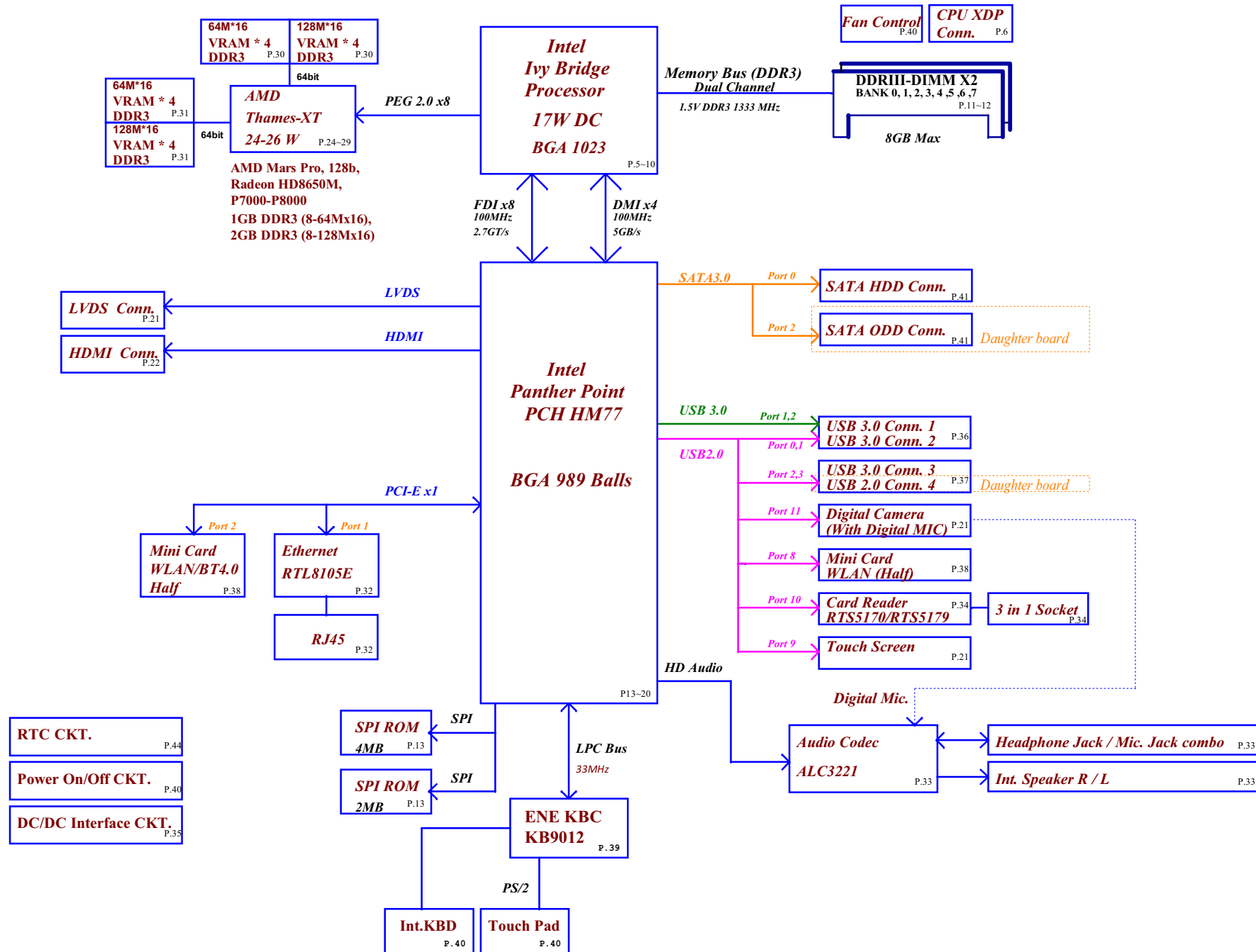


PCB 0T3 LA-9102P REV0 M/B
 DA60000UU00



PCB-MB
 DA80000R911

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				Custom	1.0
				Date:	Tuesday, September 25, 2012
				Sheet	1 of 57

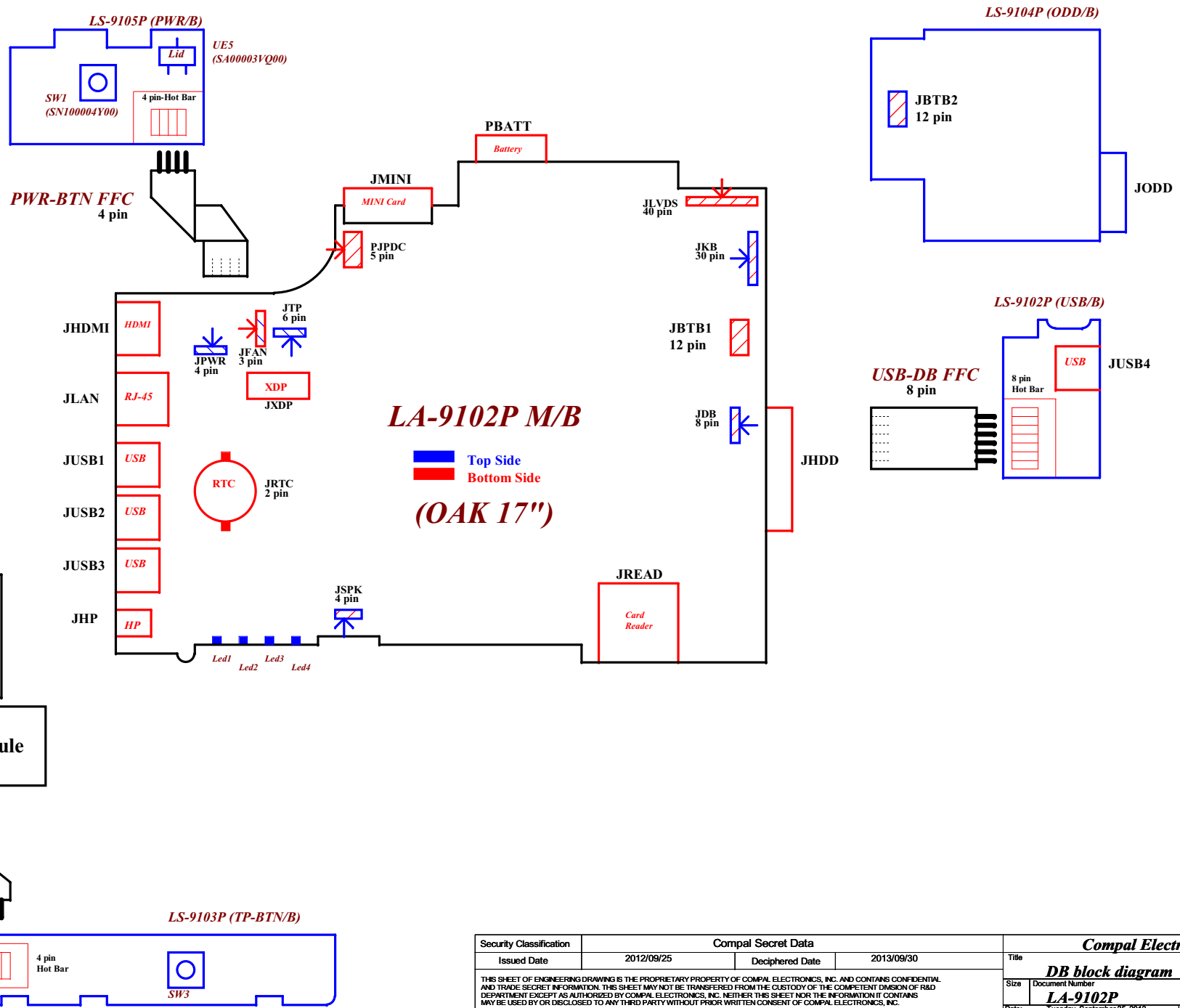


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Project Code : VAW11

File Name : LA-9102P



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Board ID Table for AD channel

Vcc	3.3V +/- 5%
Ra	100K +/- 5%

Board ID	Rb	V _{AD_BID} min	V _{AD_BID} typ	V _{AD_BID} max	EC AD3
0	0	0 V	0 V	0.155 V	0x00-0x0C
1	8.2K +/- 5%	0.168 V	0.250 V	0.362 V	0x0D-0x1C
2	18K +/- 5%	0.375 V	0.503 V	0.621 V	0x1D-0x30
3	33K +/- 5%	0.634 V	0.819 V	0.945 V	0x31-0x49
4	56K +/- 5%	0.958 V	1.185 V	1.359 V	0x4A-0x69
5	100K +/- 5%	1.372 V	1.650 V	1.838 V	0x6A-0x8E
6	200K +/- 5%	1.851 V	2.200 V	2.420 V	0x8F-0xBB
7	NC	2.433 V	3.300 V	3.300 V	0xBC-0xFF

BOARD ID Table

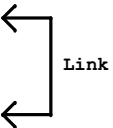
ID	PCB Revision
0	0.1
1	0.1
2	0.2
3	0.2
4	0.3
5	0.3
6	1.0
7	1.0

Project ID Table

ID	Project Revision
0	
1	
2	
3	
4	
5	UMA
6	DIS THAMES
7	DIS MARS PRO

SMBUS Control Table

	SOURCE	MINI1	MINI2	BATT	SODIMM	Express Card	Thermal Sensor	FFS	VGA Thermal Sensor	VGA	XDP	Charger
EC_SMB_CK1 EC_SMB_DA1	KB9012			V								V
EC_SMB_CK2 EC_SMB_DA2	KB9012								V	V		
PCH_SML0CLK PCH_SML0DATA	PCH											
PCH_SML1CLK PCH_SML1DATA	PCH											
MEM_SMBCLK MEM_SMBDATA	PCH	V	V		V	V		V			V	



PCH	USB PORT#	DESTINATION
	0	USB conn.2
	1	USB conn.1
	2	USB conn.3
	3	USB conn.4 (DB)
	4	NC
	5	NC
	6	NC
	7	NC
	8	MINI CARD (WLAN)
	9	NC
	10	Card Reader
	11	Camera
	12	NC
13	NC	

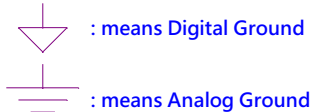
CLK	DIFFERENTIAL	DESTINATION	FLEX CLOCKS	DESTINATION
	CLKOUT_PCIE0	10/100 LAN	CLKOUTFLEX0	None
	CLKOUT_PCIE1	MINI CARD WLAN	CLKOUTFLEX1	None
	CLKOUT_PCIE2	None	CLKOUTFLEX2	None
	CLKOUT_PCIE3	None	CLKOUTFLEX3	None
	CLKOUT_PCIE4	None		
	CLKOUT_PCIE5	None		
	CLKOUT_PCIE6	None		
	CLKOUT_PCIE7	None		
CLKOUT_PEG_B	None			

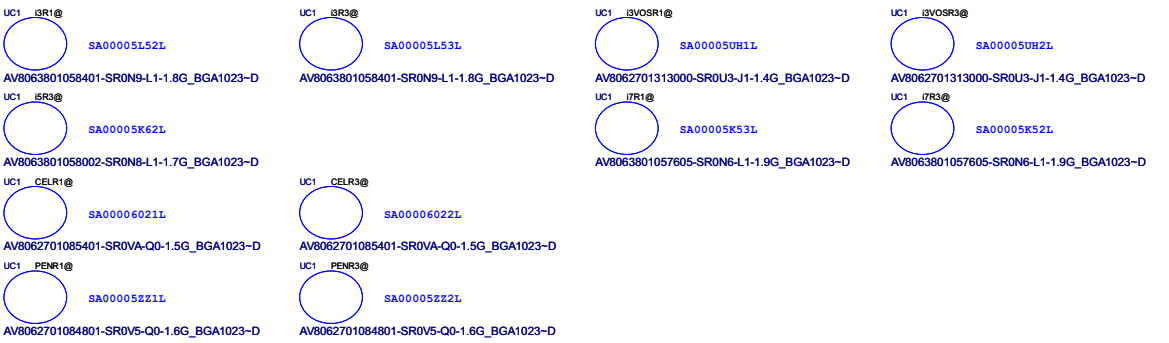
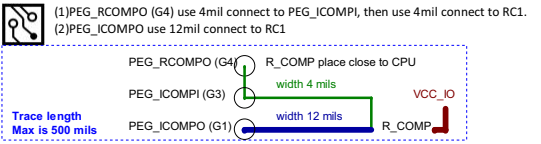
CLKOUT	DESTINATION
PCI0	PCH_LOOPBACK
PCI1	EC LPC
PCI2	None
PCI3	None
PCI4	None

SATA	DESTINATION
SATA0	HDD
SATA1	None
SATA2	ODD
SATA3	None
SATA4	None
SATA5	None

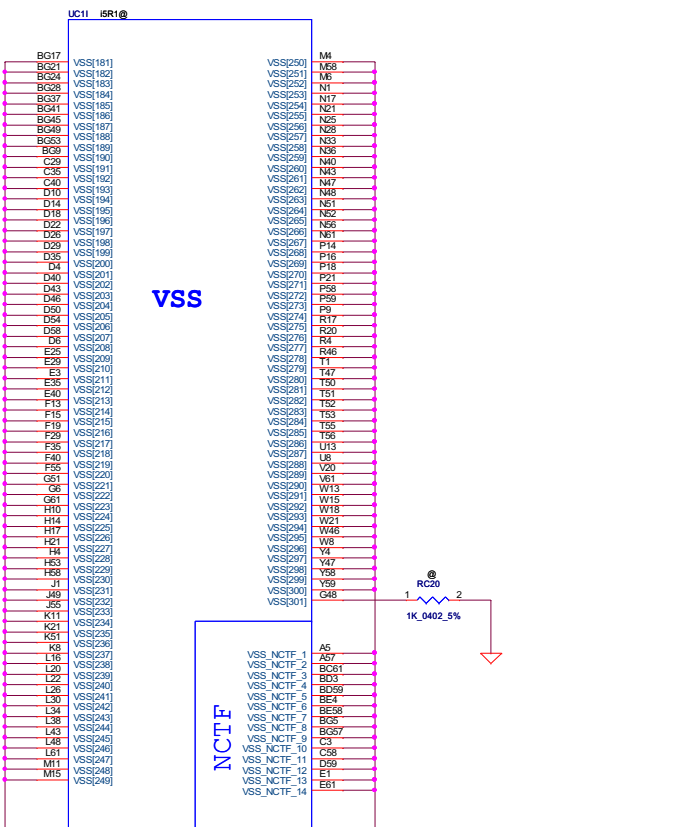
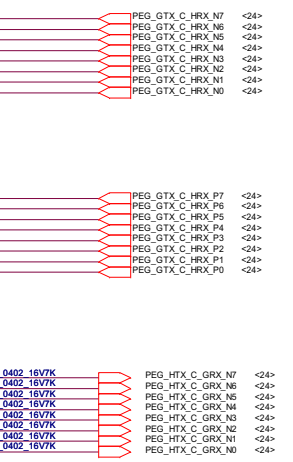
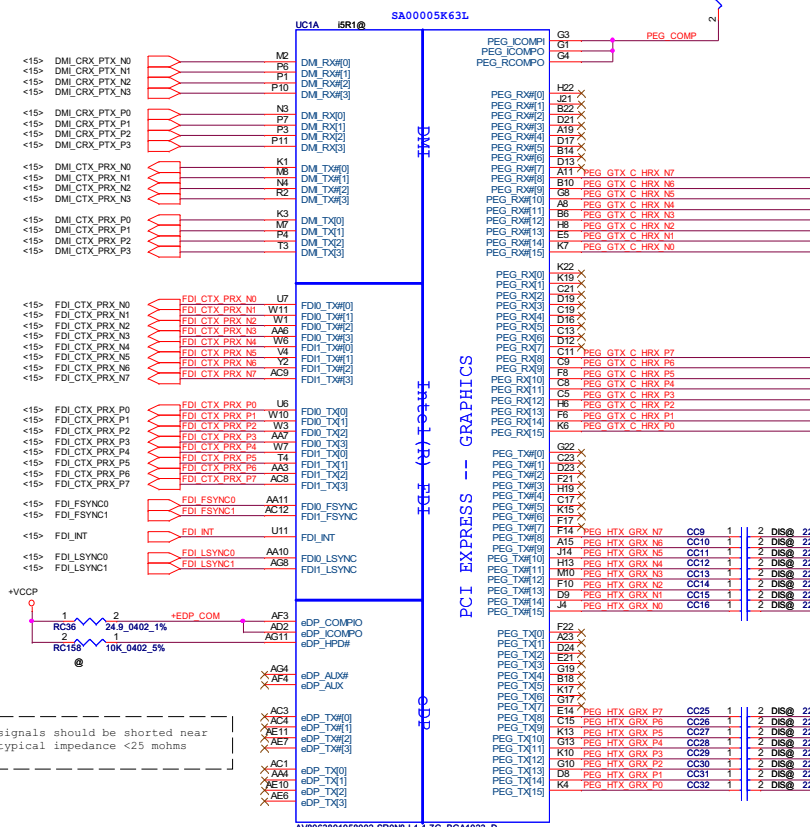
PCI EXPRESS	DESTINATION
Lane 1	10/100 LAN
Lane 2	MINI CARD (WLAN)
Lane 3	None
Lane 4	None
Lane 5	None
Lane 6	None
Lane 7	None
Lane 8	None

Symbol Note :

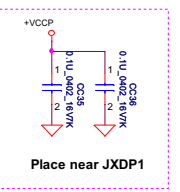
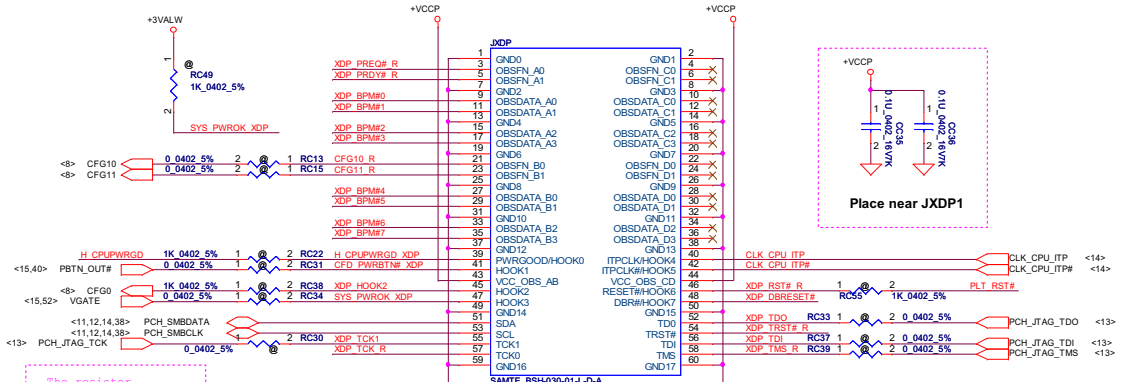




PEG_ICOMPI and RCOMP0 signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 mohms
 PEG_ICOMPU signals should be routed with - max length = 500 mils - typical impedance = 14.5 mohms

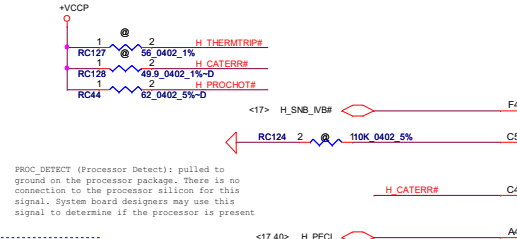
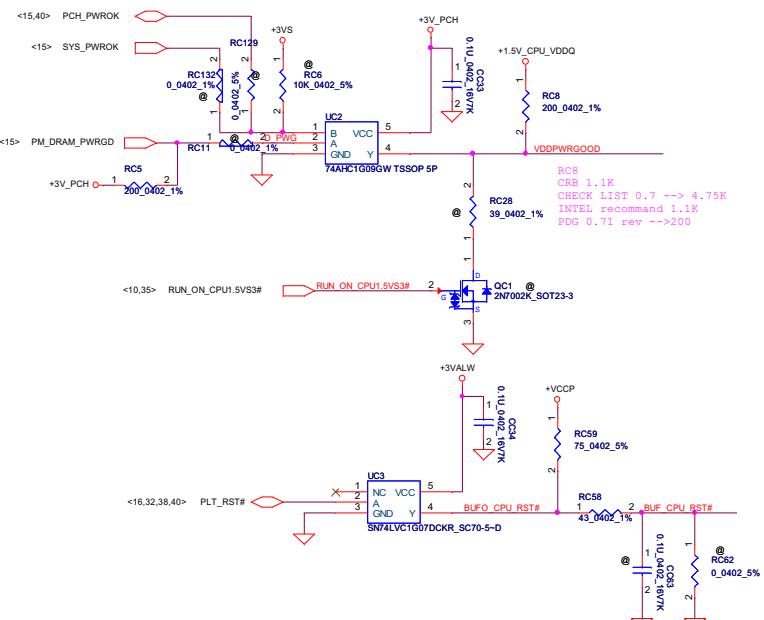


eDP_COMPIO and ICOMPU signals should be shorted near balls and routed with typical impedance <25 mohms

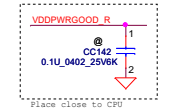
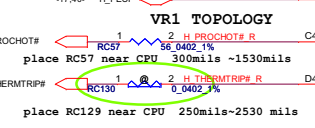
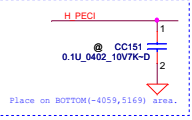


The resistor for HOOK2 should be placed such that the stub is very small on CFG0 net

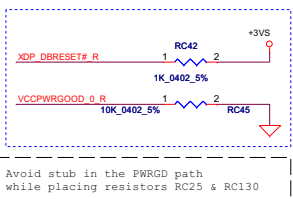
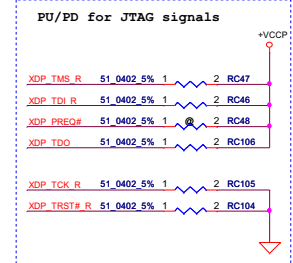
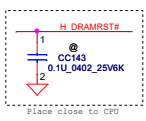
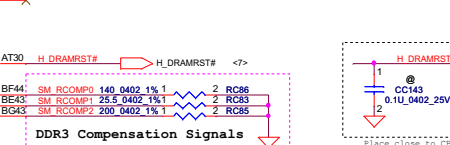
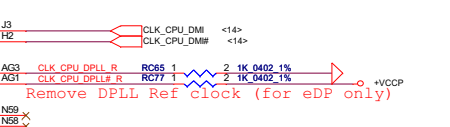
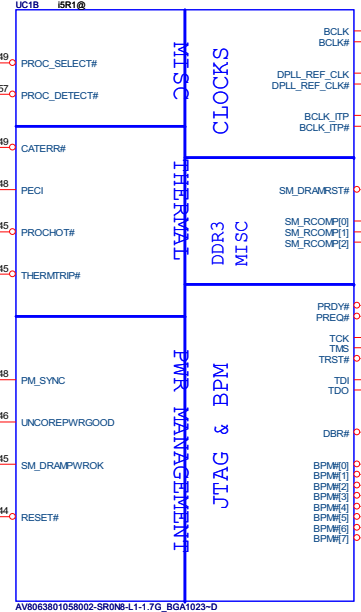
SP02000L900



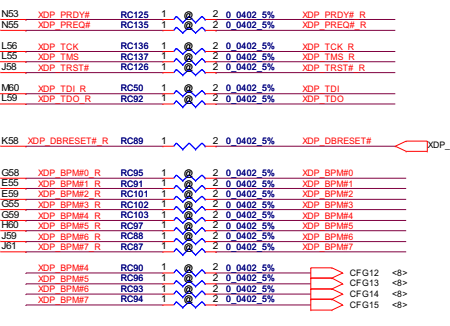
PROC_DETECT (Processor Detect): pulled to ground on the processor package. There is no connection to the processor silicon for this signal. System board designers may use this signal to determine if the processor is present

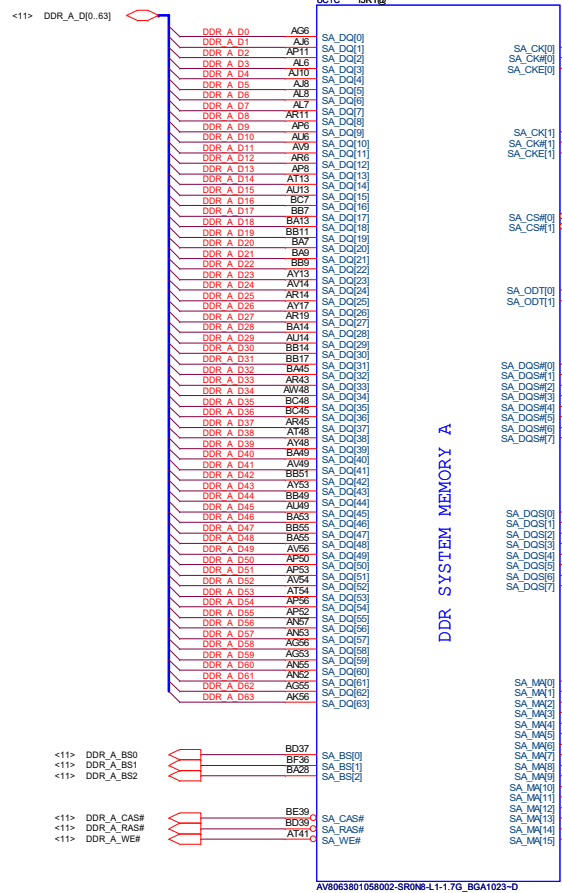


ESD request to reserve CC141

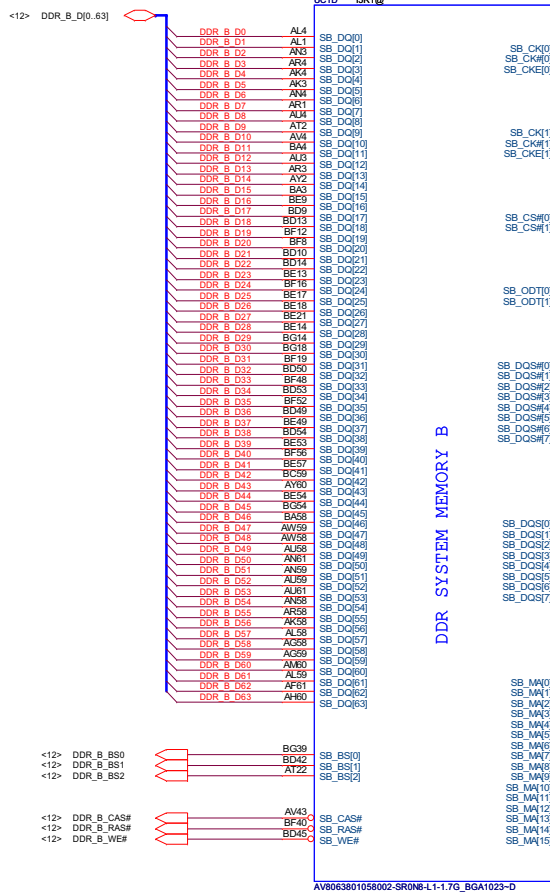


Avoid stub in the PWRGD path while placing resistors RC25 & RC130

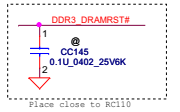
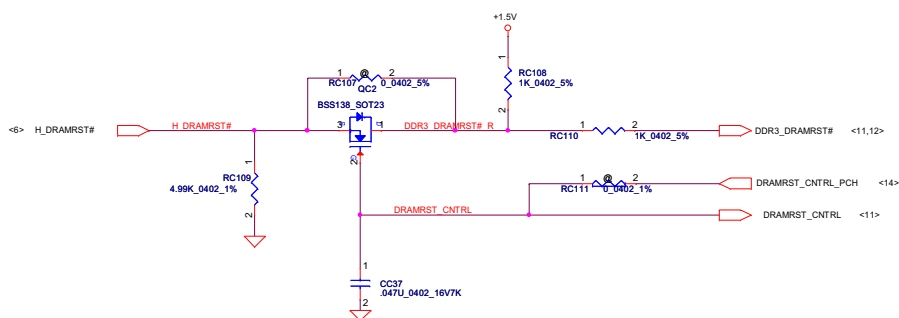




DDR SYSTEM MEMORY A

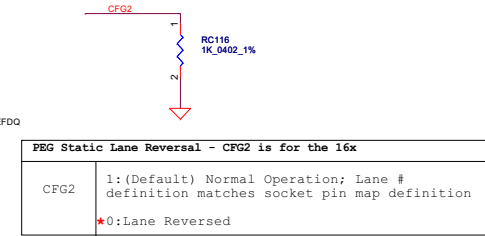
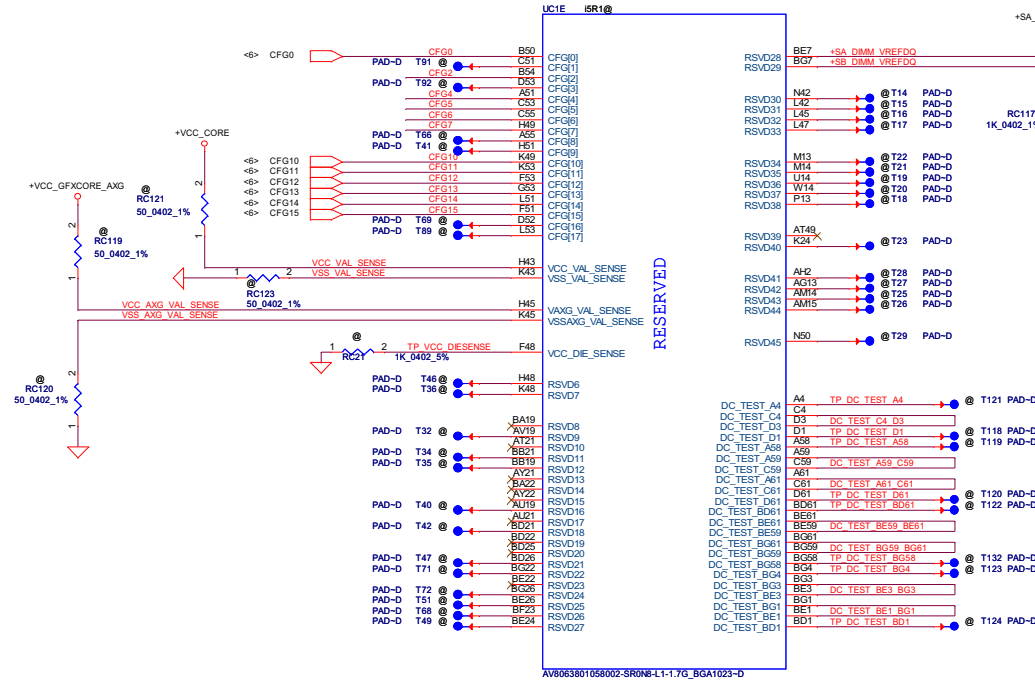


DDR SYSTEM MEMORY B



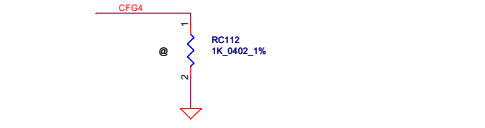
Security Classification	Compal Secret Data		Title	
Issued Date	2012/09/25	Deciphered Date	2013/09/30	PROCESSOR(3/6) DDRIII
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CFG Straps for Processor



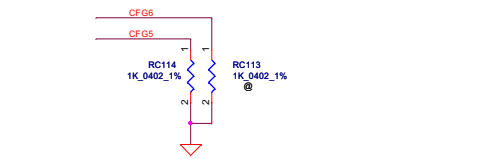
PEG Static Lane Reversal - CFG2 is for the 16x

CFG2	1: (Default) Normal Operation; Lane # definition matches socket pin map definition *0: Lane Reversed
------	---



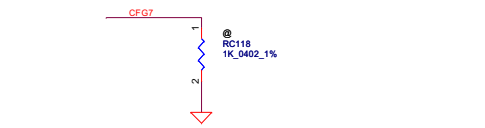
Display Port Presence Strap

CFG4	*1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port
------	---



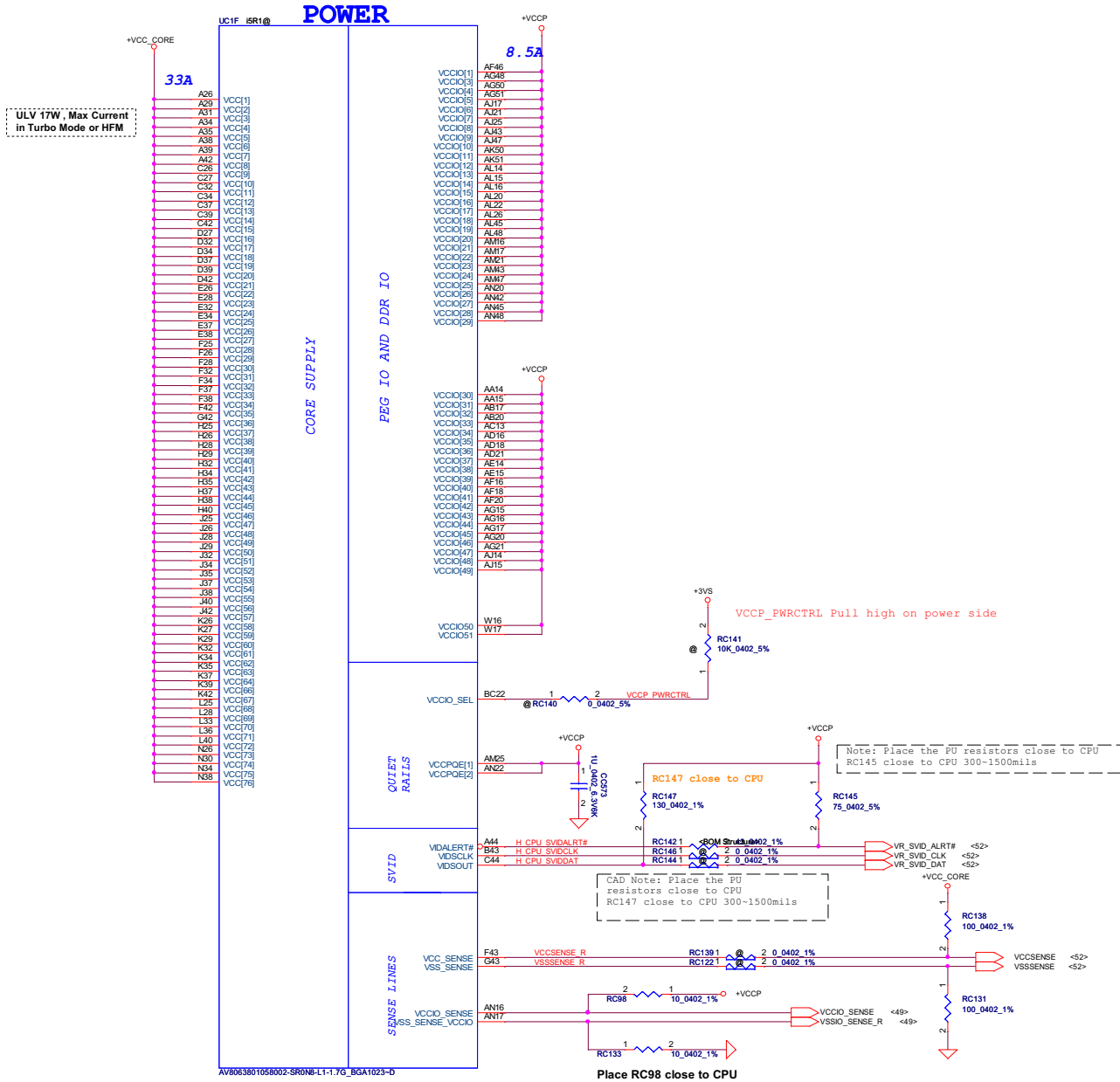
PCIe Port Bifurcation Straps

CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled *10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled
----------	---



PEG DEFER TRAINING

CFG7	*1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training
------	--



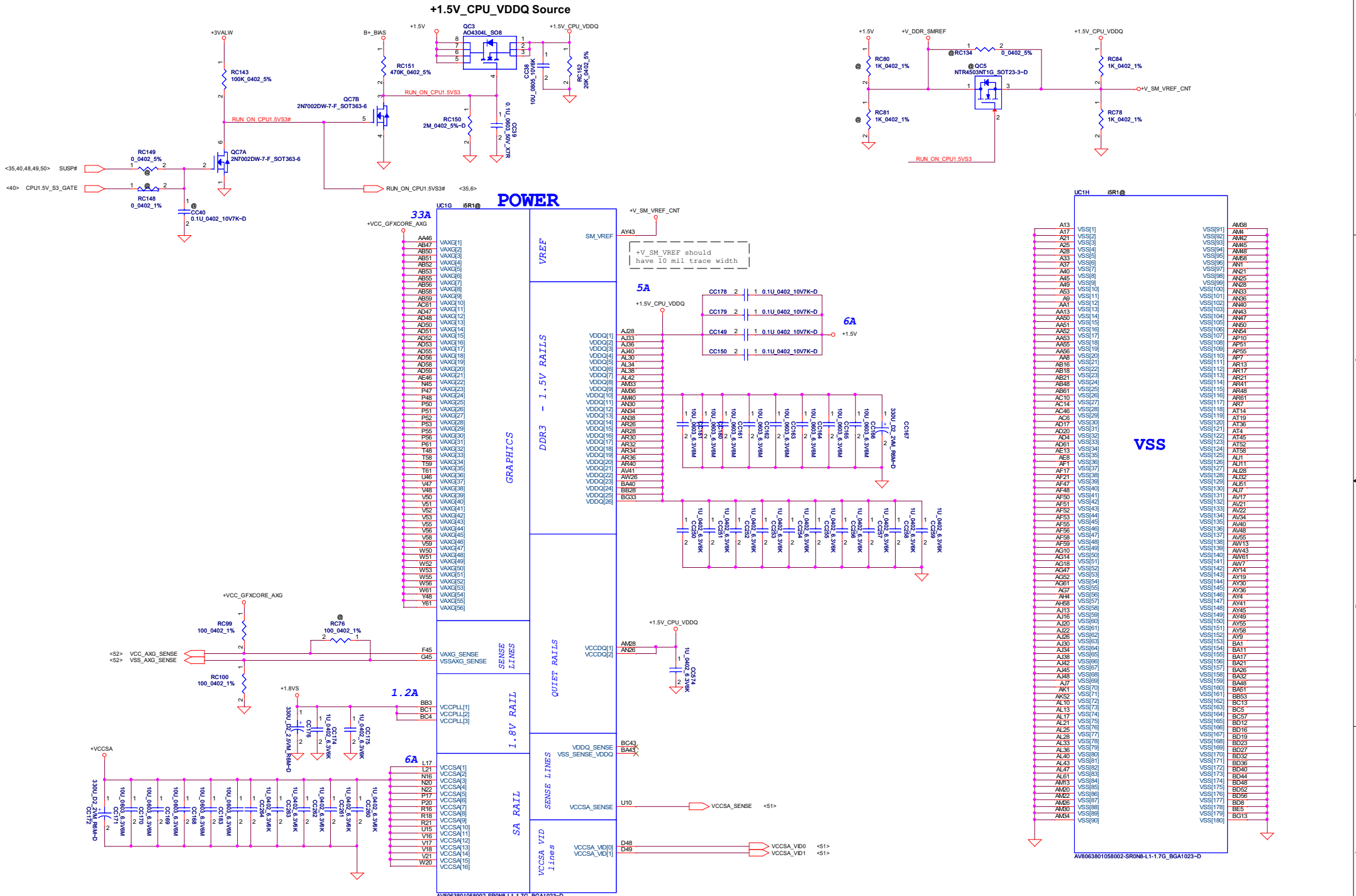
ULV 17W . Max Current in Turbo Mode or HFM

Iccmax current changed for PDDG Rev0.7

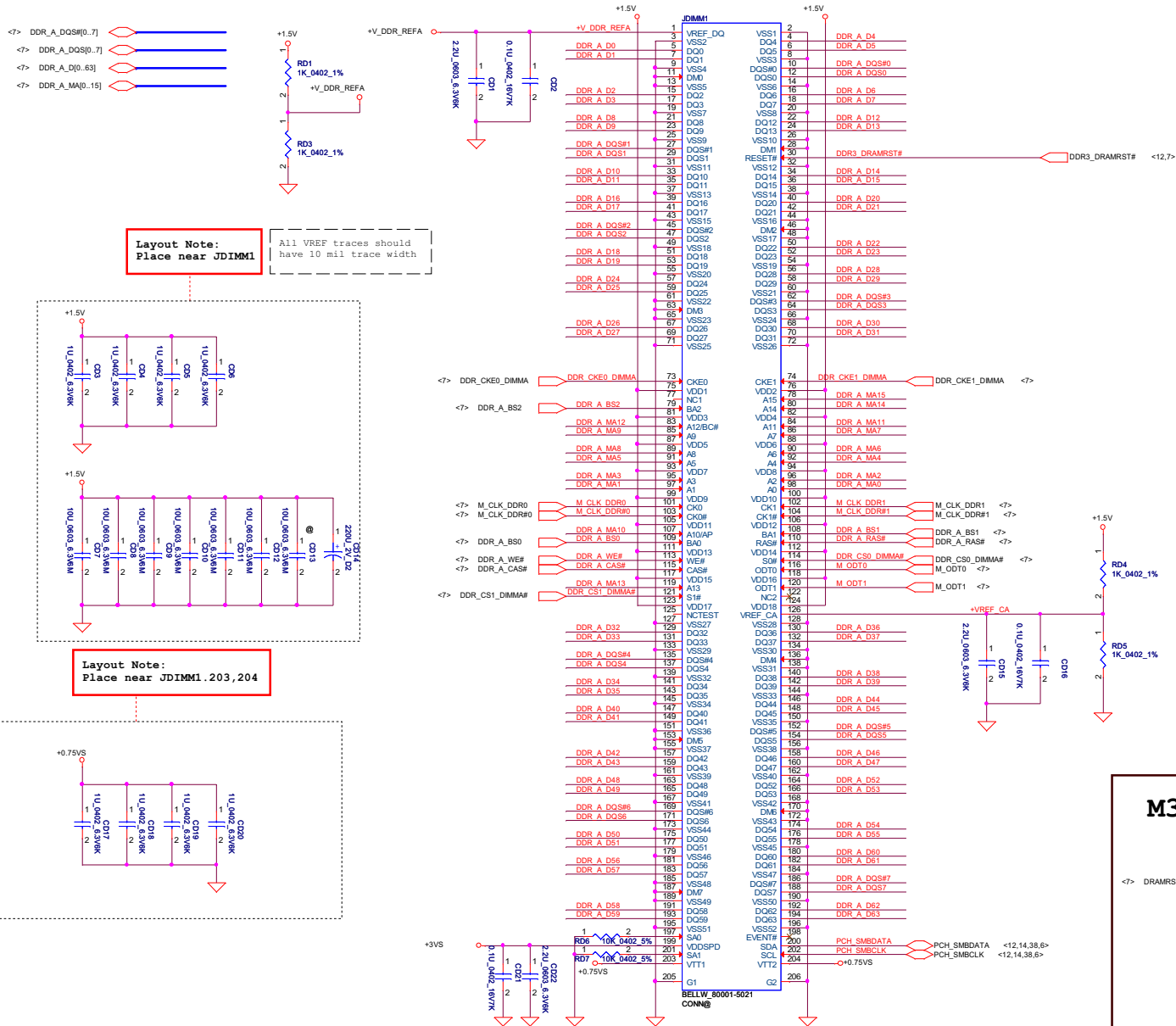
CPU Power Rail Table		
Voltage Rail	Voltage	80 Iccmax Current (A)
VCC	0.65-1.3	53
VCCIO	1.05/1	8.5
VAXG	0.0-1.1	33
VCCPLL	1.8	1.2
VDDQ	1.5	5
VCCSA	0.65-0.9	6
+1.5V_MEM	1.5	12-16 *

* Description
 5A to Mem controller(+1.5V_CPU_VDDQ)
 5-6A to 2 DIMMs/channel
 2-5A to +1.5V_RUN & +0.75V_DDR_VTT

AV8083801058002-3R0N8-L1-1.7G_BGA1023-0

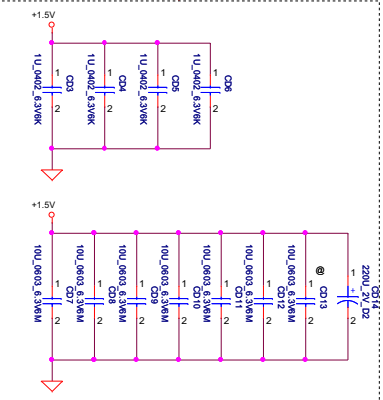


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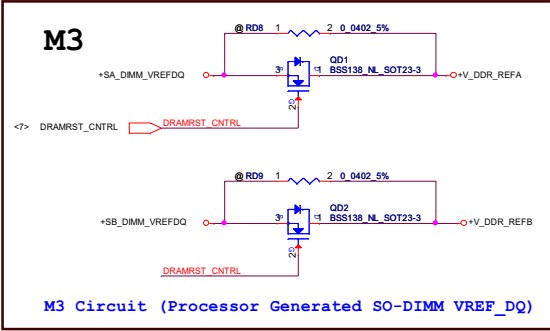
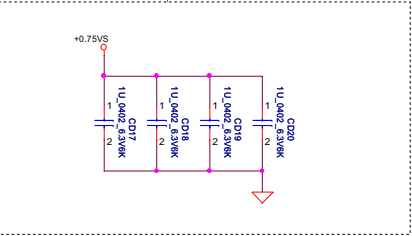


Layout Note:
Place near JDIMM1

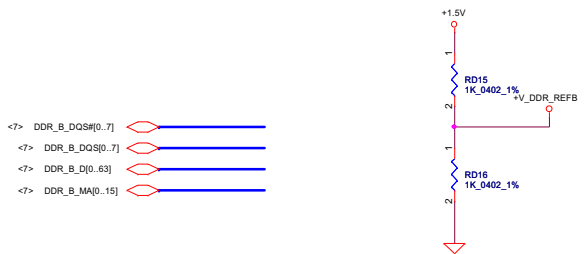
All VREF traces should have 10 mil trace width



Layout Note:
Place near JDIMM1.203,204



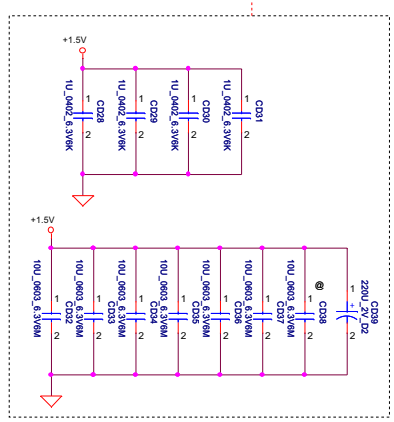
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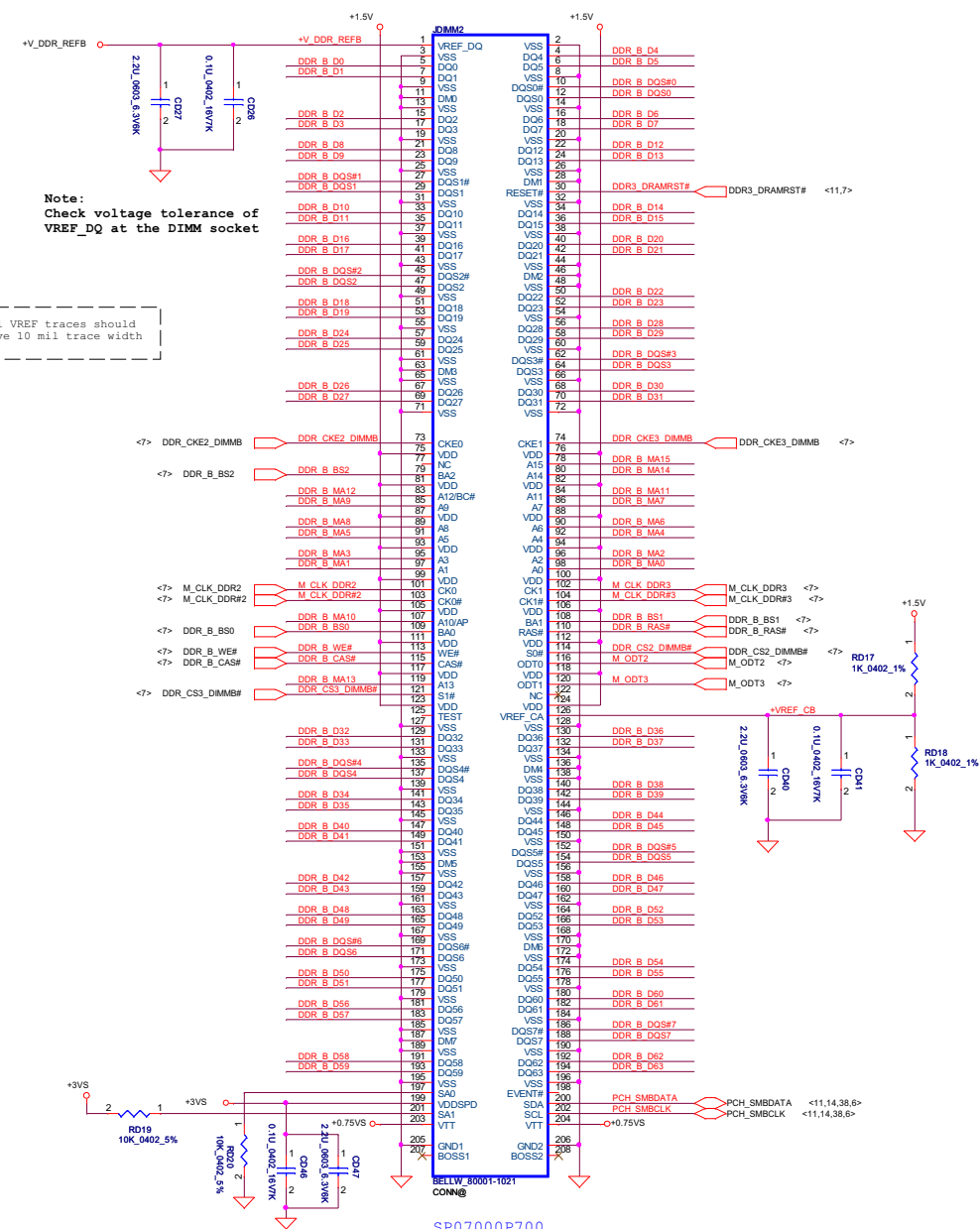
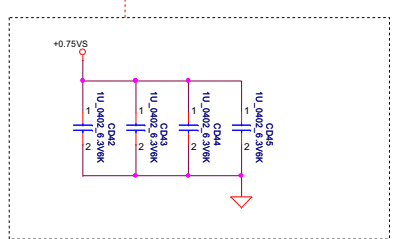
Note:
Check voltage tolerance of
VREF_DQ at the DIMM socket

All VREF traces should
have 10 mil trace width

Layout Note:
Place near JDIMMB

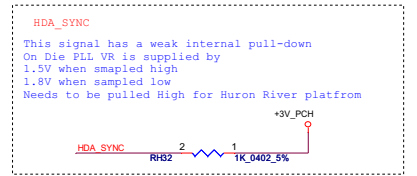
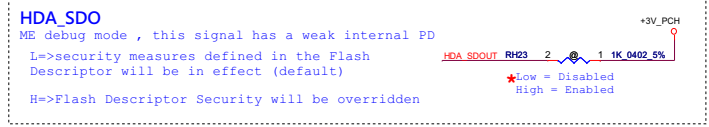
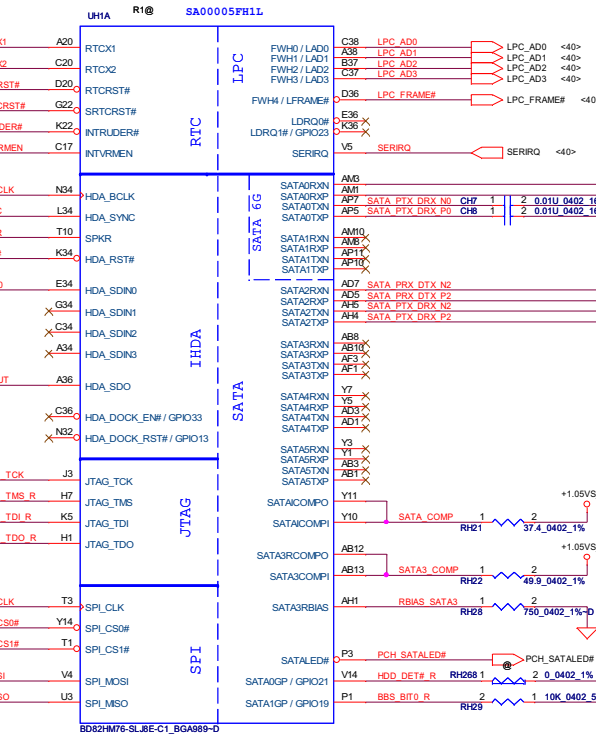
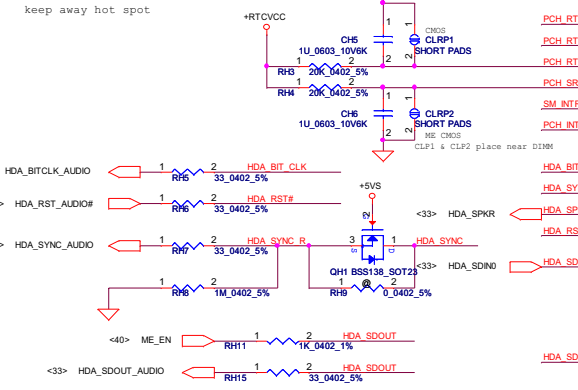
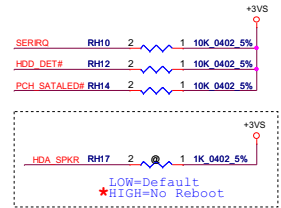
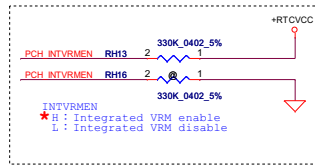
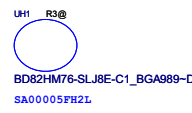
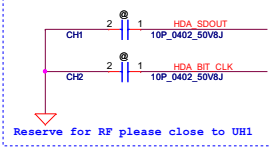
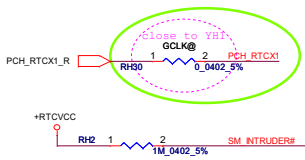
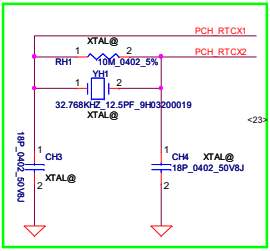


Layout Note:
Place near JDIMMB.203,204

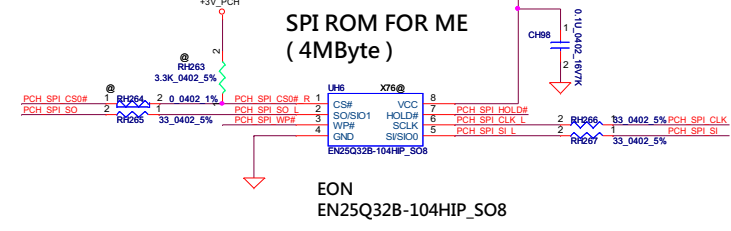
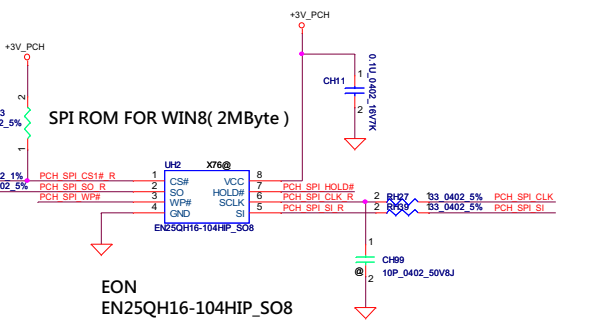
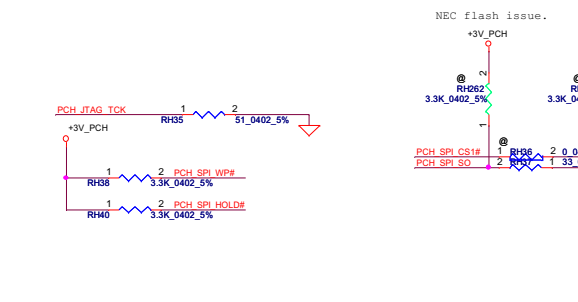
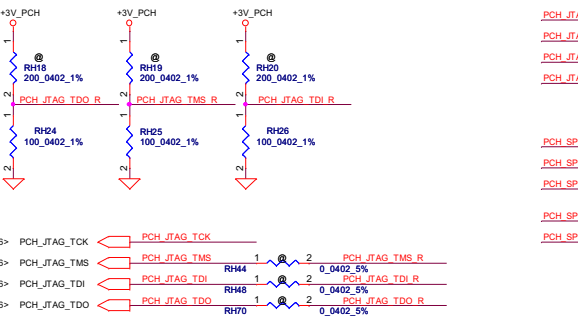
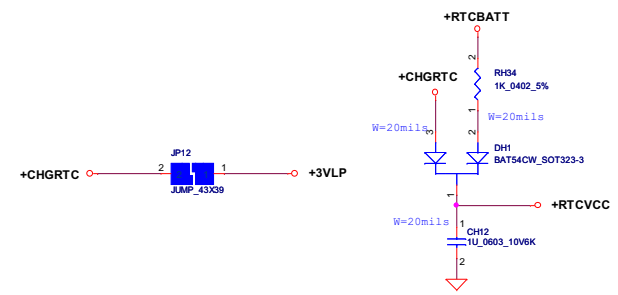


SP07000P700

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Date:		Tuesday, September 25, 2012	Sheet 12 of 57	

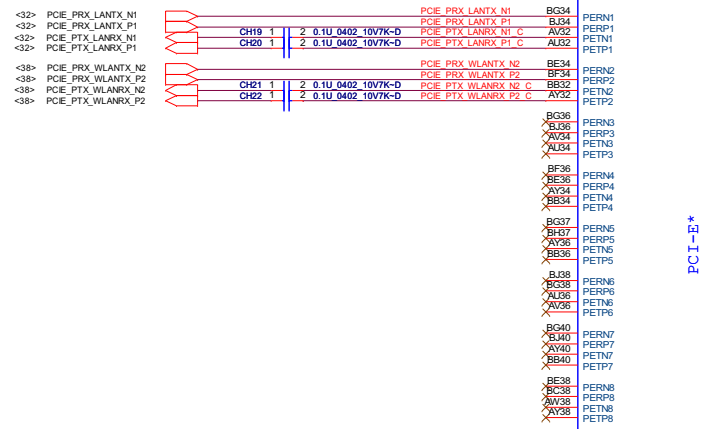


RTC Battery



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Issued Date	2012/09/25	Deciphered Date	2013/09/30	PCH (1/8) SATA/HDA/SPI/LPC	
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Size	Document Number	Date:		Rev	1.0
	LA.9102P	Tuesday, September 25, 2012		Sheet	13 of 57

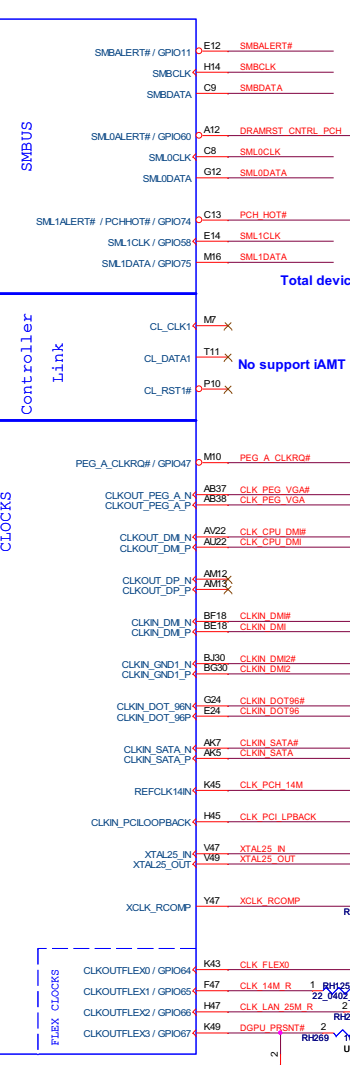
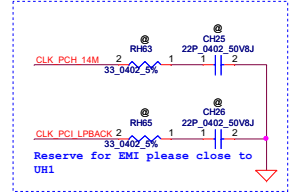
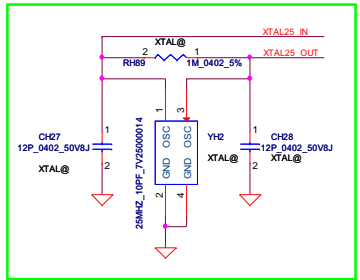
10/100 LAN ---->
 WLAN (Mini Card)---->



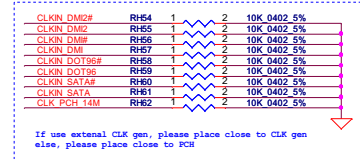
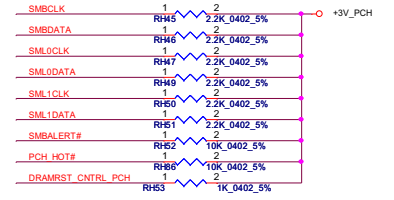
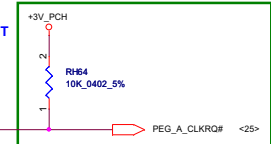
10/100 LAN ---->
 WLAN (Mini Card)---->



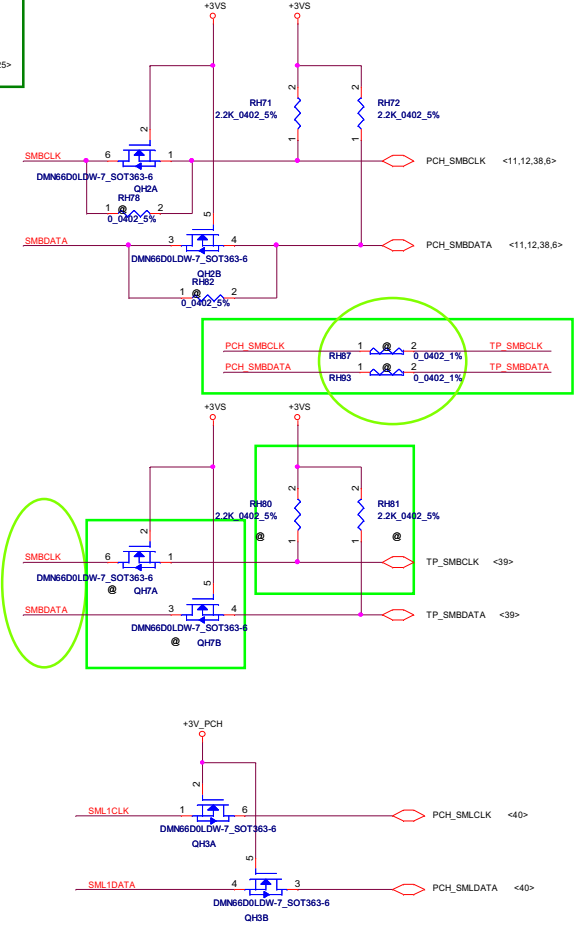
*PCIE REQ power rail:
 suspend: 0 3 4 5 6 7
 core: 12



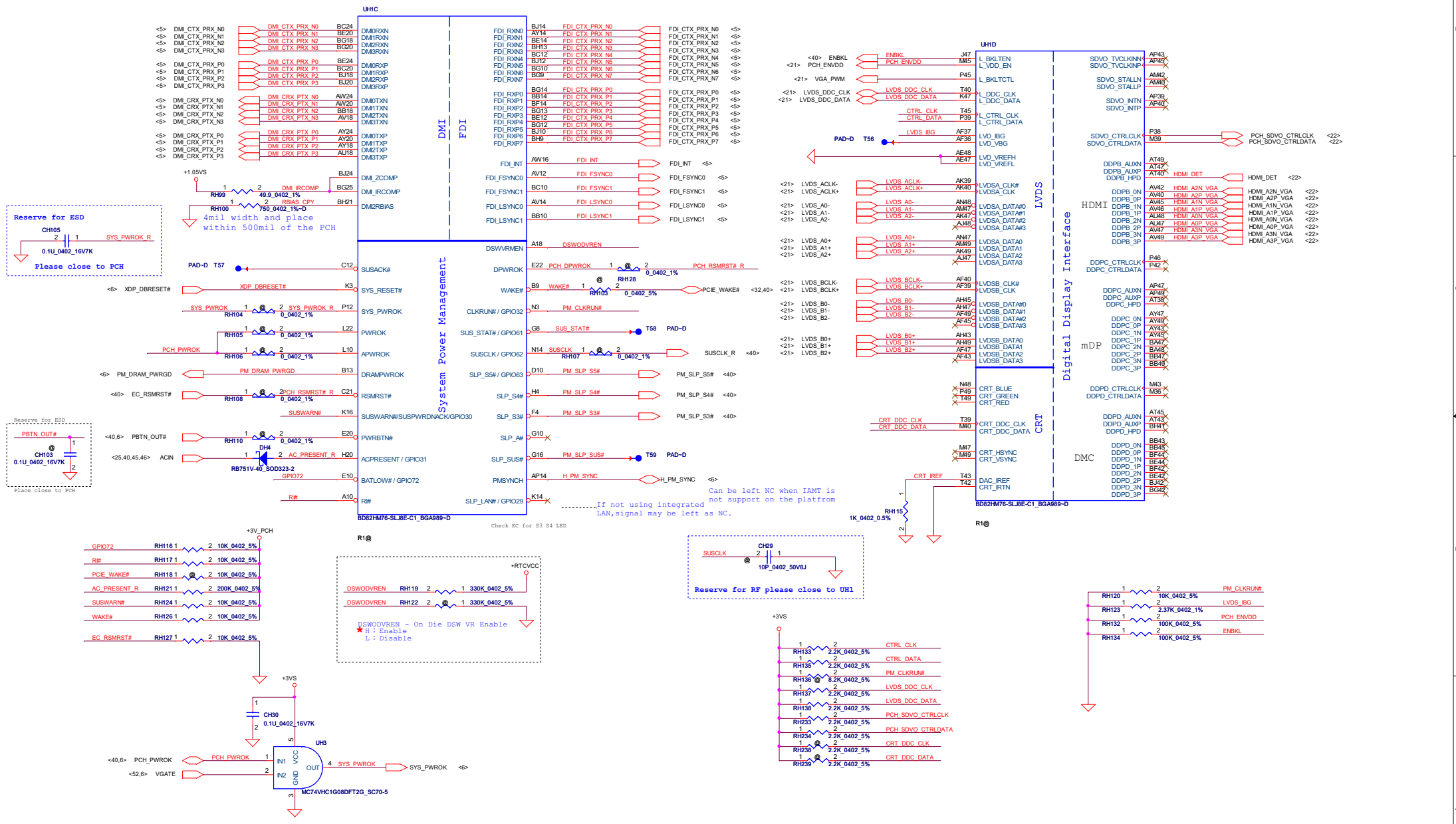
Total device
 20090512
 add double mosfet prevent
 ATI M92 electric leakage



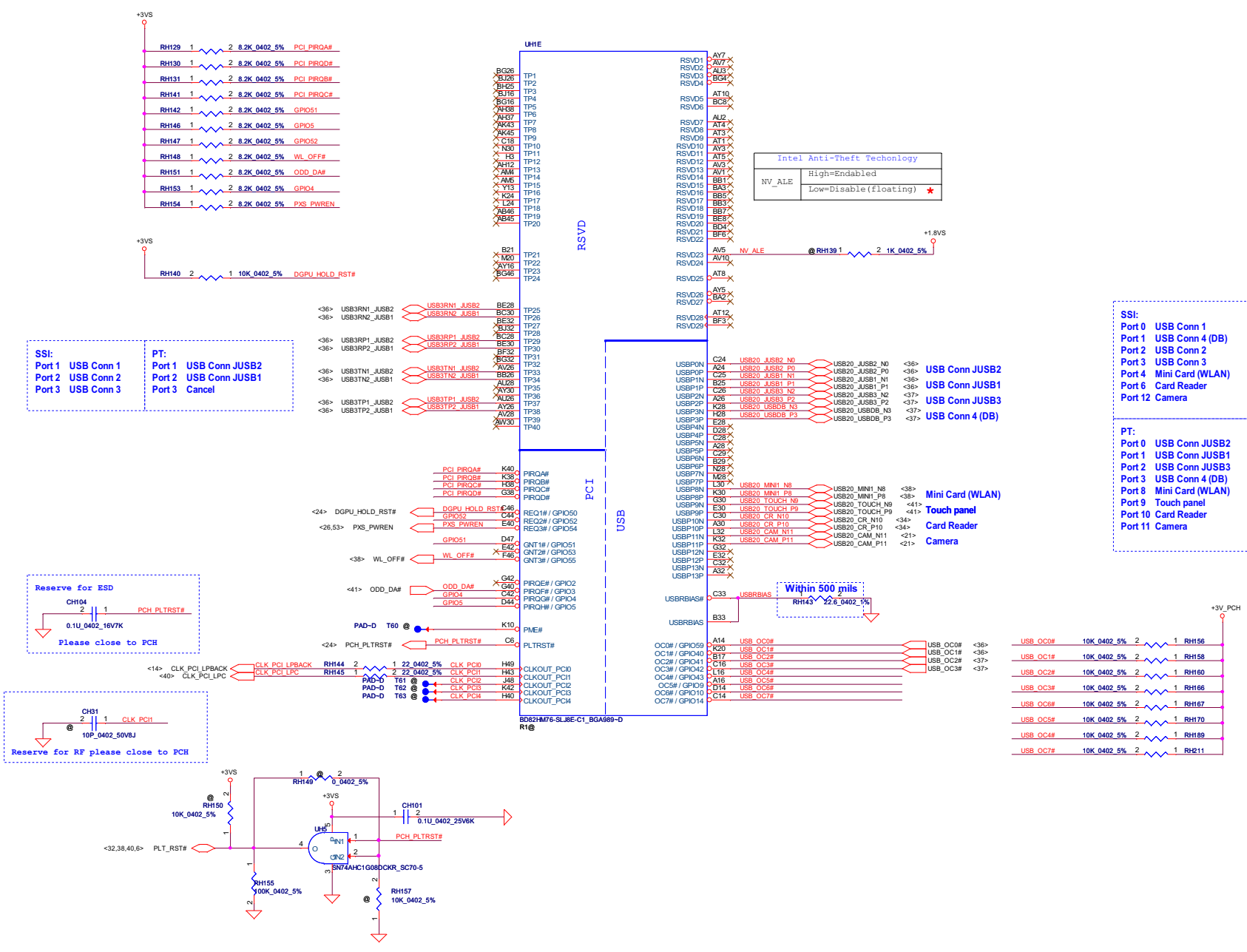
If use external CLK gen, please place close to CLK gen
 else, please place close to PCH



Security Classification	Compal Secret Data		Title	
Issued Date	2012/09/25	Deciphered Date	2013/09/30	PCH (2/8) PCIE/SMBUS/CLK
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Date:	Tuesday, September 25, 2012	Sheet	14	of 57



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2012/09/25	Deciphered Date	2013/09/30	Title	PCH (3/8) DMI/FDI/PM/GFX/DP
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				LA-9102P	Rev 1.0
				Date:	Tuesday, September 25, 2012
				Sheet	15 of 57



Intel Anti-Theft Technology	
NV_ALE	High=Enabled
	Low=Disable(floating) *

SSI:
Port 1 USB Conn 1
Port 2 USB Conn 2
Port 3 USB Conn 3

PT:
Port 1 USB Conn JUSB2
Port 2 USB Conn JUSB1
Port 3 Cancel

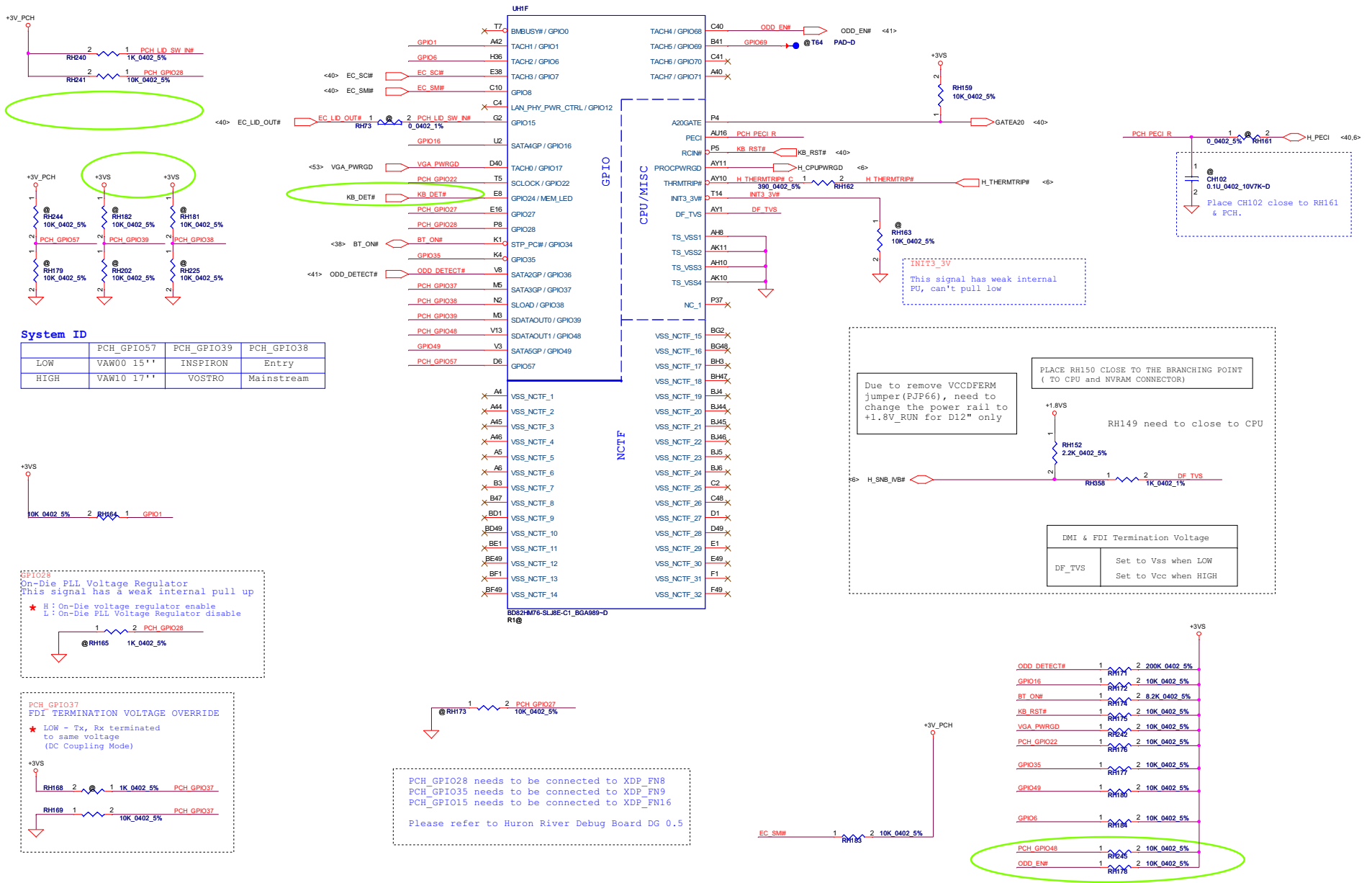
SSI:
Port 0 USB Conn 1
Port 1 USB Conn 4(DB)
Port 2 USB Conn 2
Port 3 USB Conn 3
Port 4 Mini Card (WLAN)
Port 6 Card Reader
Port 12 Camera

PT:
Port 0 USB Conn JUSB2
Port 1 USB Conn JUSB1
Port 2 USB Conn JUSB3
Port 3 USB Conn 4(DB)
Port 8 Mini Card (WLAN)
Port 9 Touch panel
Port 10 Card Reader
Port 11 Camera

Reserve for ESD
CH04 2 1 1 PCH_PLTRST#
0.1u_0402_16V7K
Please close to PCH

Reserve for RF please close to PCH
CH1 2 1 1 CLK_PCH#
10P_0402_50V8J

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Issued Date	2012/09/25	Deciphered Date	2013/09/30
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Rev	1.0		



System ID

	PCH_GPIO57	PCH_GPIO39	PCH_GPIO38
LOW	VAW00 15''	INSPIRON	Entry
HIGH	VAW10 17''	VOSTRO	Mainstream

PCH_GPIO28
On-Die PLL Voltage Regulator
This signal has a weak internal pull up
* H : On-Die voltage regulator enable
* L : On-Die PLL Voltage Regulator disable

PCH_GPIO37
FDI TERMINATION VOLTAGE OVERRIDE
* LOW - Tx, Rx terminated to same voltage (DC Coupling Mode)

PCH_GPIO28 needs to be connected to XDP_FN8
PCH_GPIO35 needs to be connected to XDP_FN9
PCH_GPIO15 needs to be connected to XDP_FN16
Please refer to Huron River Debug Board DG 0.5

Due to remove VCCDFERM jumper (RJP66), need to change the power rail to +1.8V_RUN for D12" only

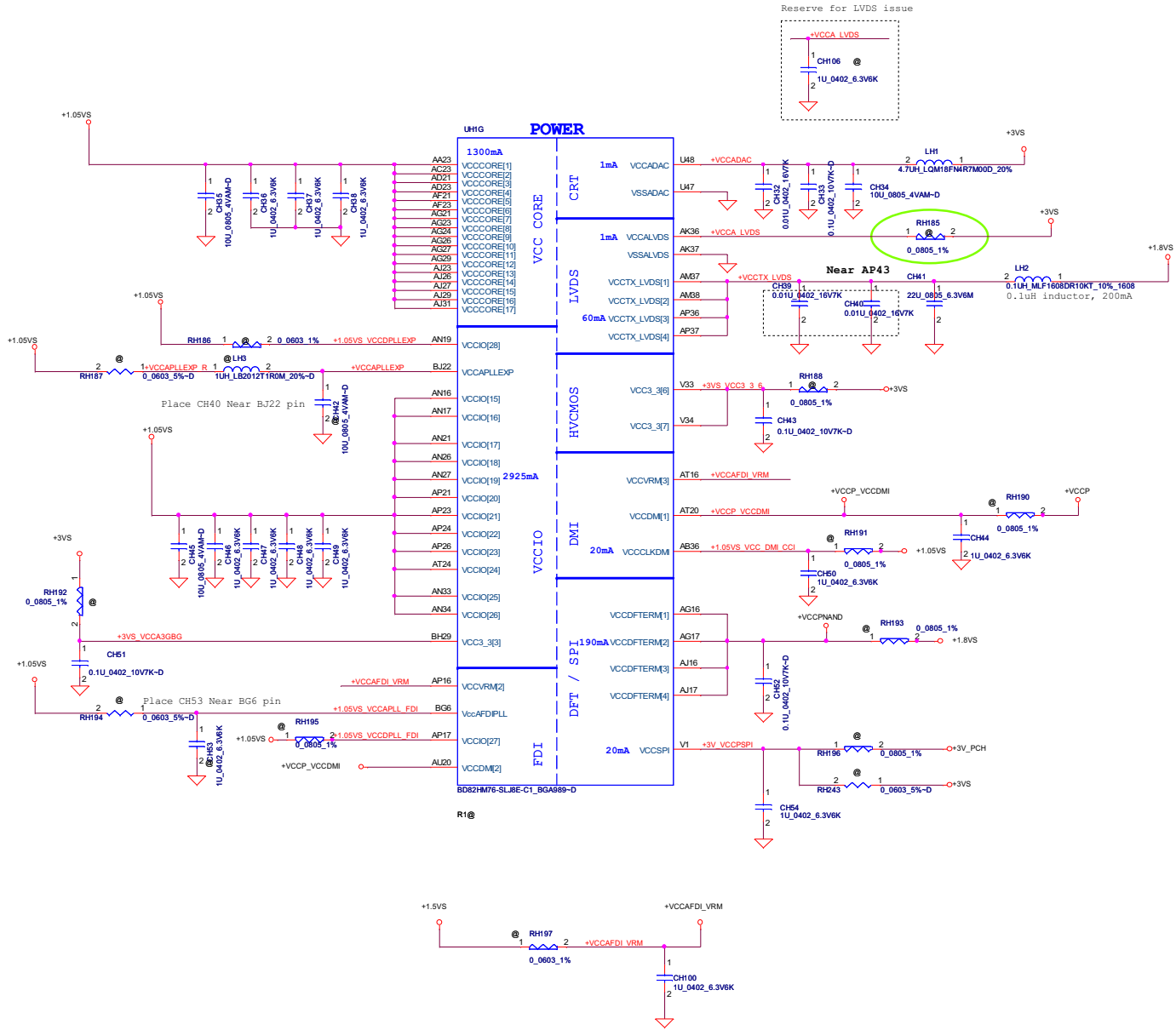
PLACE RH150 CLOSE TO THE BRANCHING POINT (TO CPU AND NVRAM CONNECTOR)

RH149 need to close to CPU

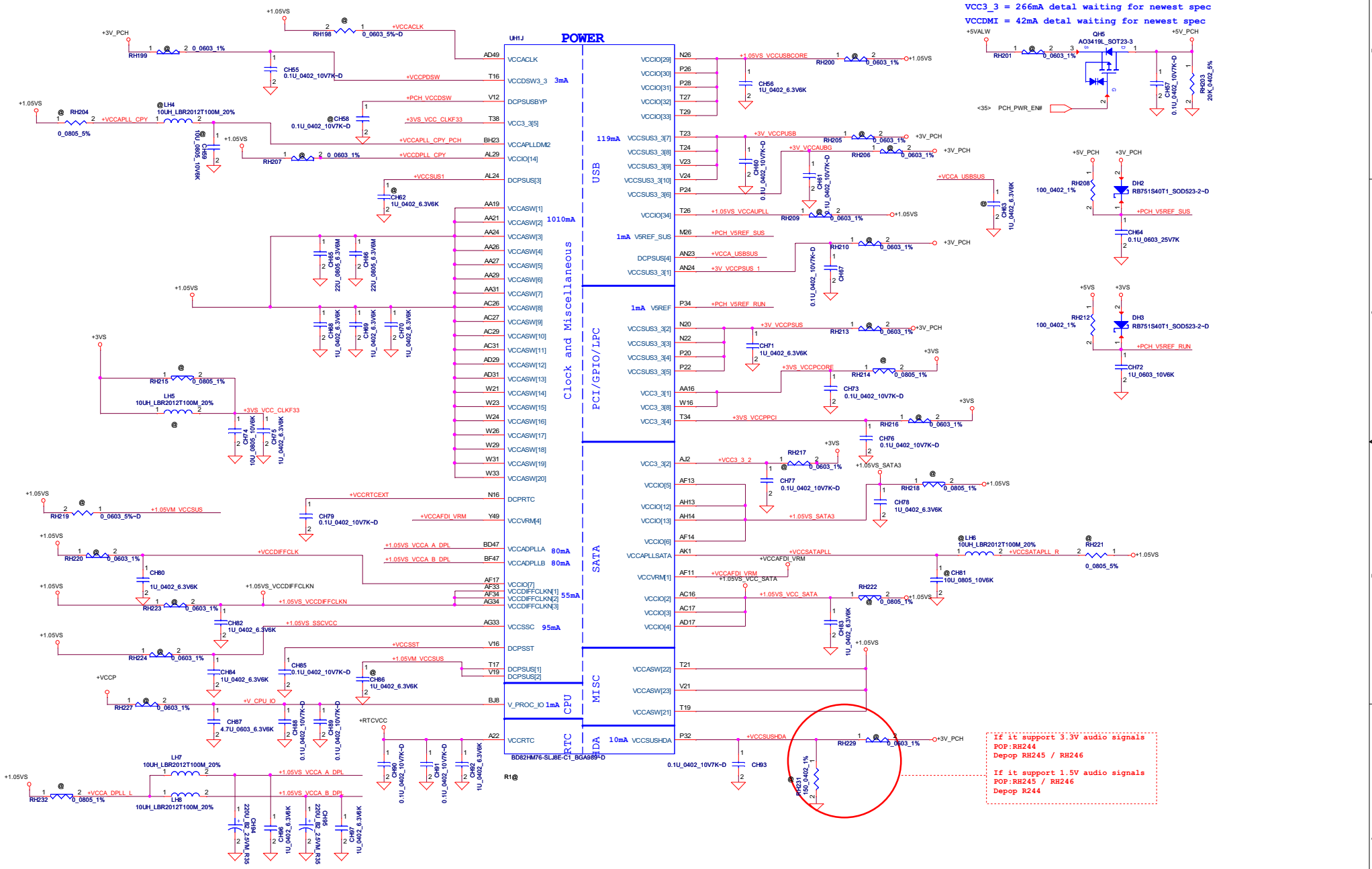
INIT3_3V
This signal has weak internal PU, can't pull low

DMi & FDI Termination Voltage

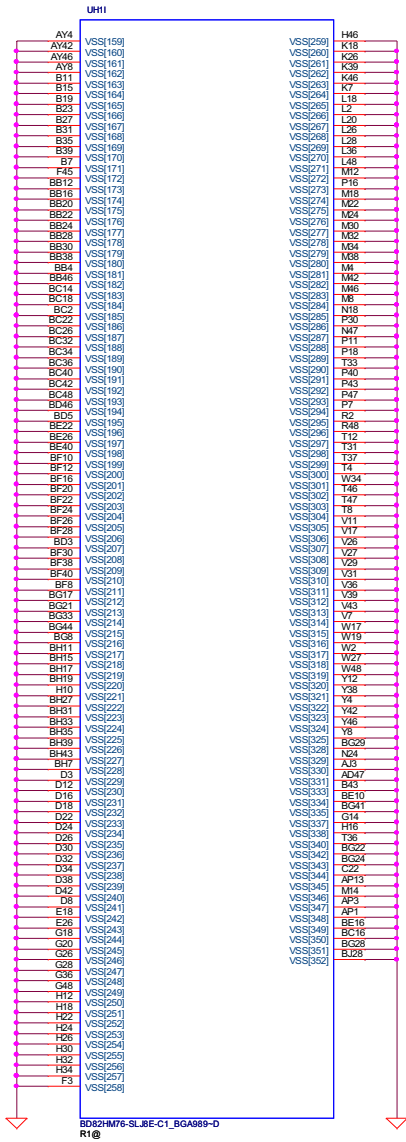
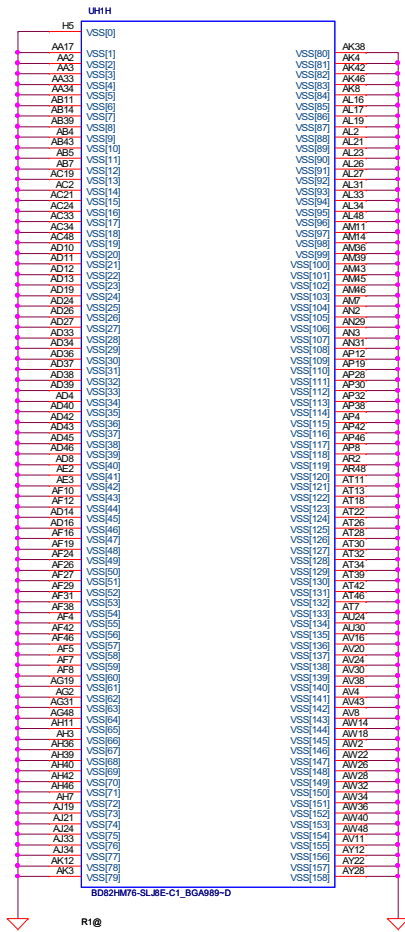
DF_TVS	Set to Vss when LOW
	Set to Vcc when HIGH



PCH Power Rail Table		
Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW	3.3	0.003
VccpNAND	1.8	0.19
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.119
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.16
VccCLRDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.06

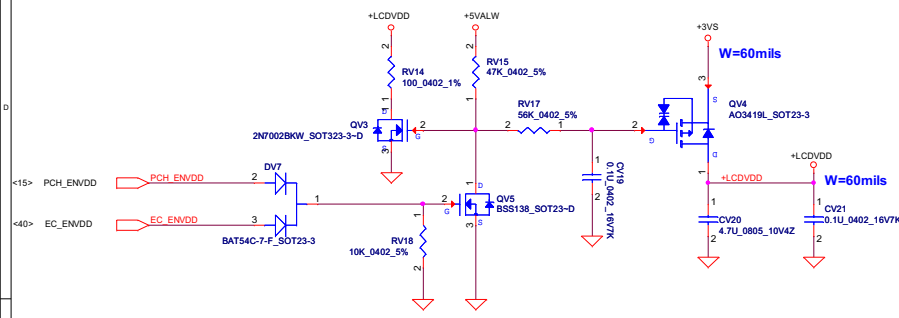


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Issued Date	2012/09/25	Deciphered Date	2013/09/30	PCH (7/8) PWR	
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				LA-9102P	Rev 1.0
				Date:	Tuesday, September 25, 2012 Sheet 19 of 57

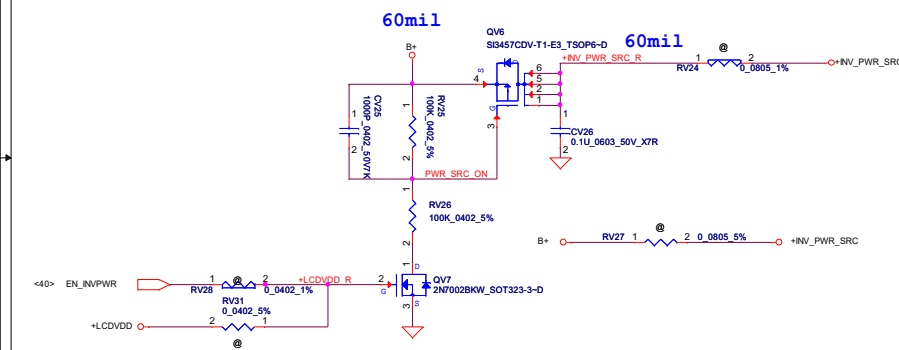


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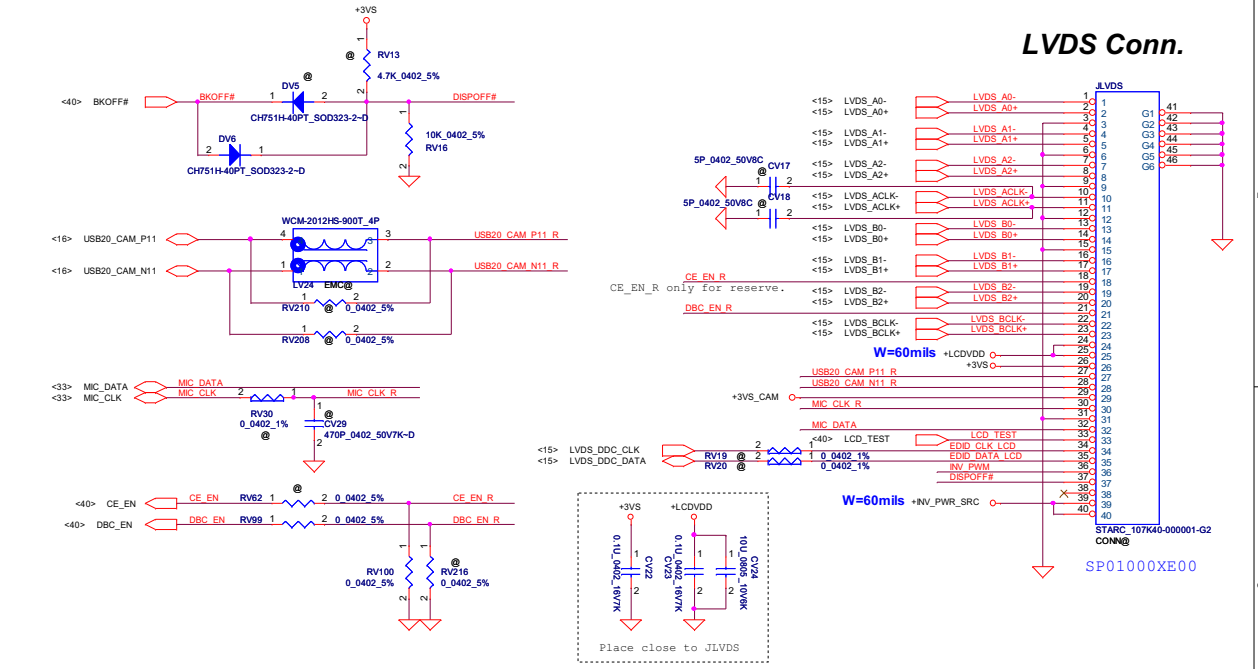
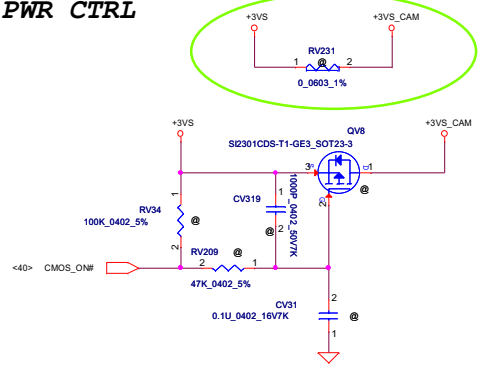
LCD PWR CTRL



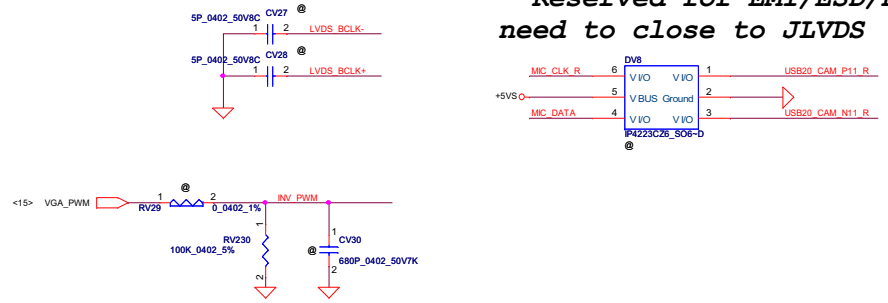
LCD backlight PWR CTRL



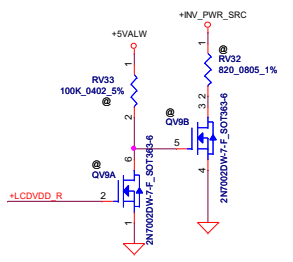
Webcam PWR CTRL



*** Reserved for EMI/ESD/RF need to close to JLVDS**

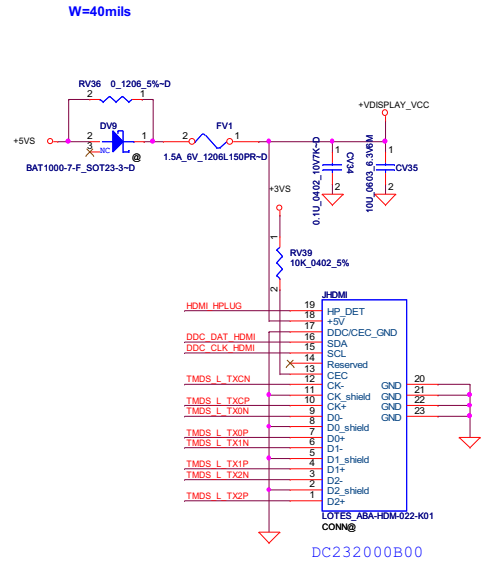
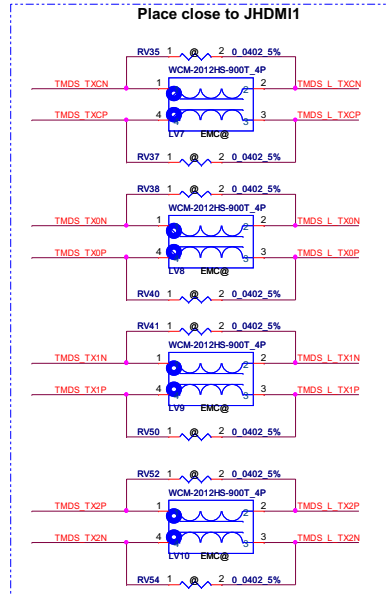
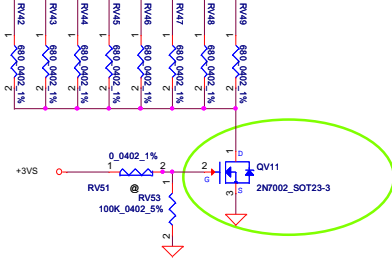


*** Reserved for LCD sequence tuning**



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<15>	HDMI_A3N_VGA	CV32	2	1	0.1U	0402	10V7K-D	TMDS_TXCN							
<15>	HDMI_A3P_VGA	CV33	2	1	0.1U	0402	10V7K-D	TMDS_TXCP							
<15>	HDMI_A6N_VGA	CV36	2	1	0.1U	0402	10V7K-D	TMDS_TXCN							
<15>	HDMI_A6P_VGA	CV37	2	1	0.1U	0402	10V7K-D	TMDS_TXCP							
<15>	HDMI_A1N_VGA	CV38	2	1	0.1U	0402	10V7K-D	TMDS_TXIN							
<15>	HDMI_A1P_VGA	CV39	2	1	0.1U	0402	10V7K-D	TMDS_TXIP							
<15>	HDMI_A2N_VGA	CV40	2	1	0.1U	0402 </tr <tr> <td><15></td> <td>HDMI_A2P_VGA</td> <td>CV41</td> <td>2</td> <td>1</td> <td>0.1U</td> <td>0402</td> <td>10V7K-D</td> <td>TMDS_TXCP</td> </tr>	<15>	HDMI_A2P_VGA	CV41	2	1	0.1U	0402	10V7K-D	TMDS_TXCP
<15>	HDMI_A2P_VGA	CV41	2	1	0.1U	0402	10V7K-D	TMDS_TXCP							

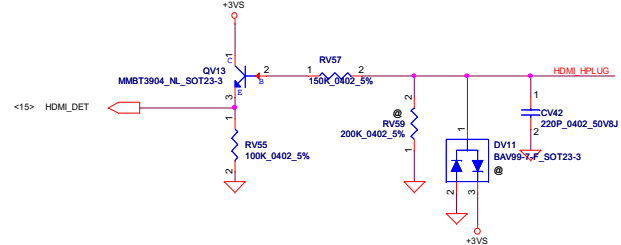
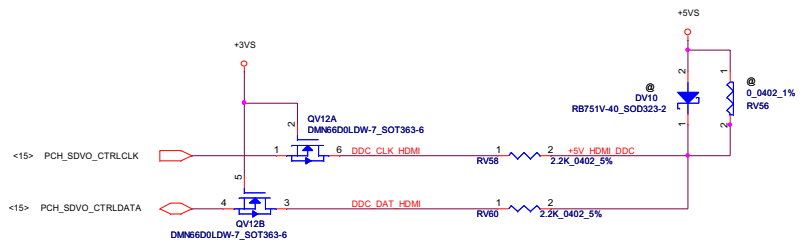


TMDS_TXCN	@ CV358	1	2	100P_0402_50V8J
TMDS_TXCP	@ CV360	1	2	100P_0402_50V8J
TMDS_TXIN	@ CV362	1	2	100P_0402_50V8J
TMDS_TXIP	@ CV363	1	2	100P_0402_50V8J
TMDS_TXIN	@ CV359	1	2	100P_0402_50V8J
TMDS_TXIP	@ CV357	1	2	100P_0402_50V8J
TMDS_TX2N	@ CV361	1	2	100P_0402_50V8J
TMDS_TX2P	@ CV364	1	2	100P_0402_50V8J

20111024 EMI ADD

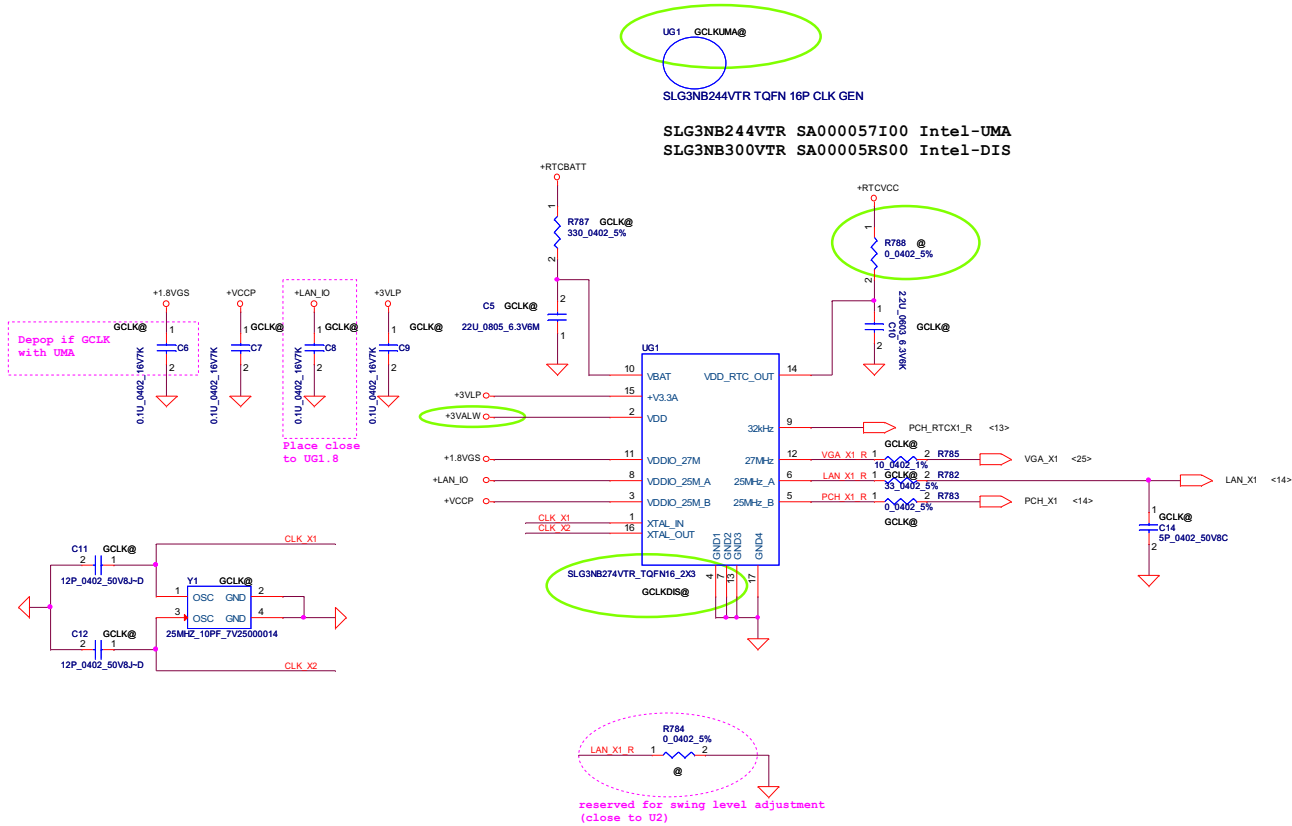
TMDS_L_TXCN	CV349	1	2	3.3P_0402_50V8C-D
TMDS_L_TXCP	CV350	1	2	3.3P_0402_50V8C-D
TMDS_L_TXIN	CV351	1	2	3.3P_0402_50V8C-D
TMDS_L_TXIP	CV352	1	2	3.3P_0402_50V8C-D
TMDS_L_TXIN	CV353	1	2	3.3P_0402_50V8C-D
TMDS_L_TXIP	CV354	1	2	3.3P_0402_50V8C-D
TMDS_L_TX2N	CV355	1	2	3.3P_0402_50V8C-D
TMDS_L_TX2P	CV356	1	2	3.3P_0402_50V8C-D

20110805 EMI ADD



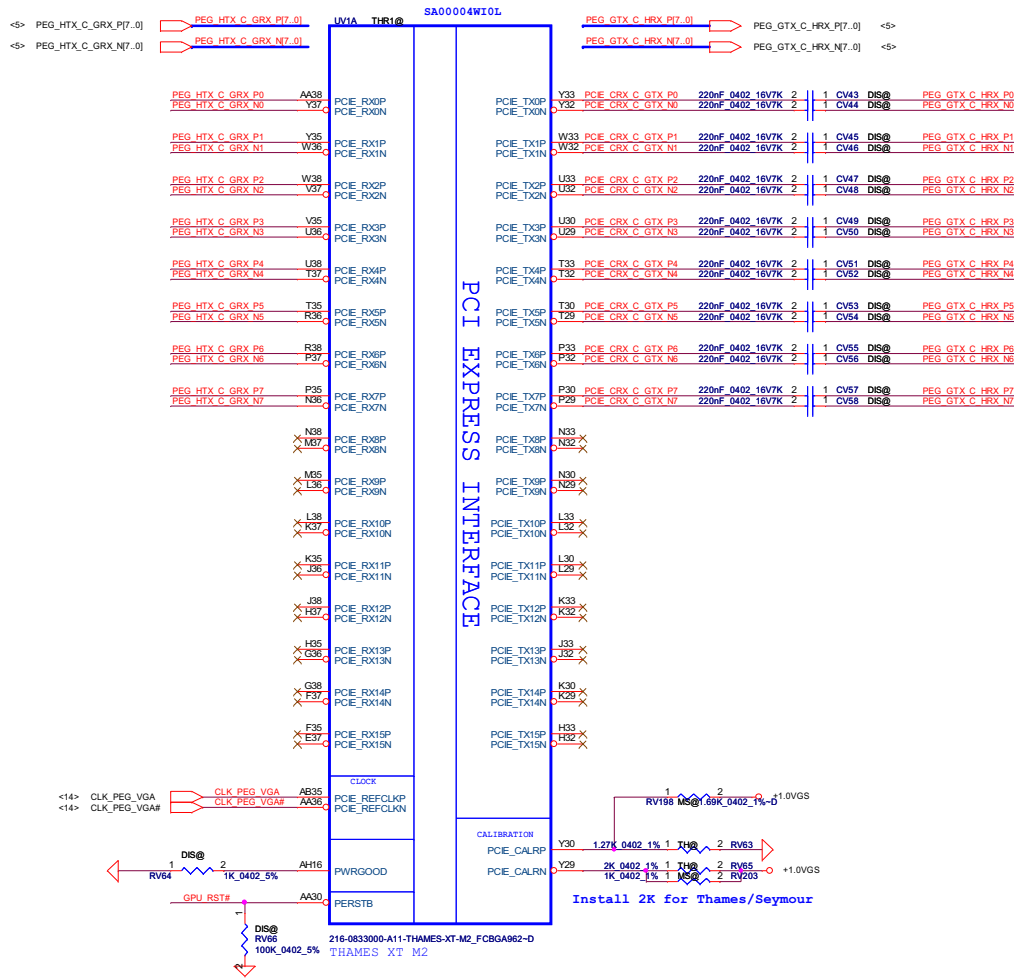
46@	ROYALTY HDMI W/LOGO
Part Number	Description
RO00000028M	HDMI M/Logo:RO00000028M

Security Classification	Compal Secret Data		Title	HDMI	
Issued Date	2012/09/25	Deciphered Date	2013/09/30	Size	Document Number
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			Date:	Tuesday, September 25, 2012	Sheet 22 of 57

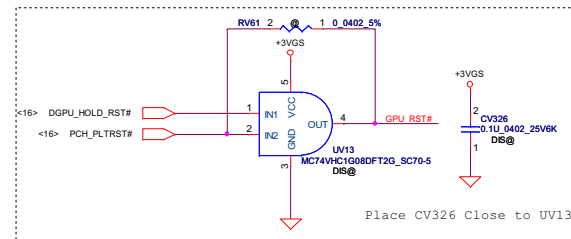
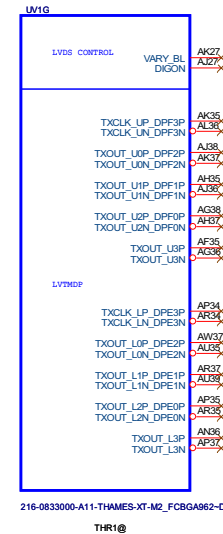


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GFX PCIE LANE REVERSAL



LVDS Interface



SA00004W11L

216-0833000-A11-THAMES-XT-M2_FCBGA962-D



SA00005X10L

MARS-PRO_FCBGA962-D

MARS Pro



SA00005X10L

MARS-PRO_FCBGA962-D

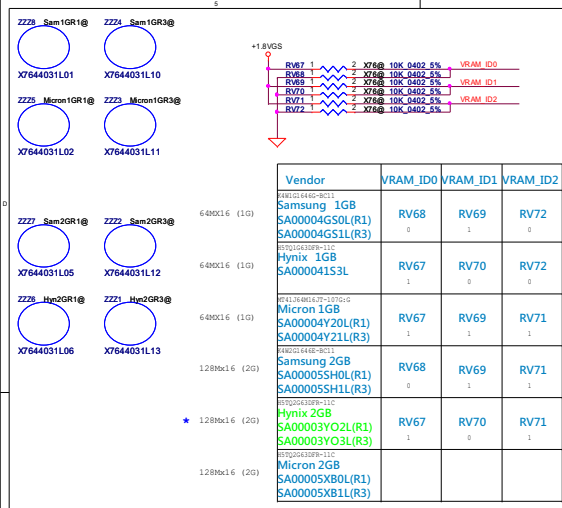
MARS Pro



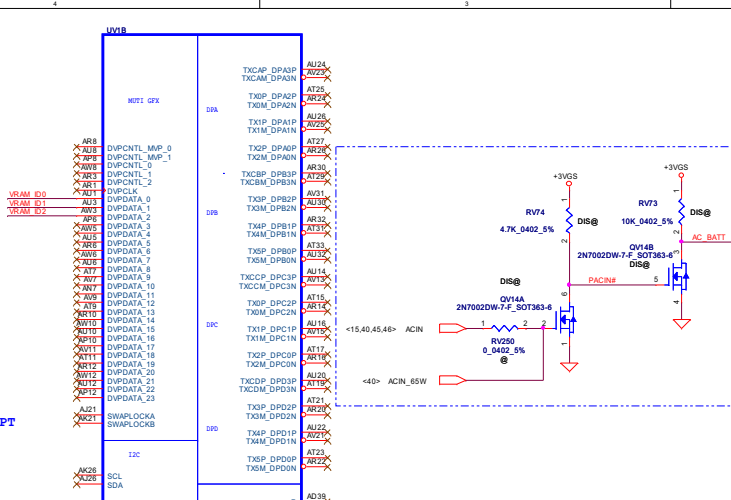
Chelsea Pro

Chelsea Pro

Security Classification	Compal Secret Data		Title	
Issued Date	2012/09/25	Deciphered Date	2013/09/30	ATI ThamesXT M2 PCIE/LVDS
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Vendor	VRAM_ID0	VRAM_ID1	VRAM_ID2
Samsung 1GB			
SA00004G50L(R1)	RV68	RV69	RV72
SA00004G51L(R3)	0	1	0
Hynix 1GB			
SA00004153L	RV67	RV70	RV72
0	0	0	0
Micron 1GB			
SA00004Y20L(R1)	RV67	RV69	RV71
SA00004Y21L(R3)	1	1	1
Samsung 2GB			
SA000055H0L(R1)	RV68	RV69	RV71
SA000055H1L(R3)	0	1	1
Hynix 2GB			
SA00003Y02L(R1)	RV67	RV70	RV71
SA00003Y03L(R3)	1	0	1
Micron 2GB			
SA00005X80L(R1)	RV67	RV70	RV71
SA00005X81L(R3)	1	0	1



CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

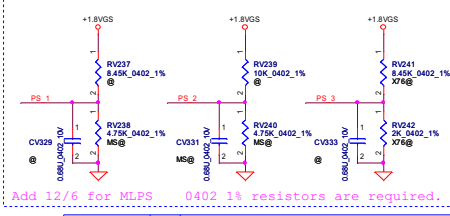
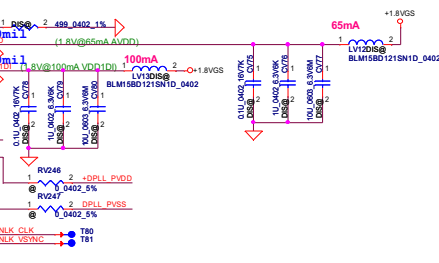
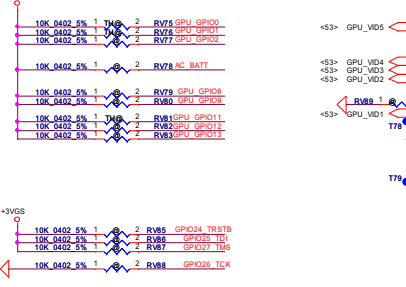
RECOMMENDED SETTINGS
 0= DO NOT INSTALL RESISTOR
 1= INSTALL 10K RESISTOR
 X= DESIGN DEPENDANT
 NA= NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
TX_PWR5_ENB	GPI00	PCI FULL TX OUTPUT SWING 0: 50% swing 1: Full swing	X
TX_DEEMPH_EN	GPI01	PCI TRANSMITTER DE-EMPHASIS 0: disable 1: enable	X
RSVD	GPI02	Advertises PCIe speed when compliance test 0: 2.5G/s 1: 5G/s	0
RSVD	GPI08	RESERVED	0
BIF_VGA_DIS	GPI09	VGA ENABLED	0
RSVD	GPI021	RESERVED	0
BIOS_ROM_EN	GPI0_22_ROMCSB	ENABLE EXTERNAL BIOS ROM 0: disable 1: enable	X
ROMDCFG(2:0)	GPI0(13:1)	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	XXX
WP_DEVICE_STRAP_ENA	V2SYNC	IGNORE WP DEVICE STRAPS	0
RSVD	H2SYNC	RESERVED	0
RSVD	GENERIC	RESERVED	0
AUD[1]	HSYNC	AUD[1][AUD0] 0: No audio function 1: Audio for DisplayPort and HDMI if dongle is detected	11
AUD[0]	VSYNC	0: Audio for DisplayPort only 1: Audio for both DisplayPort and HDMI	0

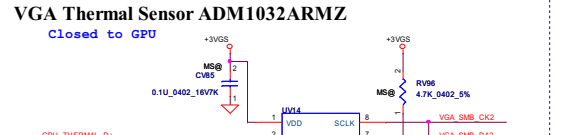
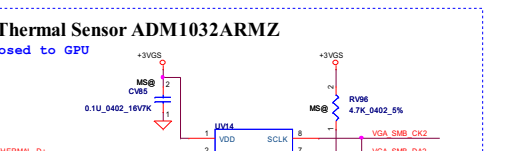
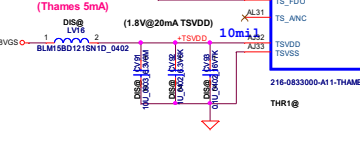
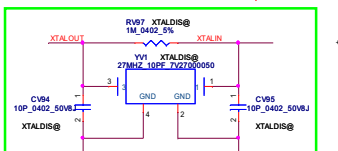
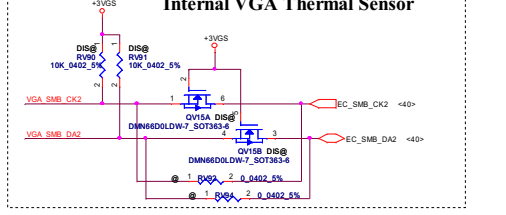
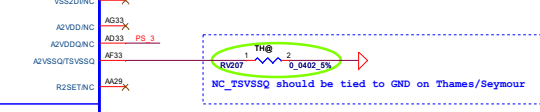
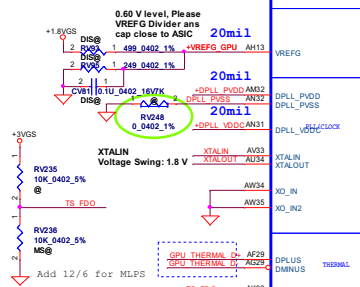
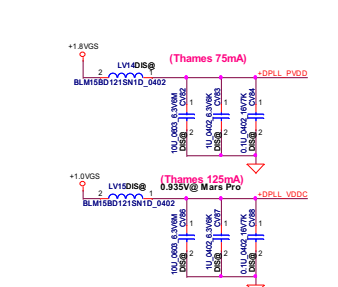
AMD RESERVED CONFIGURATION STRAPS
 ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOS ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET

Mars Pro MLPS	RV241	RV242	Bits (3:1)
Hynix	NC	4.75k	000
Samsung	8.45k	2k	001
Micron	4.75k	NC	111

STRAPS

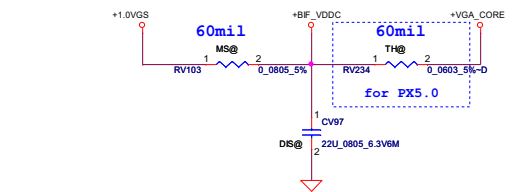
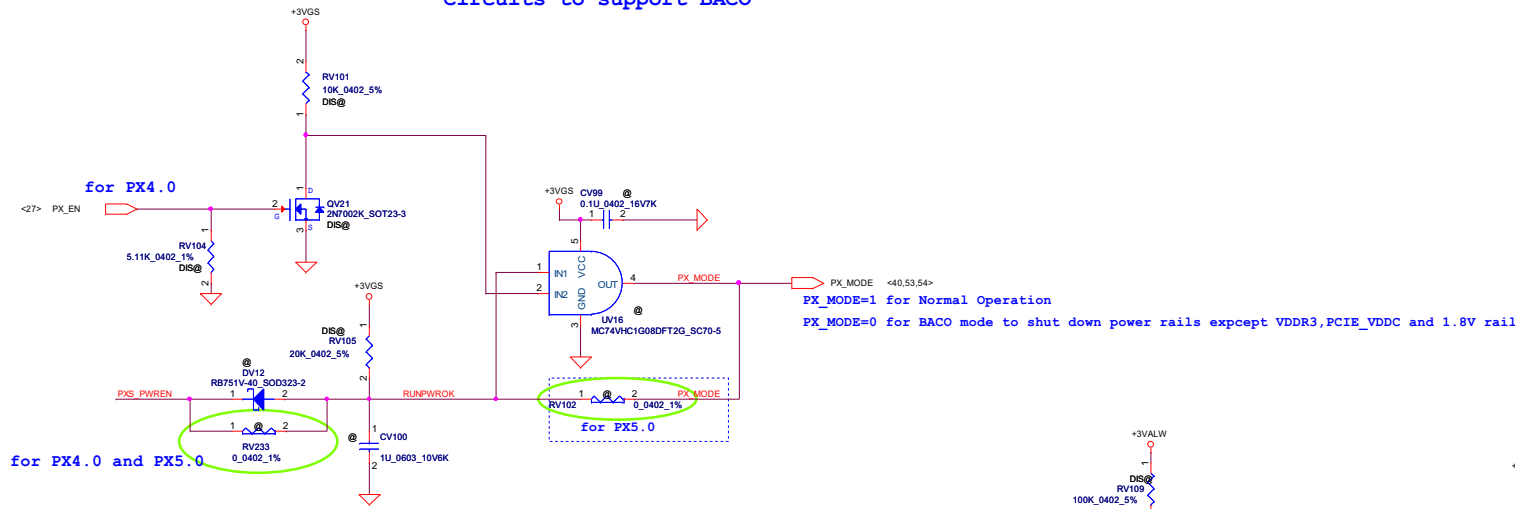


TX_PWR5_ENB	GPI00	Transmitter Power Saving Enable 0: 50% Tx output swing for mobile mode 1: Full Tx output swing (Default setting for Desktop)
TX_DEEMPH_EN	GPI01	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for desktop)

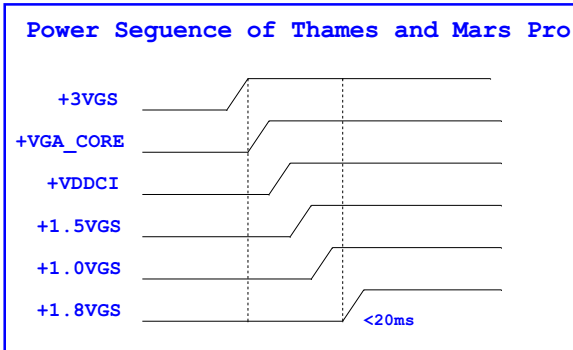


55mA@1.0V, in BACO mode

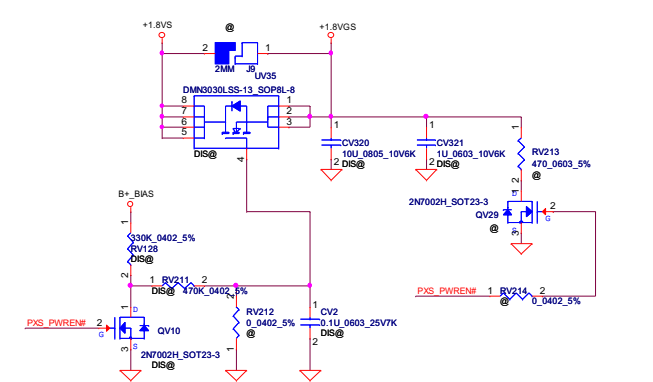
Circuits to support BACO



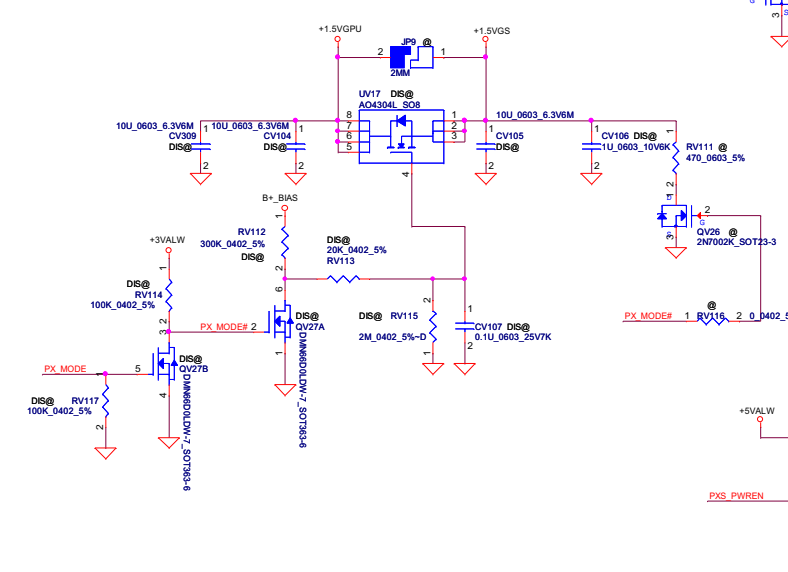
Note:
 PX4.0 +VGA_CORE,VDDCI,+1.5VGS ON
 PX4.0 +3VGS,+1.0VGS,+1.8VGS OFF
 PX5.0 +3VGS,+VGA_CORE,VDDCI,+1.5VGV,+1.0VGS,+1.8VGS OFF



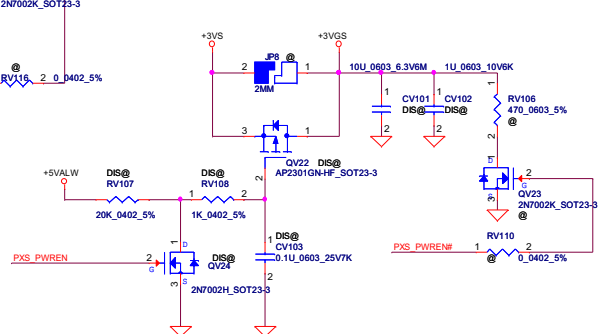
+1.8VS TO +1.8VGS



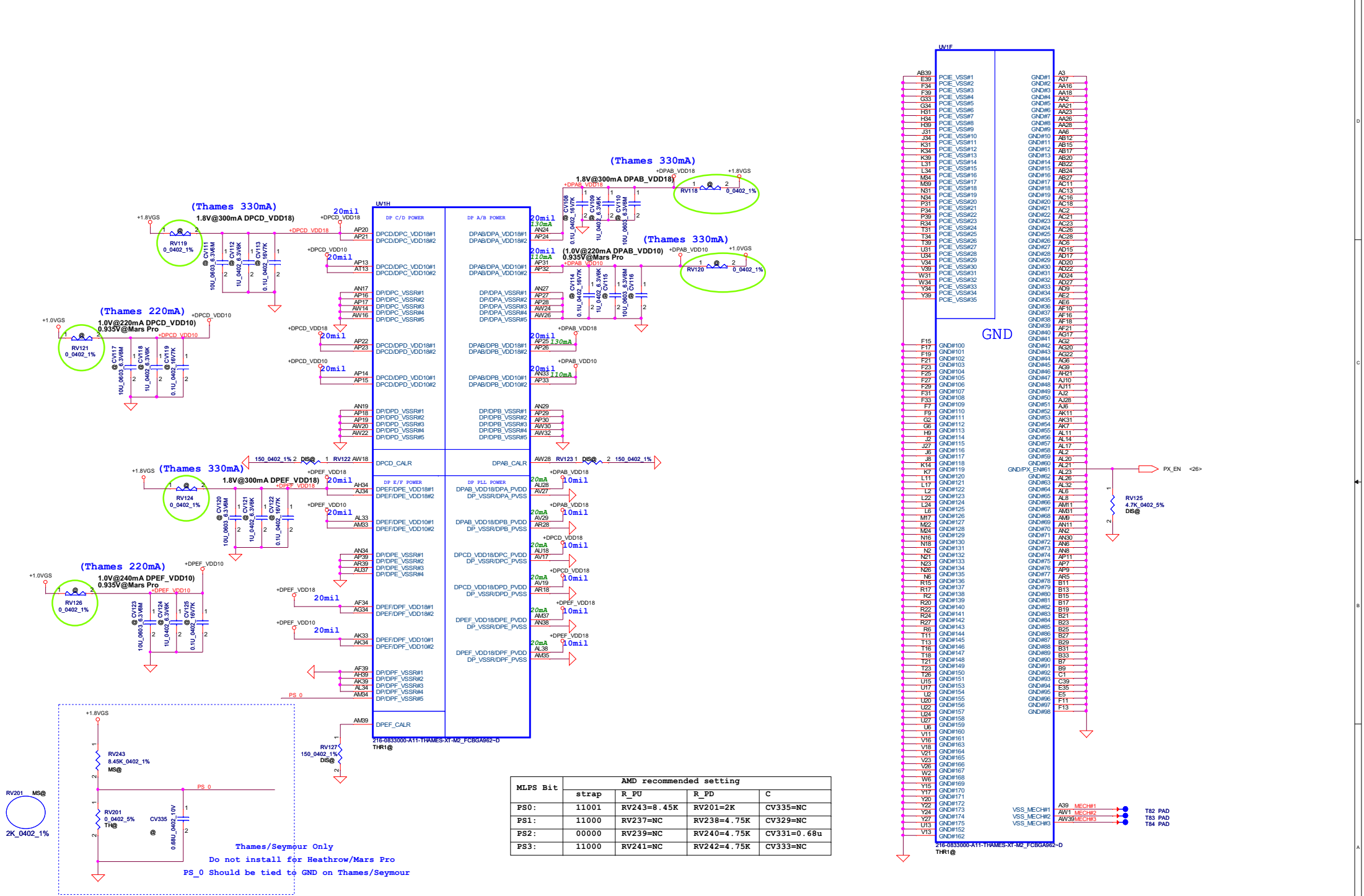
+1.5VGPU TO +1.5VGS



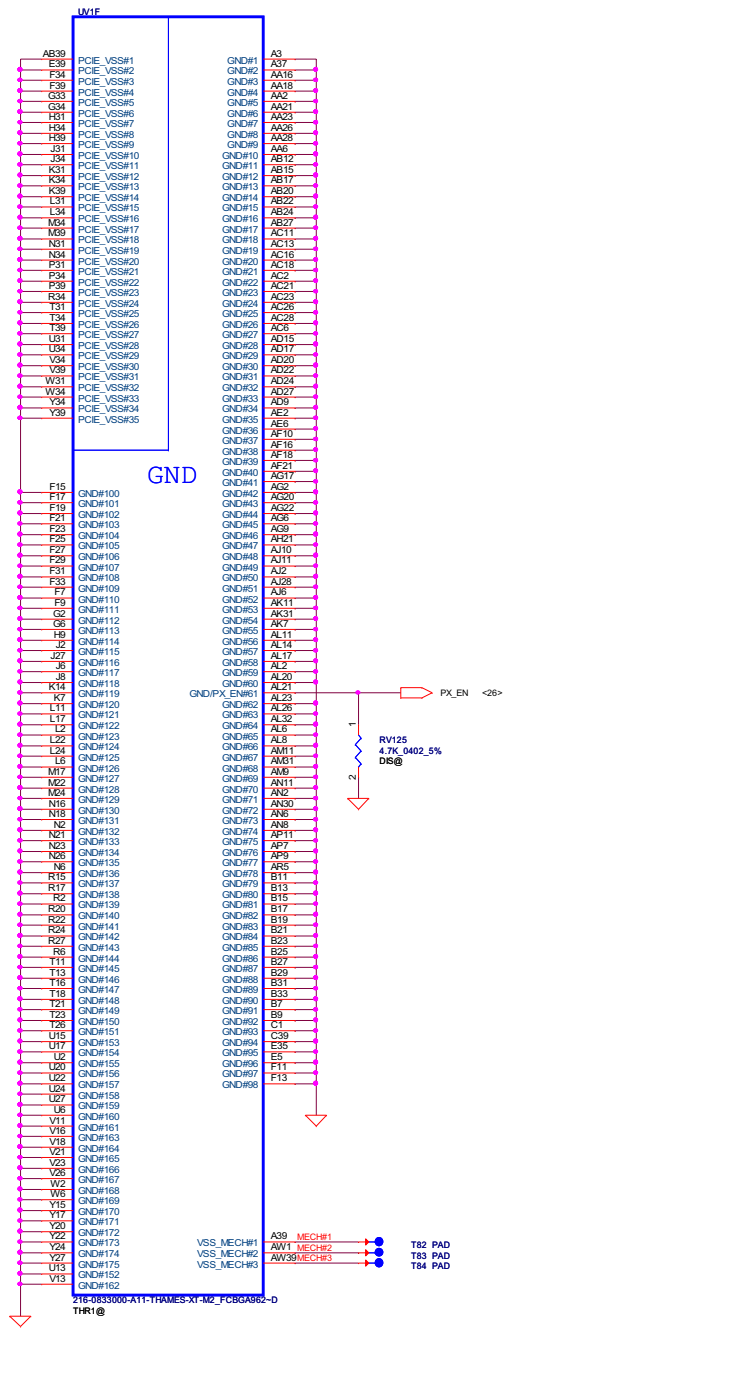
+3.3VS TO +3.3VGS

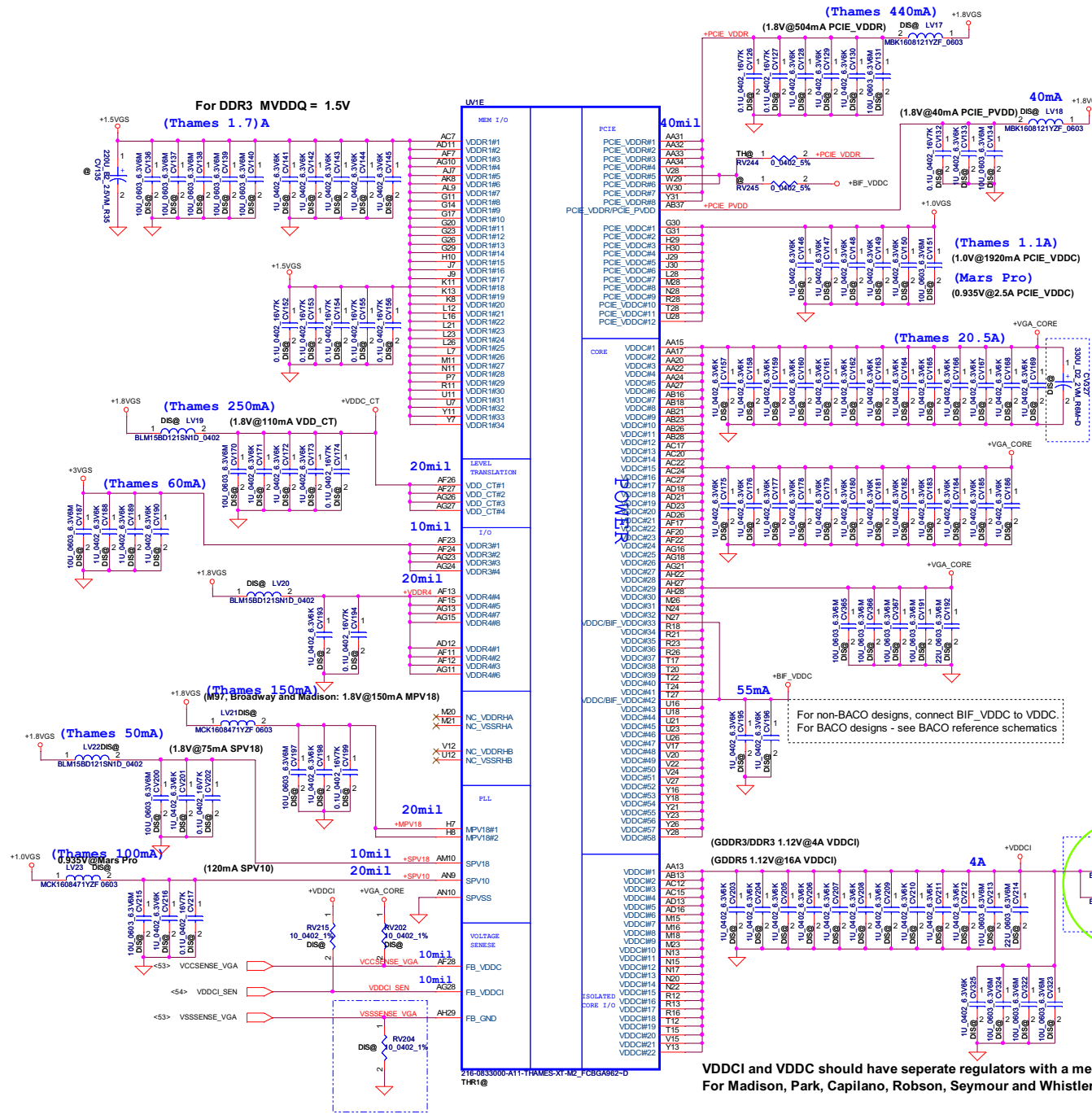


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Date: Tuesday, September 25, 2012			Sheet 26	of 57



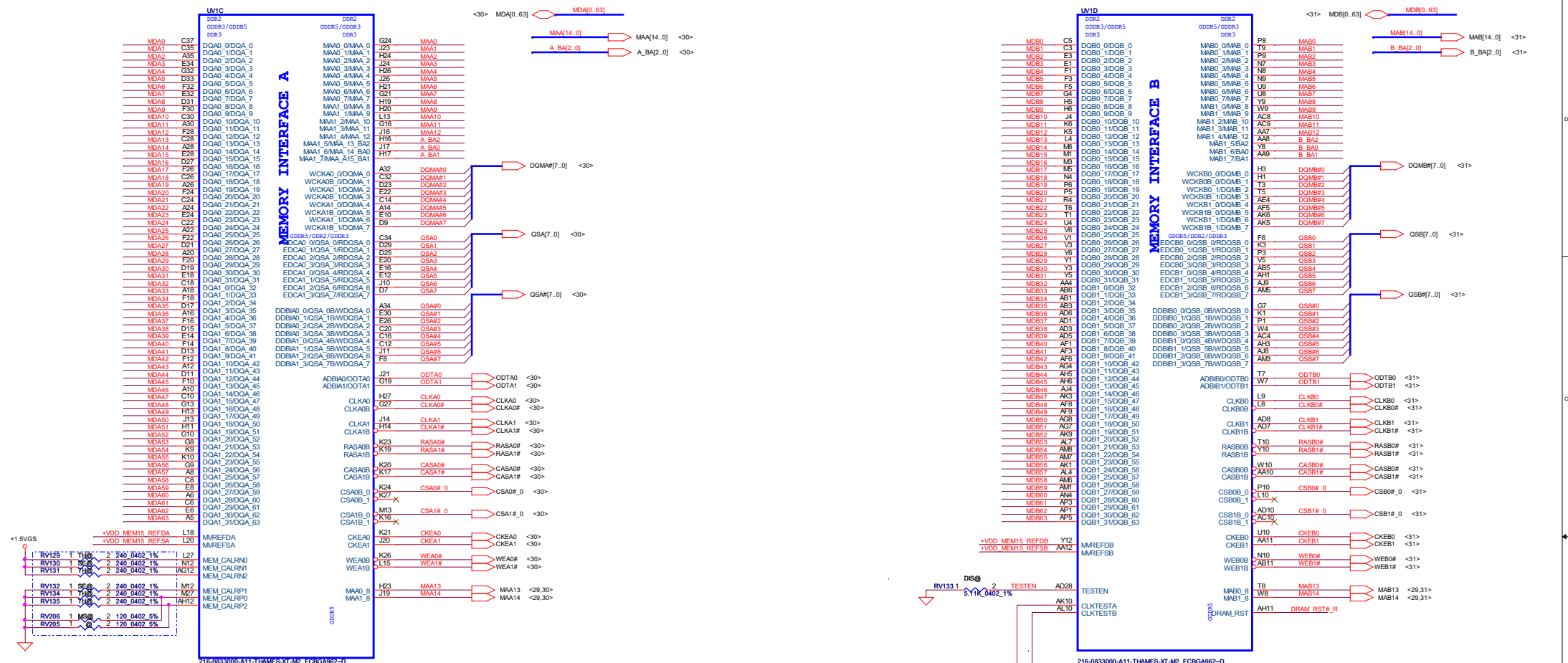
MLPS Bit	AMD recommended setting			
	strap	R_PU	R_PD	C
PS0:	11001	RV243=8.45K	RV201=2K	CV335=NC
PS1:	11000	RV237=NC	RV238=4.75K	CV329=NC
PS2:	00000	RV239=NC	RV240=4.75K	CV331=0.68u
PS3:	11000	RV241=NC	RV242=4.75K	CV333=NC





VDDCI and VDDC should have separate regulators with a merge option on PCB
 For Madison, Park, Capilano, Robson, Seymour and Whistler, VDDCI and VDDC can share one common regulator

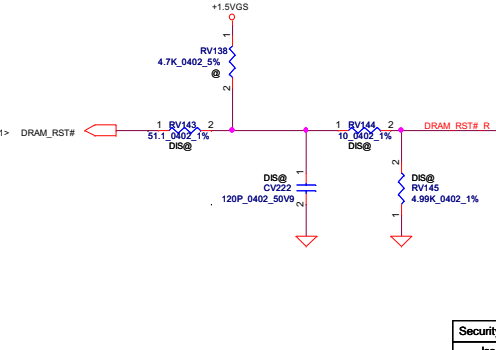
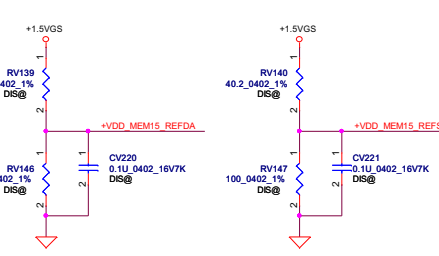
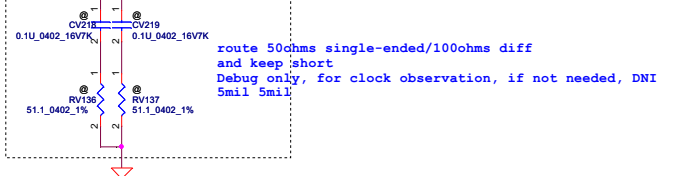
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2012/09/25	Deciphered Date	2013/09/30	Title	ATI ThamesXT M2 Power
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Size	Document Number	Rev	1.0	LA-9102P	
Date:	Tuesday, September 25, 2012	ISheet	28	of 57	



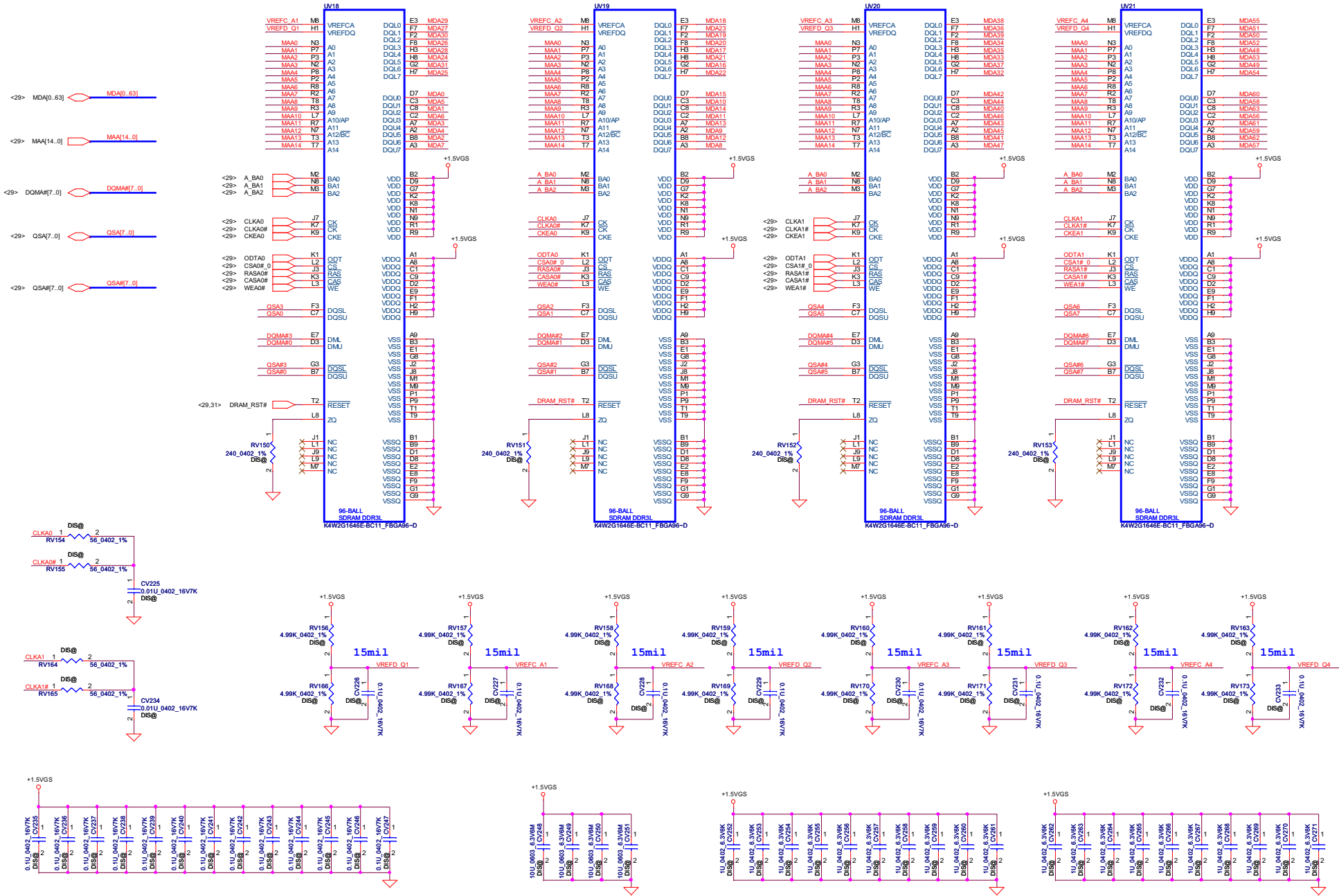
Co-lay Thames/Seymour/Mars Pro

	Thames M2	Seymour M2	Mars Pro
RV129	TH@	@	@
RV130	@	SE@	@
RV131	TH@	@	@
RV132	@	SE@	@
RV134	TH@	@	@
RV135	TH@	@	@
RV206	@	@	MS@
RV205	@	@	@

This basic topology should be used for DRAM RST for DDR3/GDDR5. These Capacitors and Resistor values are an example only. The Series R and I Cap values will depend on the DRAM load and will have to be calculated for different Memory, DRAM load and board to pass Reset Signal Spec. Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except Rser2

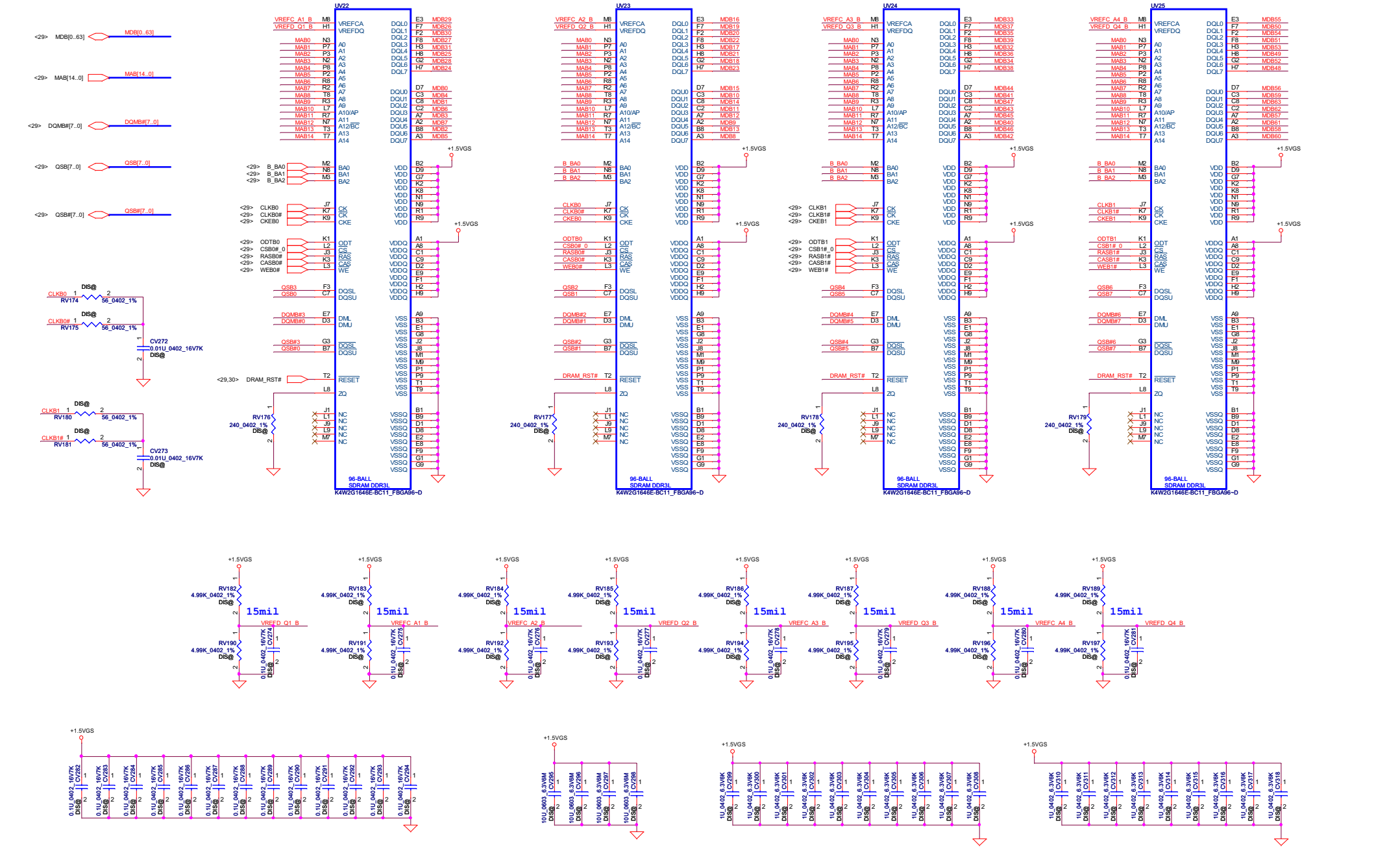


CHANNEL A: 256MB/512MB DDR3

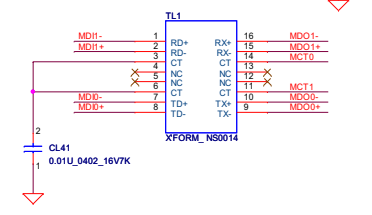
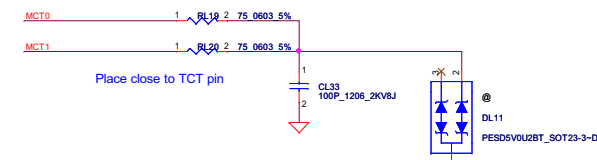
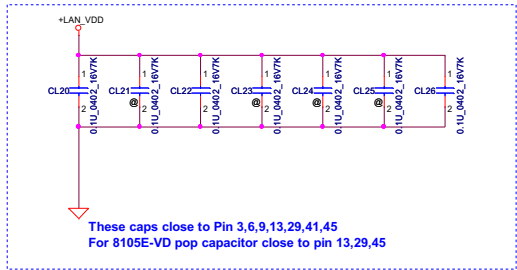
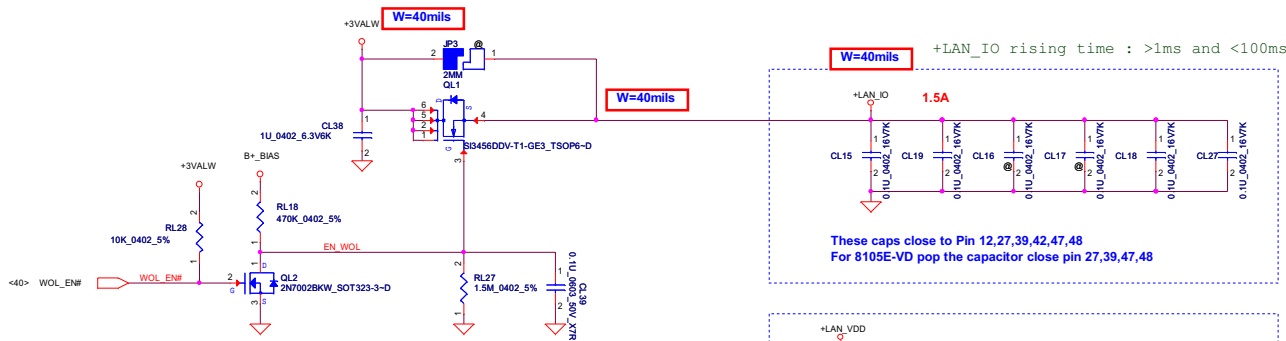


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Date:	Tuesday, September 25, 2012	ISheet	30	of 57

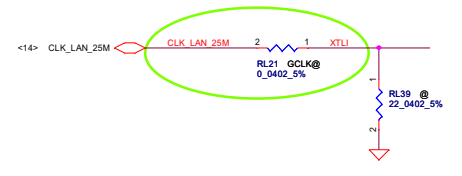
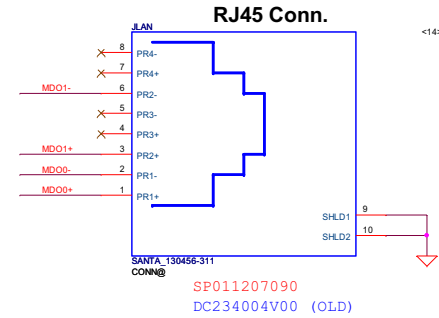
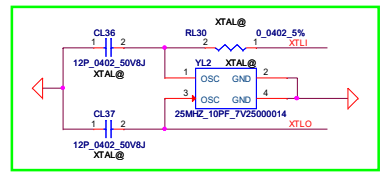
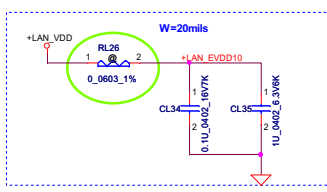
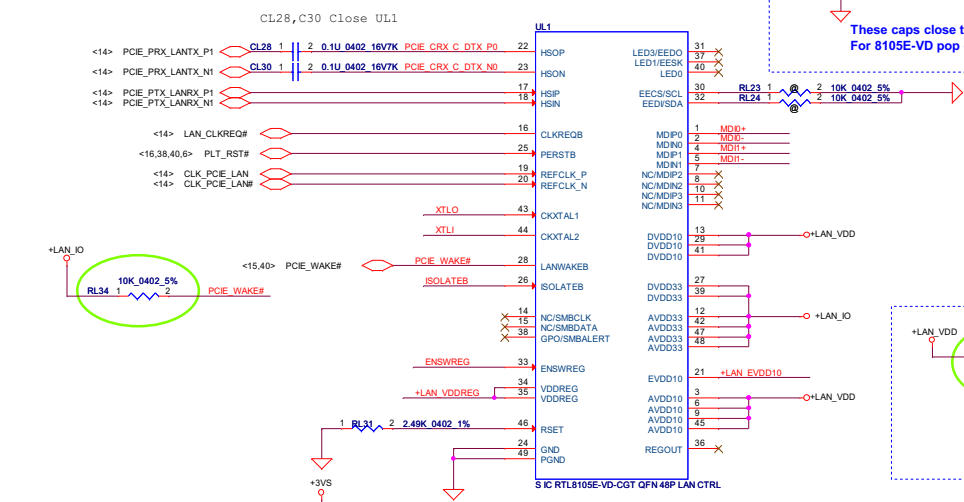
CHANNEL B: 256MB/512MB DDR3



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				Date:	Tuesday, September 25, 2012
				ISheet	31 of 57

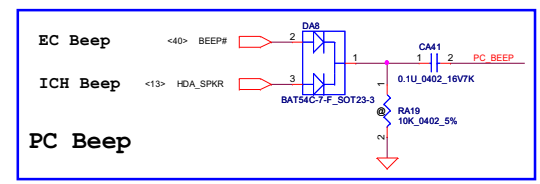
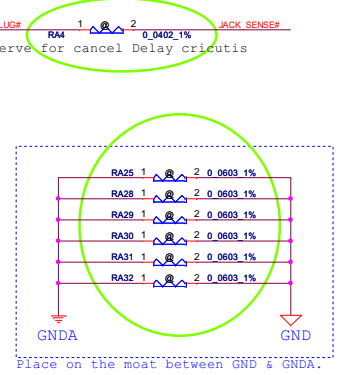
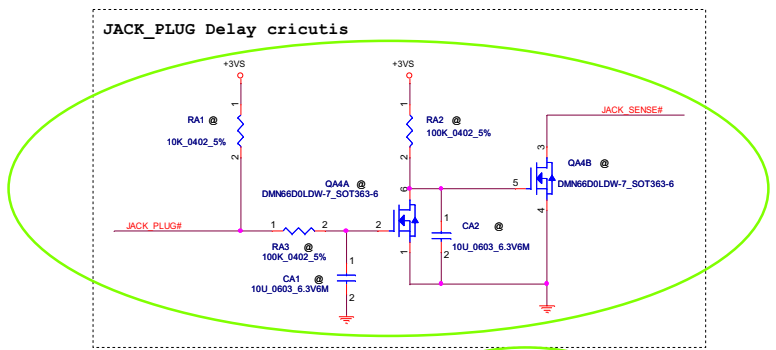
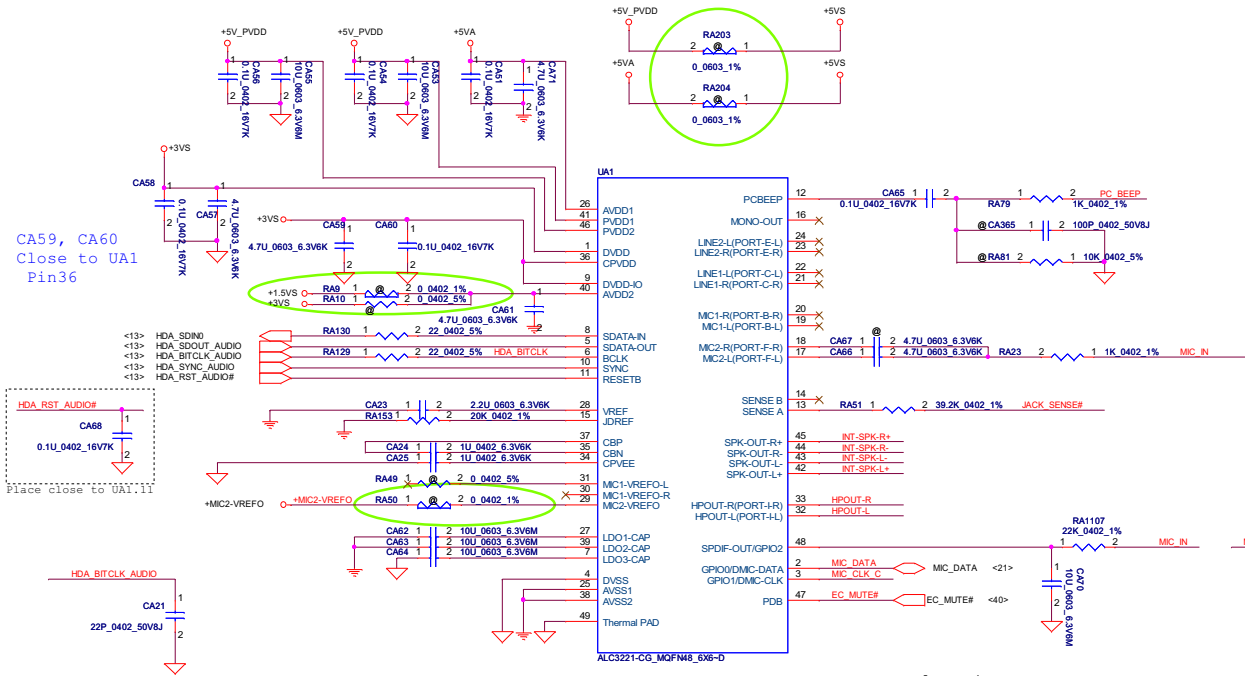


DL11 as close as possible to C27 and C32

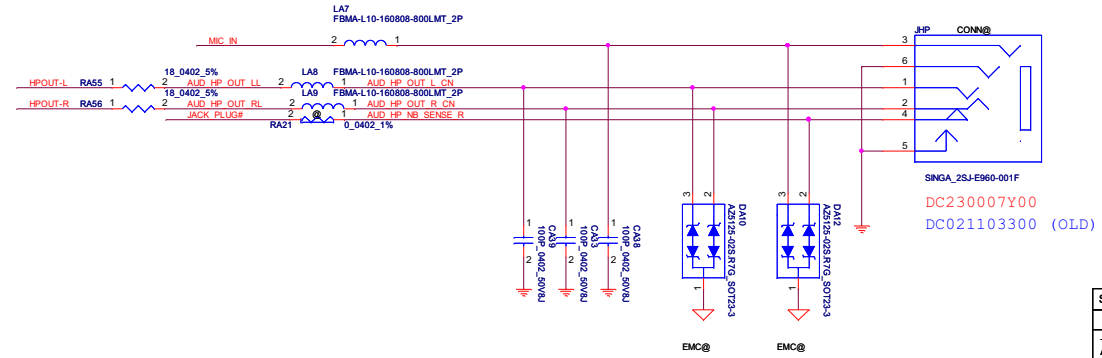


3.3V : Enable switching regulator
 0V : Disable switching regulator
 10/100 : 100@ (LDO mode used)

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				LA-9102P	1.0
			Date:	Tuesday, September 25, 2012	Sheet 32 of 57

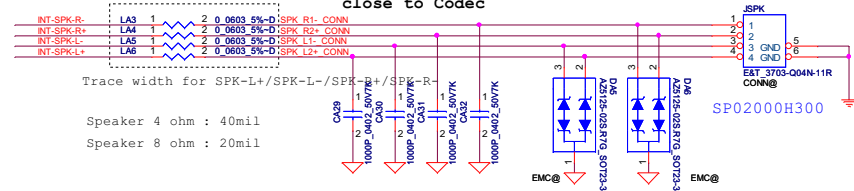


iPhone type Combo Jack

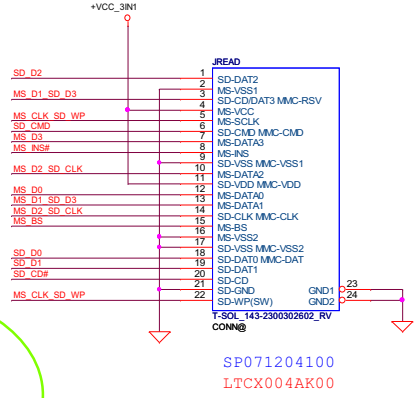
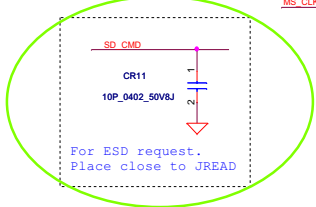
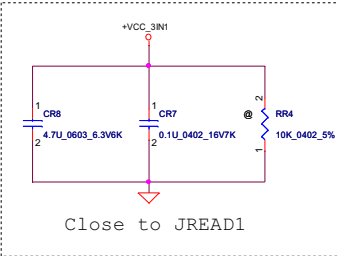
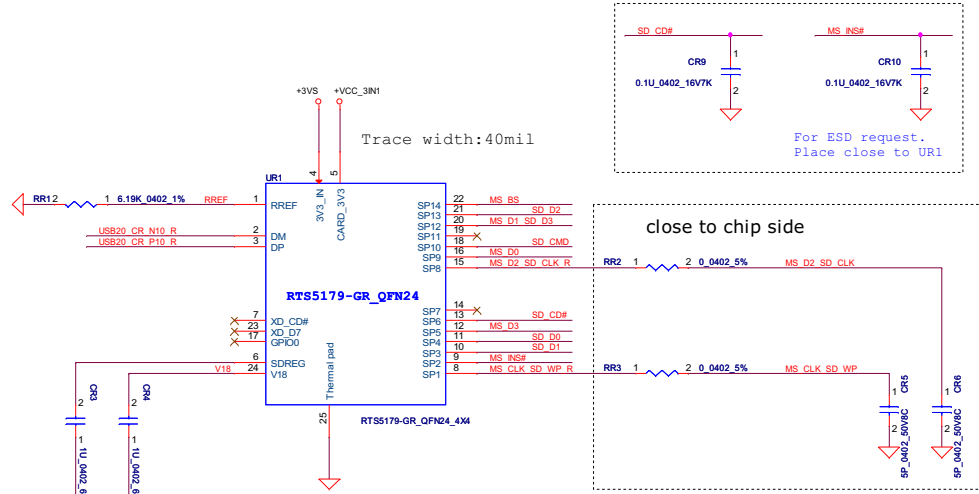
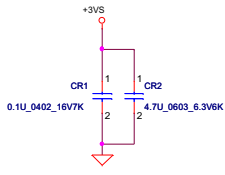
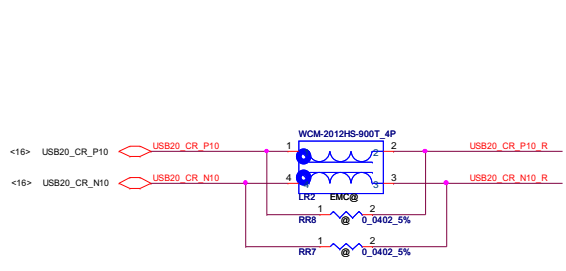


Close to UA1
Pin11,13,14,16

close to Codec



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				LA-9102P	Rev 1.0
				Date:	Tuesday, September 25, 2012 Sheet 33 of 57

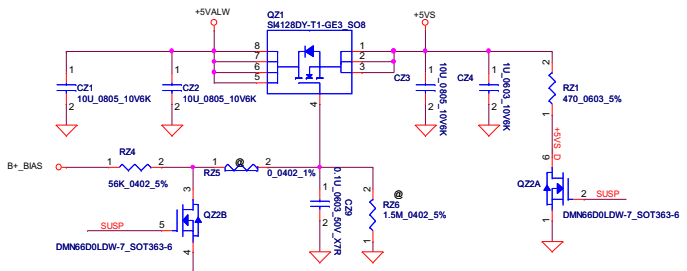


拉MS_D2_SD_CLK到Conn pin 13 SD_CLK
再打Via拉到pin 10 MS_D2

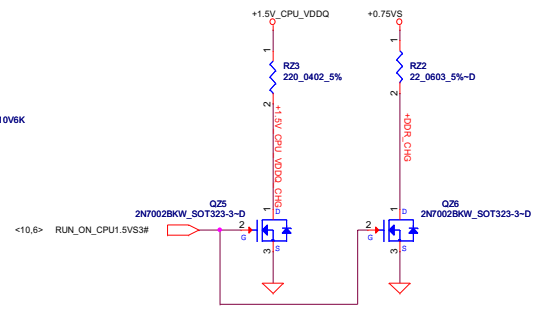
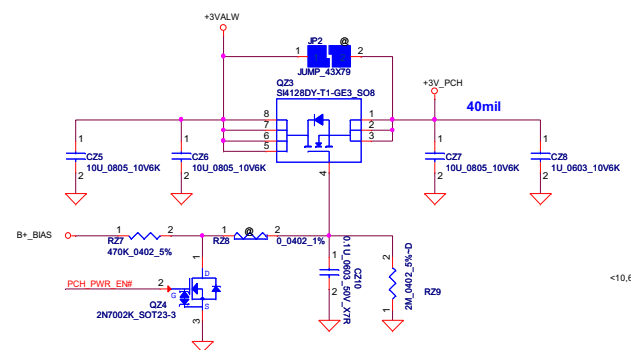
拉MS_CLK_SD_WP到Conn pin 5 MS_CLK
再打Via拉到pin 20 SD_W

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				Rev 1.0

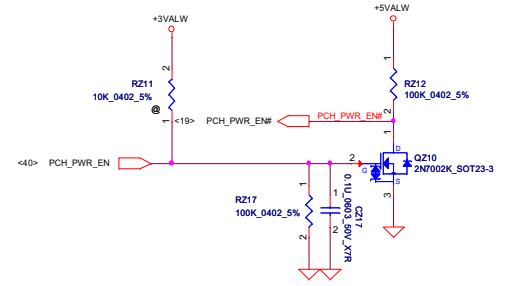
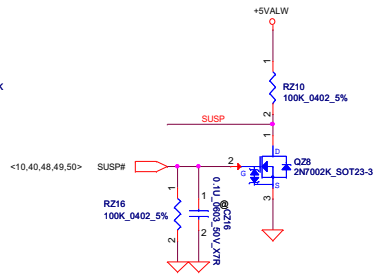
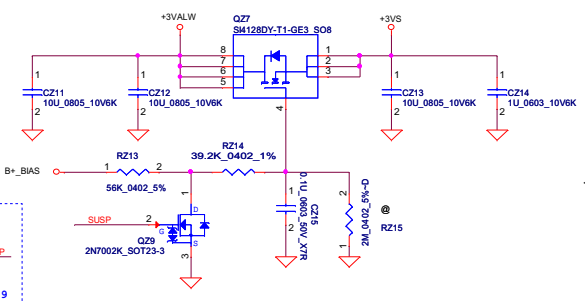
+5VALW to +5VS



+3VALW to +3V_PCH

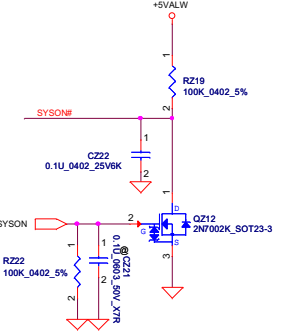
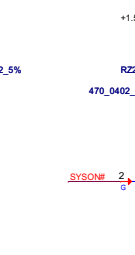
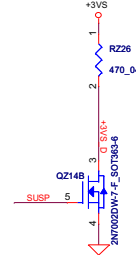
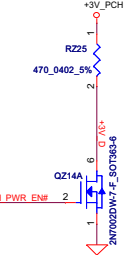
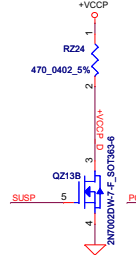
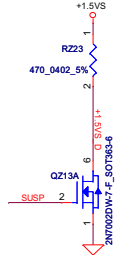
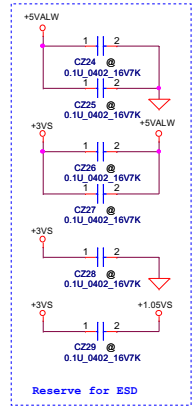
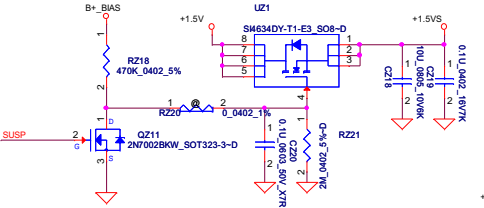


+3VALW to +3VS

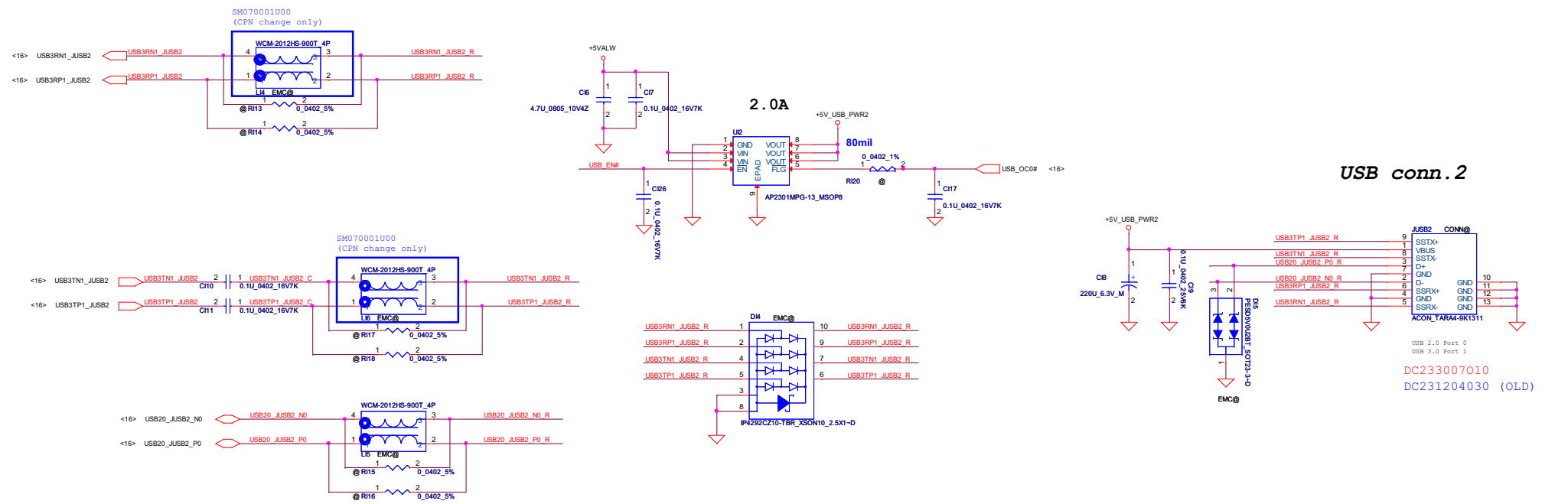
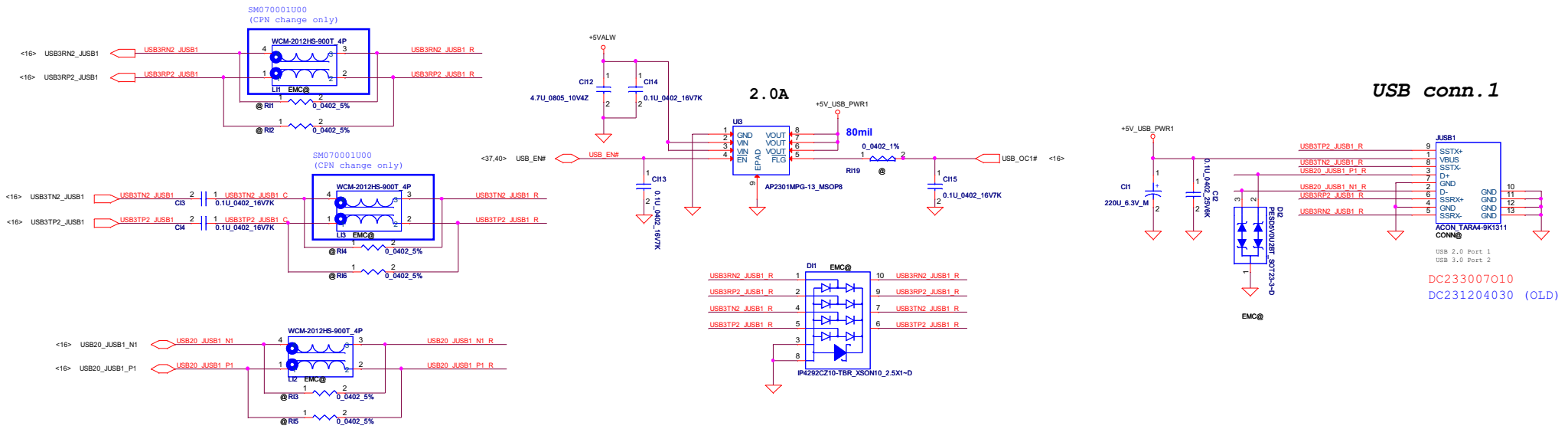


Reserve for ESD
CZ33
0.1U_0402_16V7K
Please close to QZ9

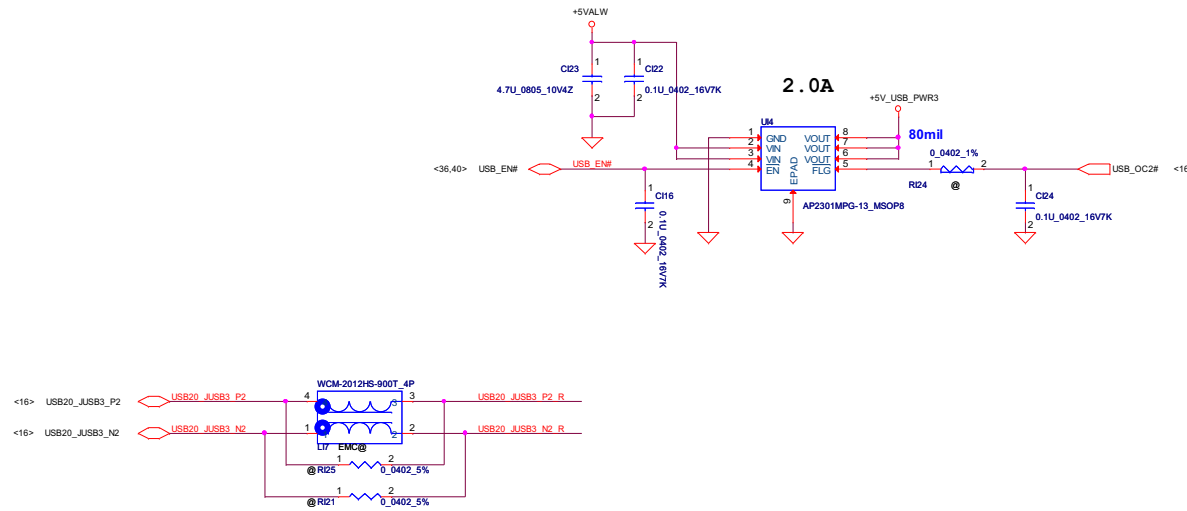
+1.5V To +1.5VS



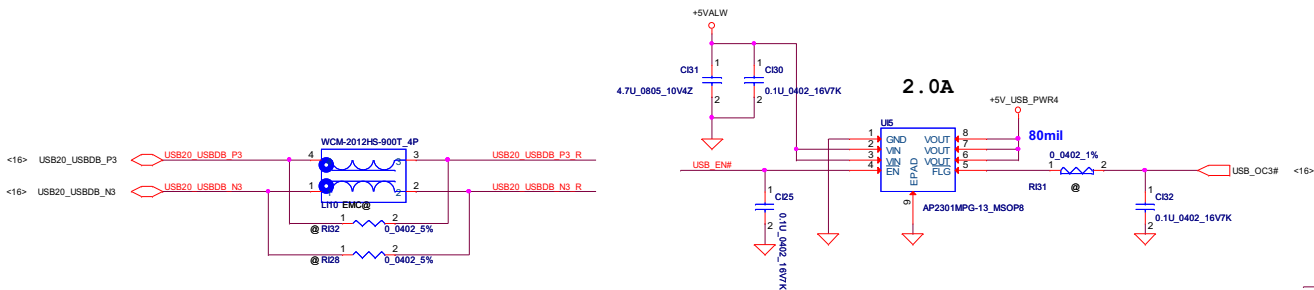
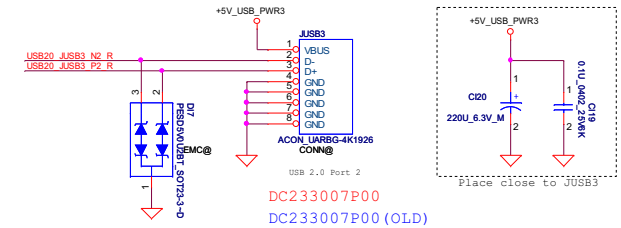
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2012/09/25		2013/09/30		1.0	
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Date: Tuesday, September 25, 2012				Sheet 35 of 57	



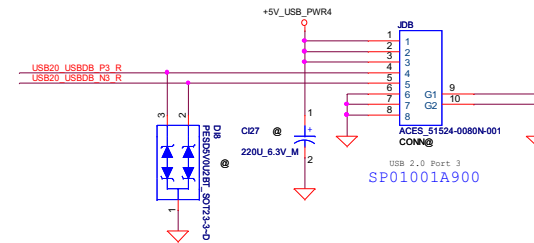
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				LA-9102P	Rev 1.0
				Date:	Wednesday, September 26, 2012 Sheet 36 of 57



USB conn. 3

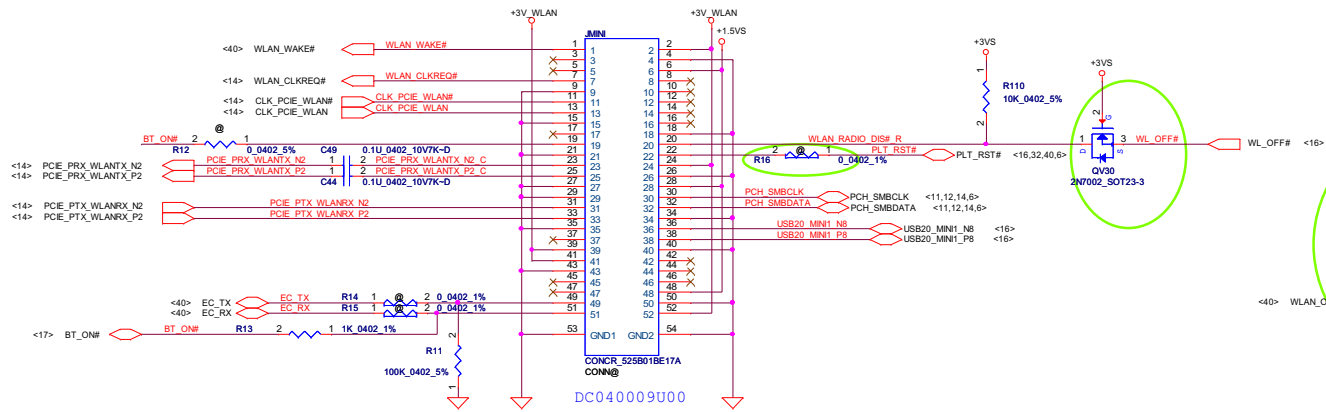


USB conn. 4

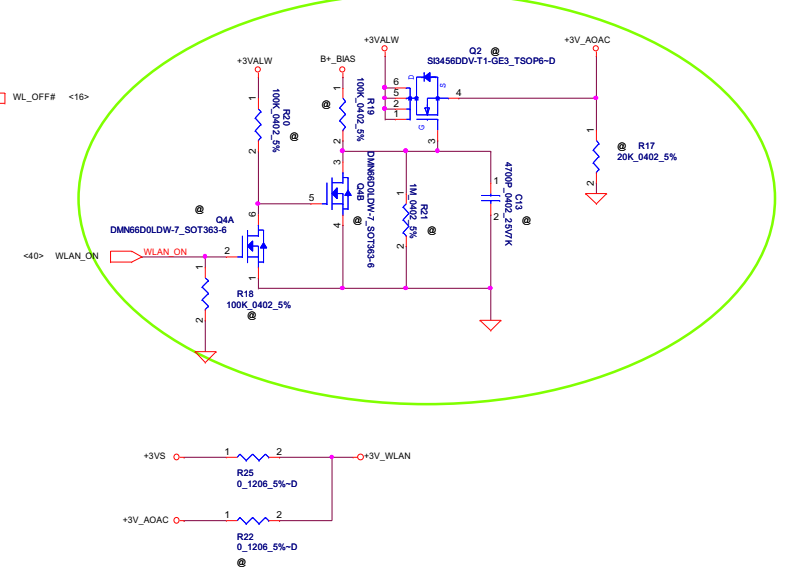


Security Classification	Compal Secret Data		Title	
Issued Date	2012/09/25	Deciphered Date	2013/09/30	MB to USB2.0 DB
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Date:	Tuesday, September 25, 2012	Sheet	37	of 57

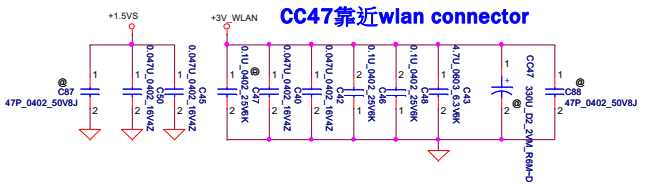
Mini WLAN/WIMAX H=6.7



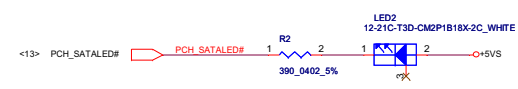
Power Control for Mini Card



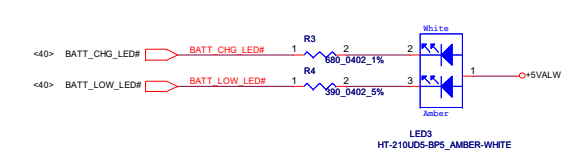
CC47靠近wlan connector



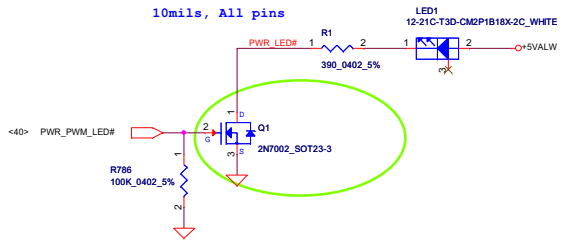
HDD LED



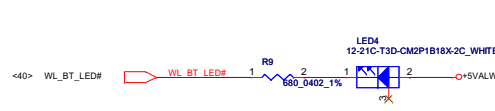
Battery LED



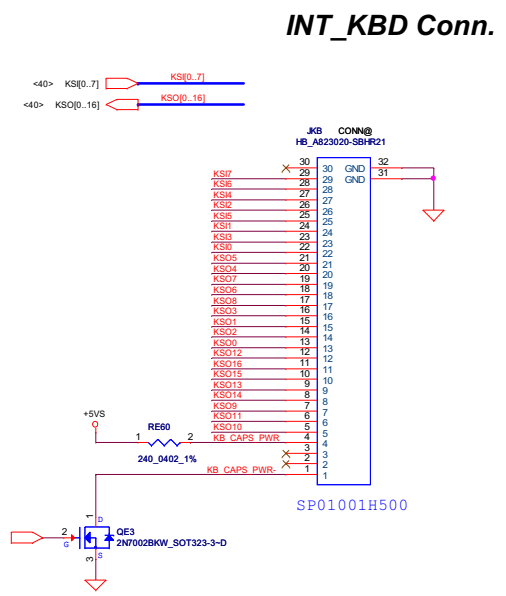
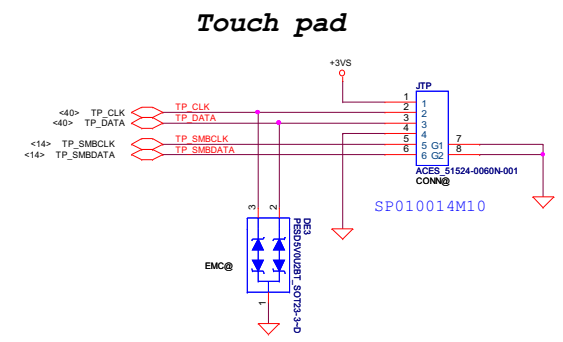
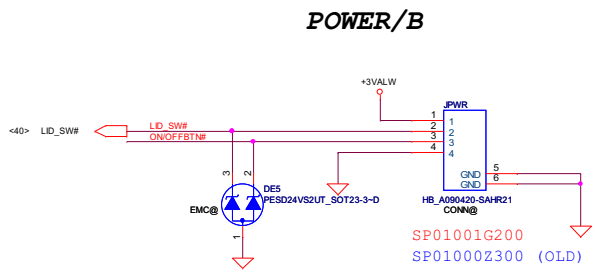
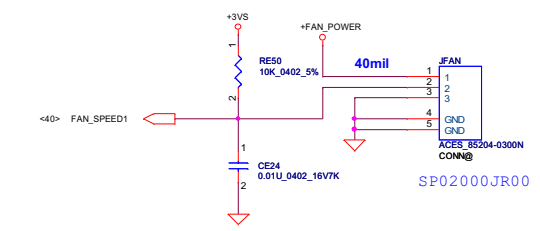
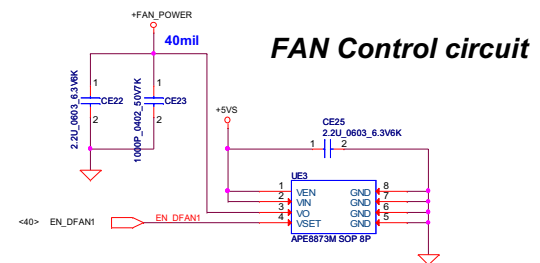
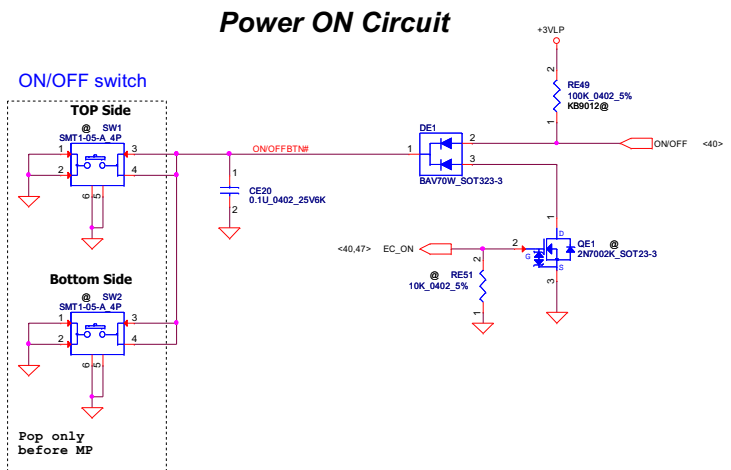
Power LED



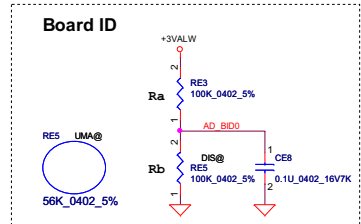
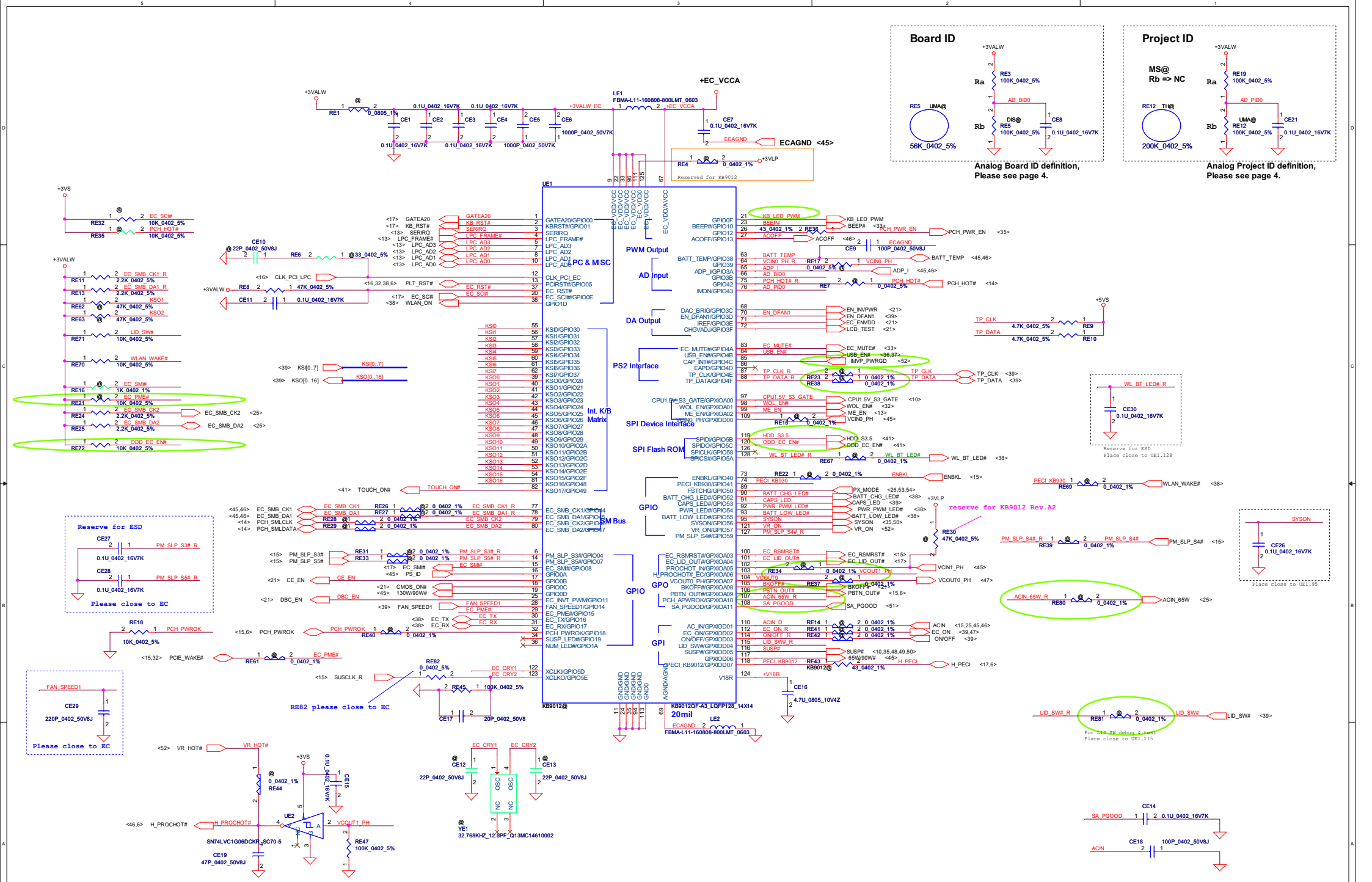
Wireless LED



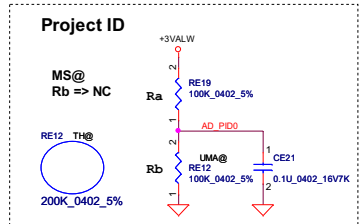
Security Classification	Compal Secret Data		Title	
Issued Date	2012/09/25	Deciphered Date	2013/09/30	Mini Card/LED
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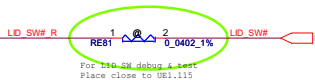
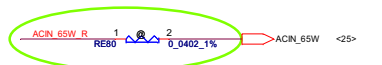
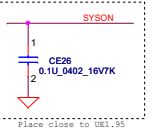
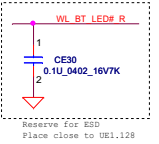
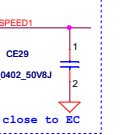
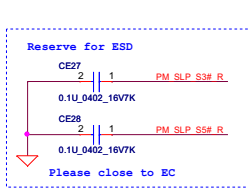
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Issued Date	2012/09/25	Deciphered Date	2013/09/30	Compal Electronics, Inc.
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Analog Board ID definition, Please see page 4.



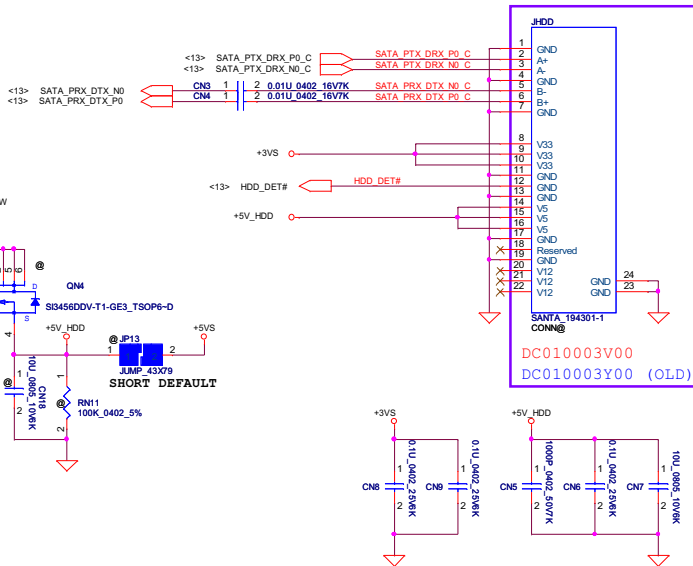
Analog Project ID definition, Please see page 4.



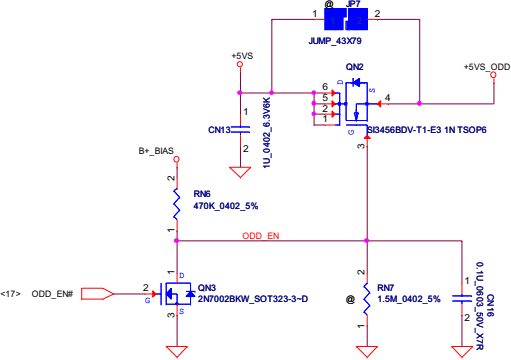
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Issued Date	2012/09/25	Deciphered Date	2013/09/30	Compal Electronics, Inc.	
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Date:				Tuesday, September 25, 2012	Sheet
				40	of 57

SATA HDD Conn.

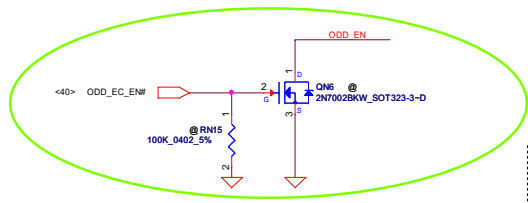
+5V_HDD Source



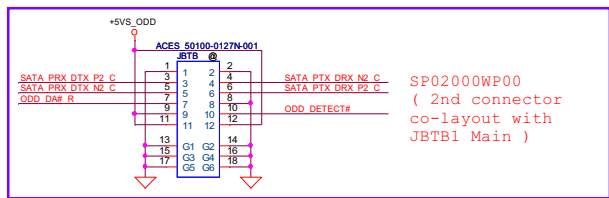
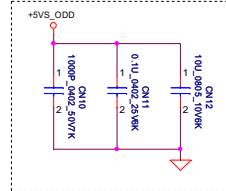
ODD Power Control



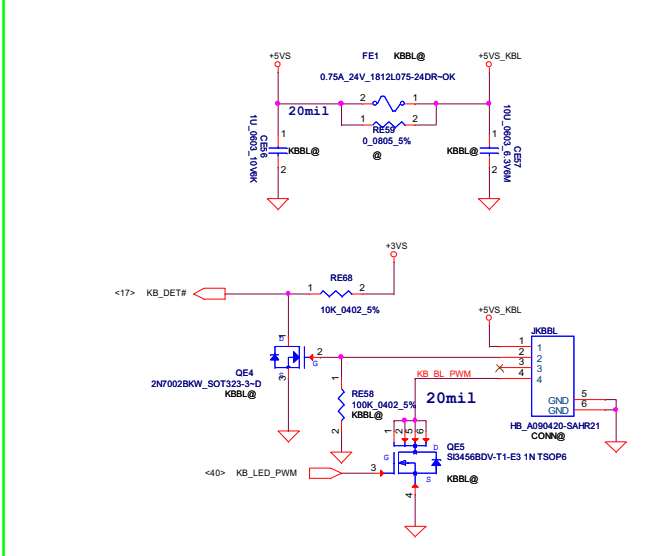
ODD BTB Conn.



Place near JBTB1 CONN.

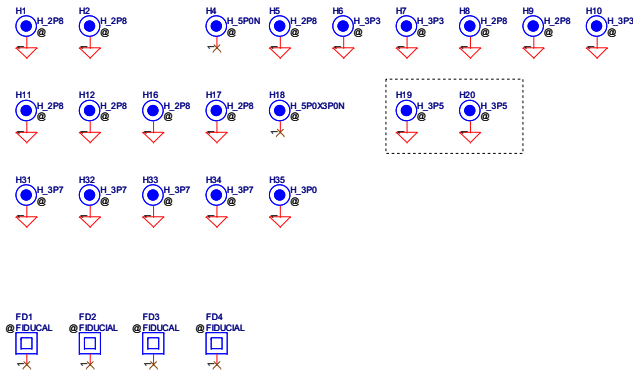


* Key Board Back Light



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Issued Date	2012/09/25	Deciphered Date	2013/09/30	HBV_ODD
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				Document Number
				LA-9102P
				Rev
				1.0
				Date: Tuesday, September 25, 2012
				Sheet 41 of 57

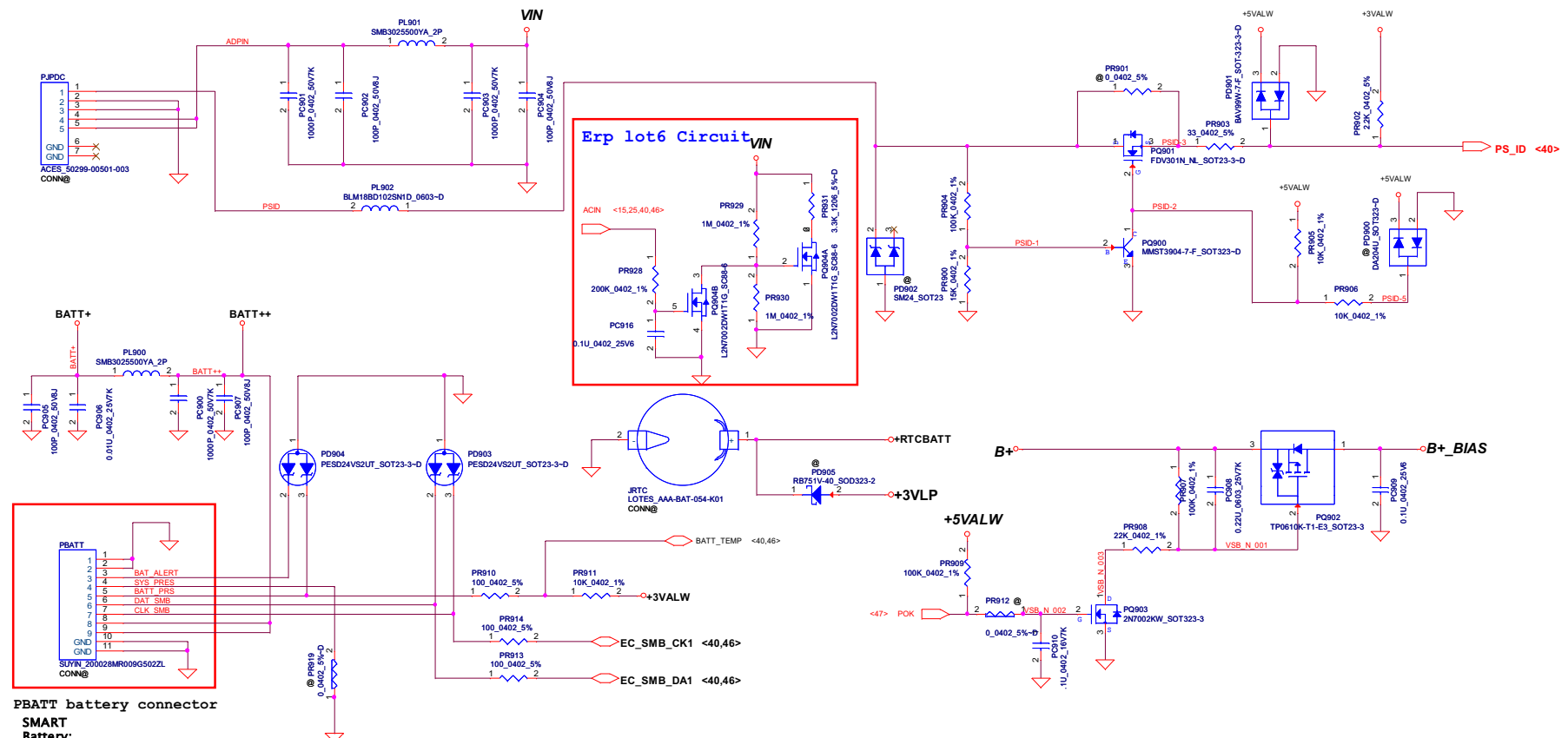
Screw Hole



Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2012/09/25	Deciphered Date	2013/09/30	
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			Size	Document Number
Date:	Tuesday, September 25, 2012	Sheet	42	of 57

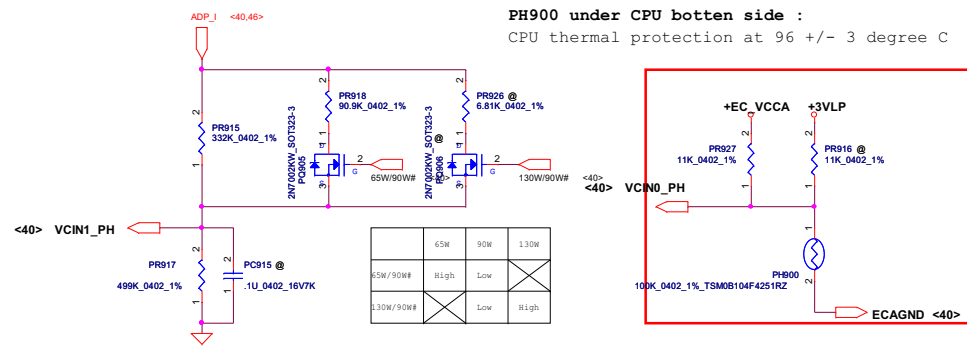
Version Change List (P. I. R. List)

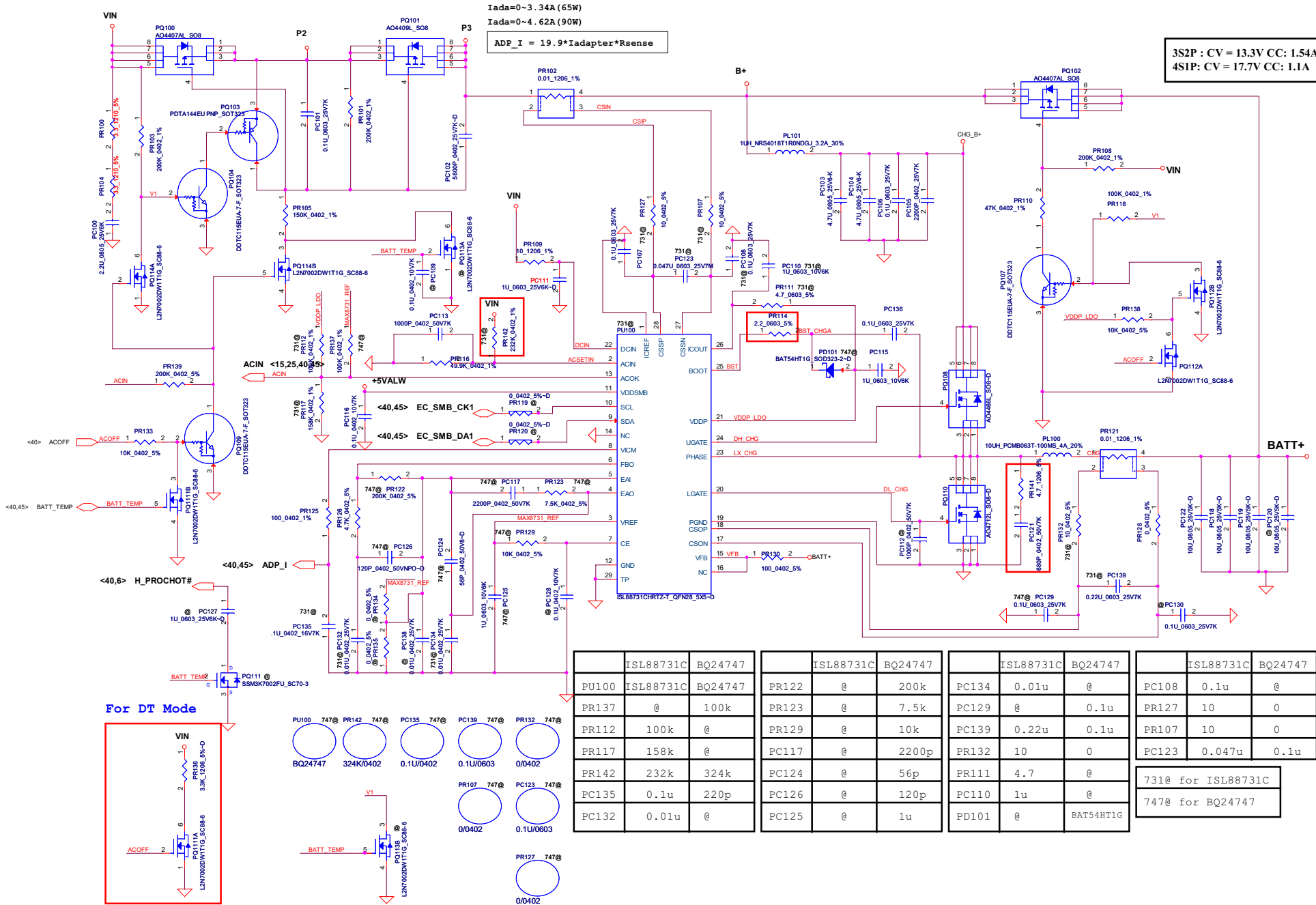
Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	21,39	LVDS	2012/05/17	SED	Add FHD Panel CE_ENABLE, DBC_ENABLE function from SED request	Add CE_EN, DBC_EN control pin to EC	0.2
2	21	LVDS	2012/05/22	SED	Follow SED team request disable CE_EN function	Change RV62 to DE-POP and RV100 to POP for disable CE_EN function	0.2
3	33	Audio codec	2012/05/23	CODEC	Follow CODEC vendor suggestion	Add NBDIO JACK_PLUG delay circuit. Separate NET JACK_PLUG to => JACK_SENSE# & => JACK_PLUG#	0.2
4	16,21	Touch Screen	2012/05/29	HW	Add touch screen function	Add RV217, RV218, RV219, RV249, CV59, CV60, CV328, DV13, QV16, JTOUCH	0.2
5	39	Board ID	2012/05/30	HW	Board ID change for PT	Change RES from 8.2k_0402 (SD028820180) to 33k_0402 (SD028330280)	0.2
6	21,39	Touch Screen	2012/05/30	HW	Add touch screen function power control	Add NET_TOUCH_ON# from JTOUCH to UEI.82 (K890i2) for TOUCH_SCREEN_PANEL power control	0.2
7	33	Audio codec	2012/05/30	HW	Follow RealTek suggestion remove, delete reserve MUTE circuit	Delete D1,QA1,QA2,QA3,RA24,RA26,RA60,RA62,RA68,RA109,CA72,CA73	0.2
8	15,16, 39,41	ESD	2012/05/30	ESD	ESD ask CAP for reserve	Reserve 0.1u/0402 CH104,C223,CH105,CE27,CE29	0.2
9	14	Green CLK	2012/05/30	HW	For Green CLK test	Change RH31,RH41,RV232 Ohm from *GCLK#* to *@* for break the clock signal to device	0.2
10	10,26,41	DC/DC	2012/05/31	HW	Change "+1.5V_CPU_VDDQ", "+1.5VS", "+1.5VGS" derating	Change RC150 330k/0402 to 2M/0402; RC151 100k/0402 to 470k/0402, RZ18 100k/0402 to 470k/0402, RV115 0/0402 to 2M/0403	0.2
11	41	DC/DC	2012/05/31	HW	For power sequence trunning	Change RZ15 to DE-POP	0.2
12	06,15,16, 39,41	ESD	2012/05/31	ESD	Follow ESD team request	Change 0.1u/0402 from "@*" to POP	0.2
13	32	Green CLK	2012/06/15	HW	Change for Green CLK bom control	Change RL21,RL30 from "@*" to "GCLK#"	0.2
14	41	DC/DC	2012/06/15	HW	For WLAN card power sequence issue	Change RZ4,RZ13 from 470k/0402 56k/0403	0.2
15	35,41	Schematic page modify	2012/06/18	HW	Schematic page modify for easily maintain.	Swap Page. 35 & Page 41.	0.2
16	41	ODD	2012/06/18	HW	Change component location for easily maintain.	Move CH9,CH10 from Page.13 to Page.41	0.2
17	39	FAN	2012/06/29	HW	Fan speed noise issue	Reserve 220p/0402 CE24	0.2
18	6	CPU	2012/06/29	ESD	System boot-up shot down issue.	Change CC151 from POP to "@"	0.2
19	21,35, 39,40,41	Circuit adjust	2012/07/01	HW	Circuit & page adjust for OAK 15" & OAK 17"	1. Swap P.35 & P.41 and move touch screen circuit from P.21 to P.41. 2. Swap P.39 & P.40 page no	0.2
20	40	LID SW	2012/07/01	HW	LID SW need a trace for debug and switch.	Add RE81 for LID SW.	0.2
21	25	GPU	2012/07/01	HW	Follow AMD request, MarsPro will used MPLs.	Change RV75,RV76,RV81 from "DIS@" to "TH@"	0.2
22	29	GPU	2012/07/01	HW	Follow AMD request, MEM_CALRP2 is not need for Mars ASIC now.	Change RV205 from "MS@" to "@"	0.2
23	38	MINI card	2012/07/03	HW	Power Control for Mini card didn't need	Change R17 to "@"	0.2
24	6	XDP	2012/07/06	HW	S3 return hang issue	Change RC89 from "@*" to POP	0.2
25	23	GREEN CLK	2012/07/09	HW	Follow Green CLK FAE suggestion	1. Change UG1.2(+3VALV) & UG1.9(+3VALV) connect to +LAN_IO 2. Add R787 connect from +RTC_BATT to C5.2 & UG1.10 3. Change C14 from 0.1u to 5p/0402 4. Change C8 connect from +3V_ALW to +LAN_IO 5. Add R788.0ohm/0402 from +RTC_VCC to UG1 for GCLK & DH1 select	0.2
26	35	MOAT	2012/07/09	ESD	For ESD request reserve CAP.	Reserve those CAP for ESD MOAT.	0.2
27	18	LVDS	2012/07/10	HW	Change RES and reserve CAP for LVDS issue	Change RH185 from 0ohm-short to 0ohm/0805, and reserve CH106 1U/0402	0.2
28	41	Connector	2012/07/10	ME	For ME request	Change JBTB1 footprint from SP02000G800 (GLD) to SP02000MJ00	0.2
29	13	PCH	2012/07/11	ESD	Follow ESD team request	Add RH44,RH46,RH70 & NET_PCH_JTAG_TMS_R, PCH_JTAG_TDI_R, PCH_JTAG_TDO_R for break signal trace	0.2
30	40	PCH	2012/07/11	ESD	Follow ESD team request	1. Change NET_NAME "N59110727" to "WL_BT_LED#_R" 2. Reserve 0.1u/0402 on "WL_BT_LED#_R" for ESD	0.2
31	21	LVDS	2012/07/11	HW	Reserve for CE function for LVDS connector	Change CE_EN_R from dummy to JLVDS.18	0.2
32	32	Connector	2012/07/12	ME	For ME request	Change JLAN CPN from "DC234004V00" to "SP011207090"	0.2
33	40	FAN	2012/07/16	HW	For FAN_SPEED1 noise issue	Change CE29 from "@*" to POP	0.2
34	14	Touch PAD	2012/07/17	SED	Change Touch PAD SMBUS port for SMBUS issue	Change Touch PAD SMBUS port for SMB0 to SMB	0.3
35	32	GREEN CLK	2012/07/19	HW	Follow Silego FAE request	Change RL21 from 510 ohm to 0 ohm/0402	0.3
36	41	Touch Screen	2012/08/07	SED	Follow SED team request change JTOUCH USB signal conatct.	Change JTOUCH Pin define.	0.3
37	34	Card Reader	2012/08/14	ESD	Follow ESD team request	Reserve CR11 100p/0402 close to JREAD	0.3
38	23	GREEN CLK	2012/08/16	HW	Fixed GCLK output abnormal issue	Change UG1.2 (UG1/VDD) from +LAN_IO to +3VALW	0.3
39	33	CODEC	2012/08/16	HW	The issue already fixed by new CODEC.	Remove delay circuit and POP RA4	0.3



PBATT battery connector
SMART
Battery:
 01.GND1
 02.GND2
 03.BAT_ALERT
 04.SYS_PRES
 05.BATT_PRS
 06.DAT_SMB
 07.CLK_SMB
 08.BATT1+
 09.BATT2+

PH900 under CPU bottom side :
 CPU thermal protection at 96 +/- 3 degree C

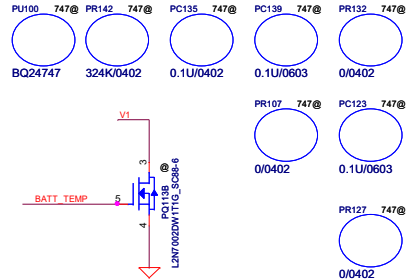
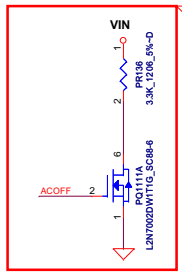




Iada=0~3.34A (65W)
 Iada=0~4.62A (90W)
 ADP_I = 19.9*Iadapter*Rsense

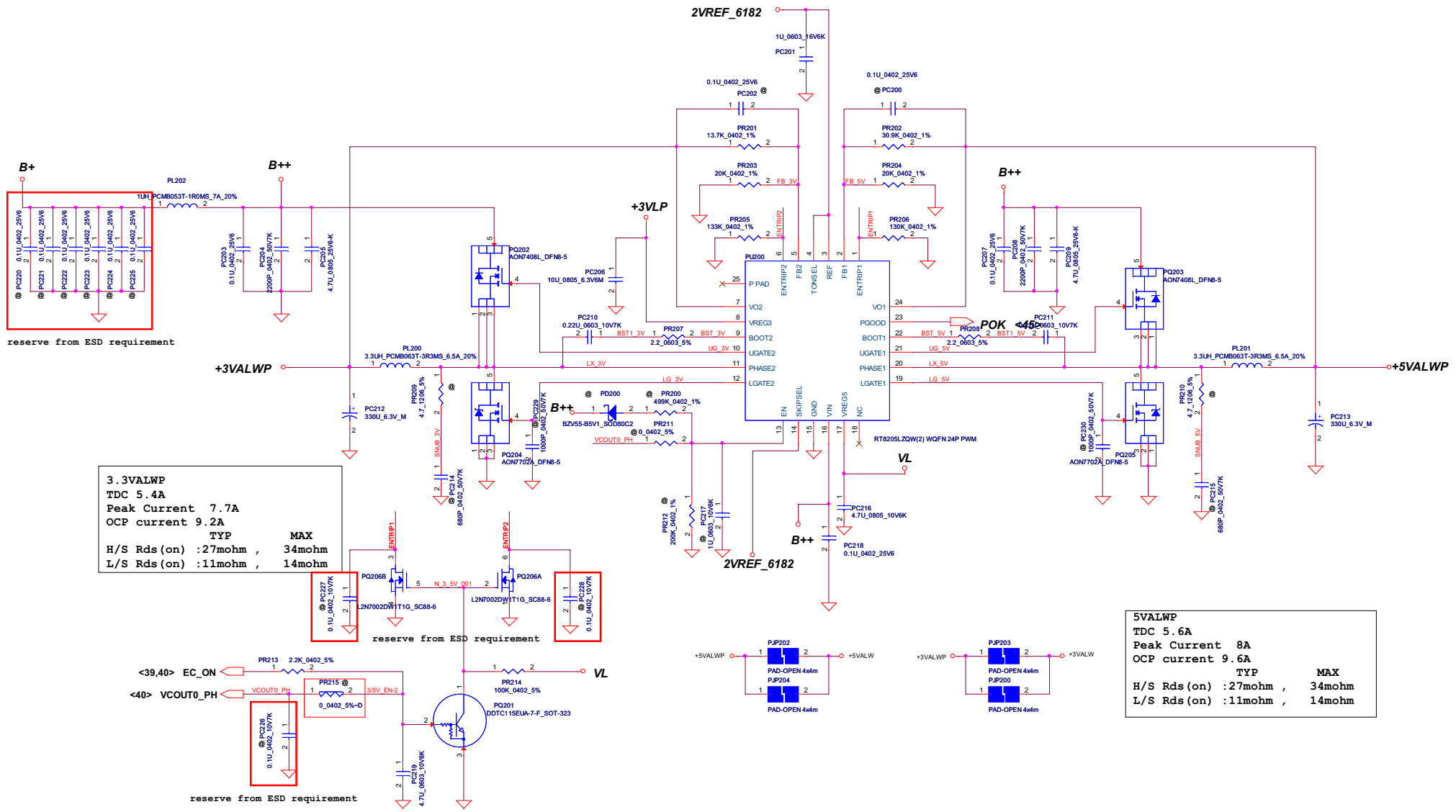
3S2P : CV = 13.3V CC: 1.54A
 4S1P: CV = 17.7V CC: 1.1A

For DT Mode



	ISL88731C	BQ24747		ISL88731C	BQ24747		ISL88731C	BQ24747		ISL88731C	BQ24747
PU100	ISL88731C	BQ24747	PR122	@	200k	PC134	0.01u	@	PC108	0.1u	@
PR137	@	100k	PR123	@	7.5k	PC129	@	0.1u	PR127	10	0
PR112	100k	@	PR129	@	10k	PC139	0.22u	0.1u	PR107	10	0
PR117	158k	@	PC117	@	2200p	PR132	10	0	PC123	0.047u	0.1u
PR142	232k	324k	PC124	@	56p	PR111	4.7	@			
PC135	0.1u	220p	PC126	@	120p	PC110	1u	@			
PC132	0.01u	@	PC125	@	1u	PD101	@	BAT54HT1G			

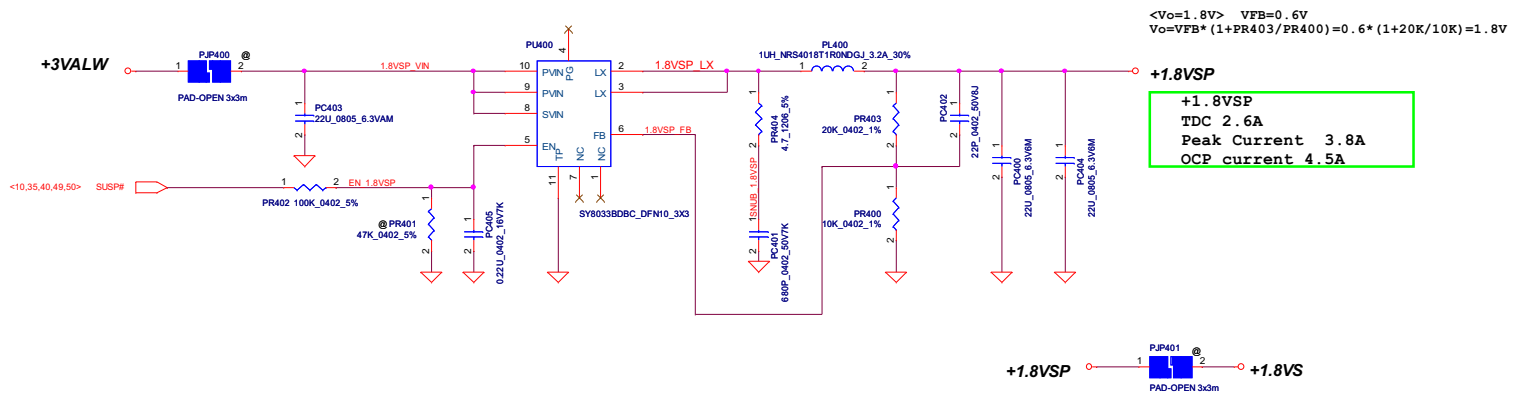
731@ for ISL88731C
 747@ for BQ24747



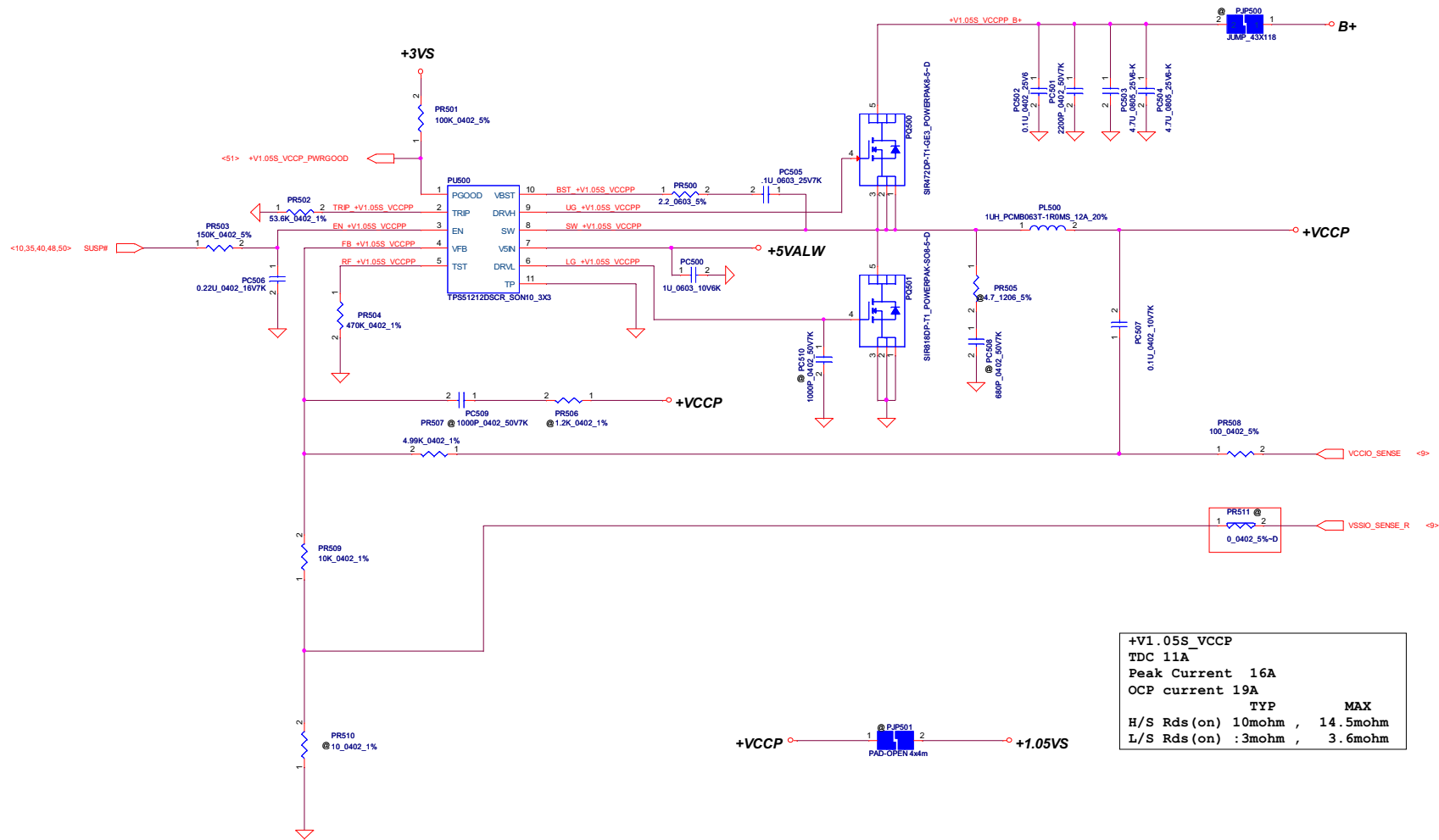
3.3VALWP
 TDC 5.4A
 Peak Current 7.7A
 OCP current 9.2A
 TYP MAX
 H/S Rds(on) :27mohm , 34mohm
 L/S Rds(on) :11mohm , 14mohm

5VALWP
 TDC 5.6A
 Peak Current 8A
 OCP current 9.6A
 TYP MAX
 H/S Rds(on) :27mohm , 34mohm
 L/S Rds(on) :11mohm , 14mohm

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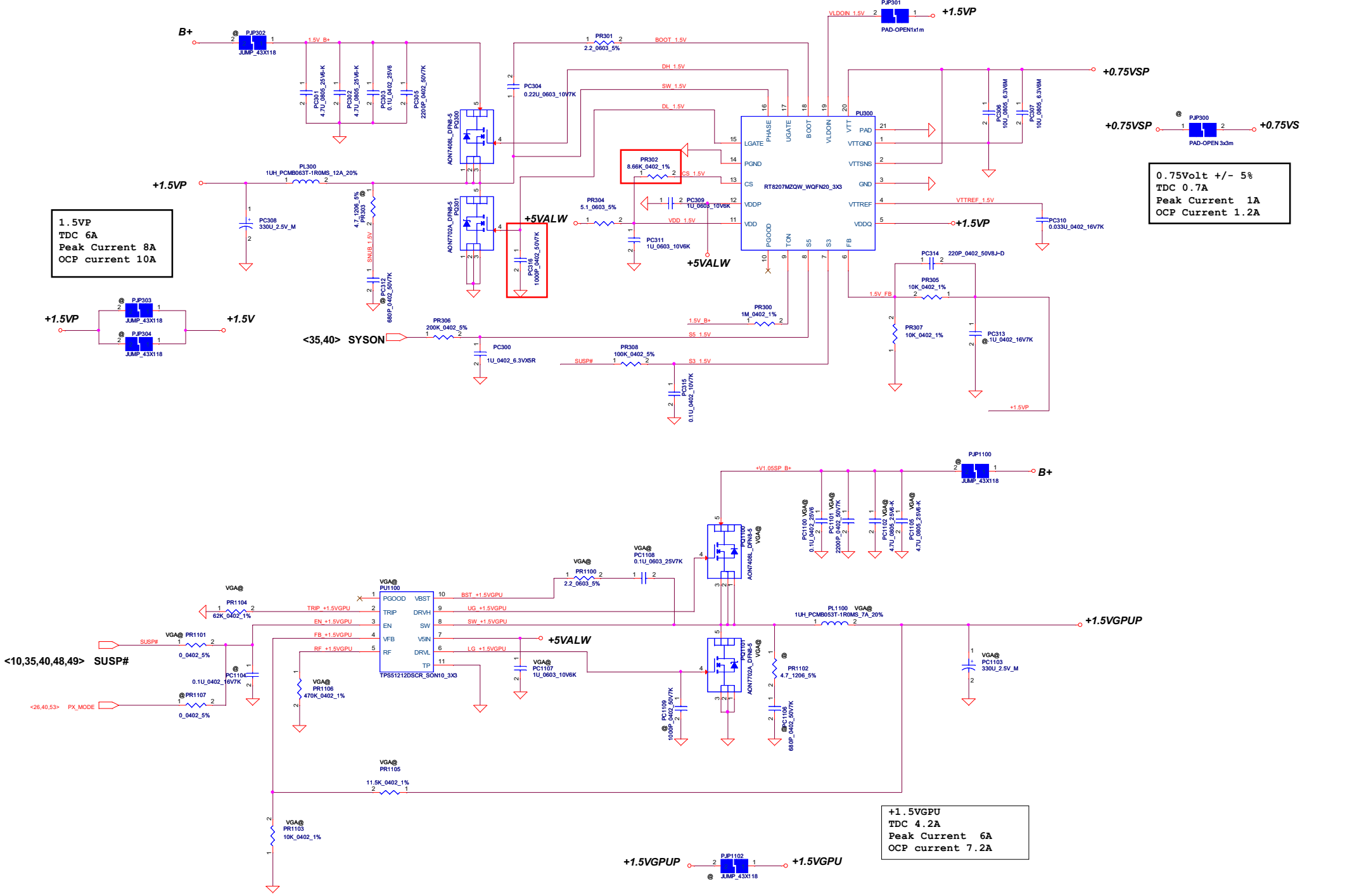
+V1.05S_VCCPP
 TDC 11A
 Peak Current 16A
 OCP current 19A
 TYP MAX
 H/S Rds(on) 10mohm , 14.5mohm
 L/S Rds(on) :3mohm , 3.6mohm

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1.5VP
TDC 6A
Peak Current 8A
OCP current 10A

0.75Volt +/- 5%
TDC 0.7A
Peak Current 1A
OCP Current 1.2A

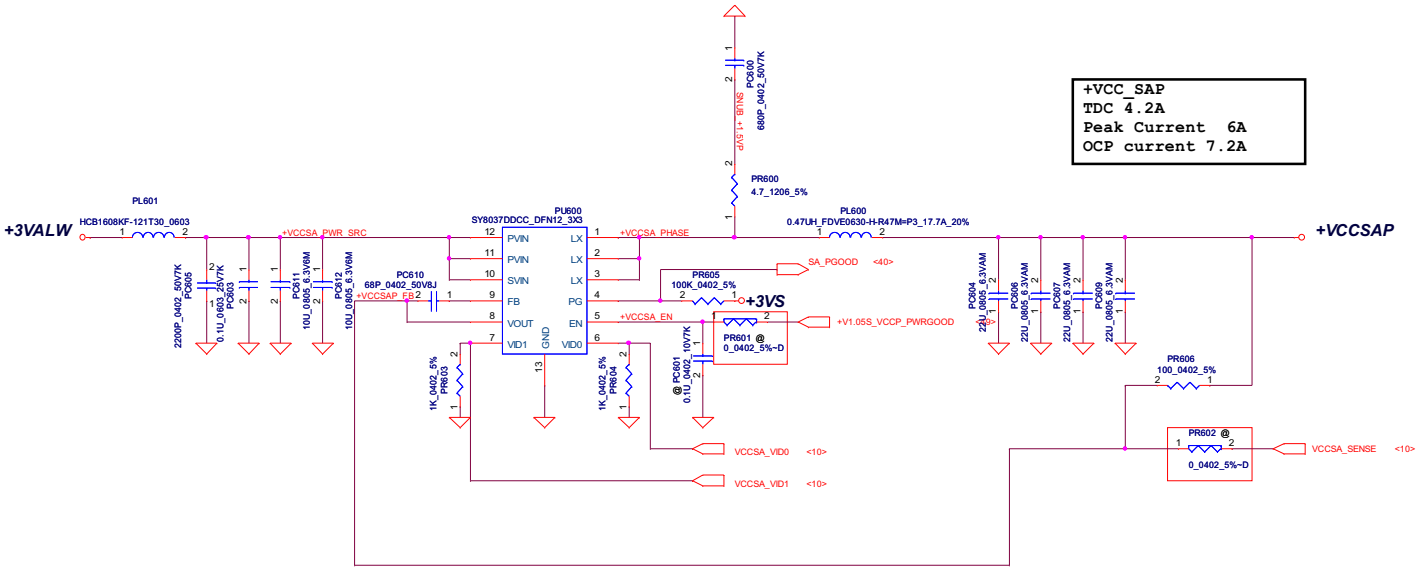
+1.5VGPU
TDC 4.2A
Peak Current 6A
OCP current 7.2A



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Issued Date	2012/09/25	Deciphered Date	2013/09/30	PWR +1.5VP/+1.5VGPUP/0.75VSP
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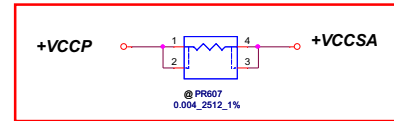
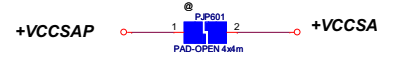
VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.85V
1	0	0.775V
1	1	0.75V

output voltage adjustable network

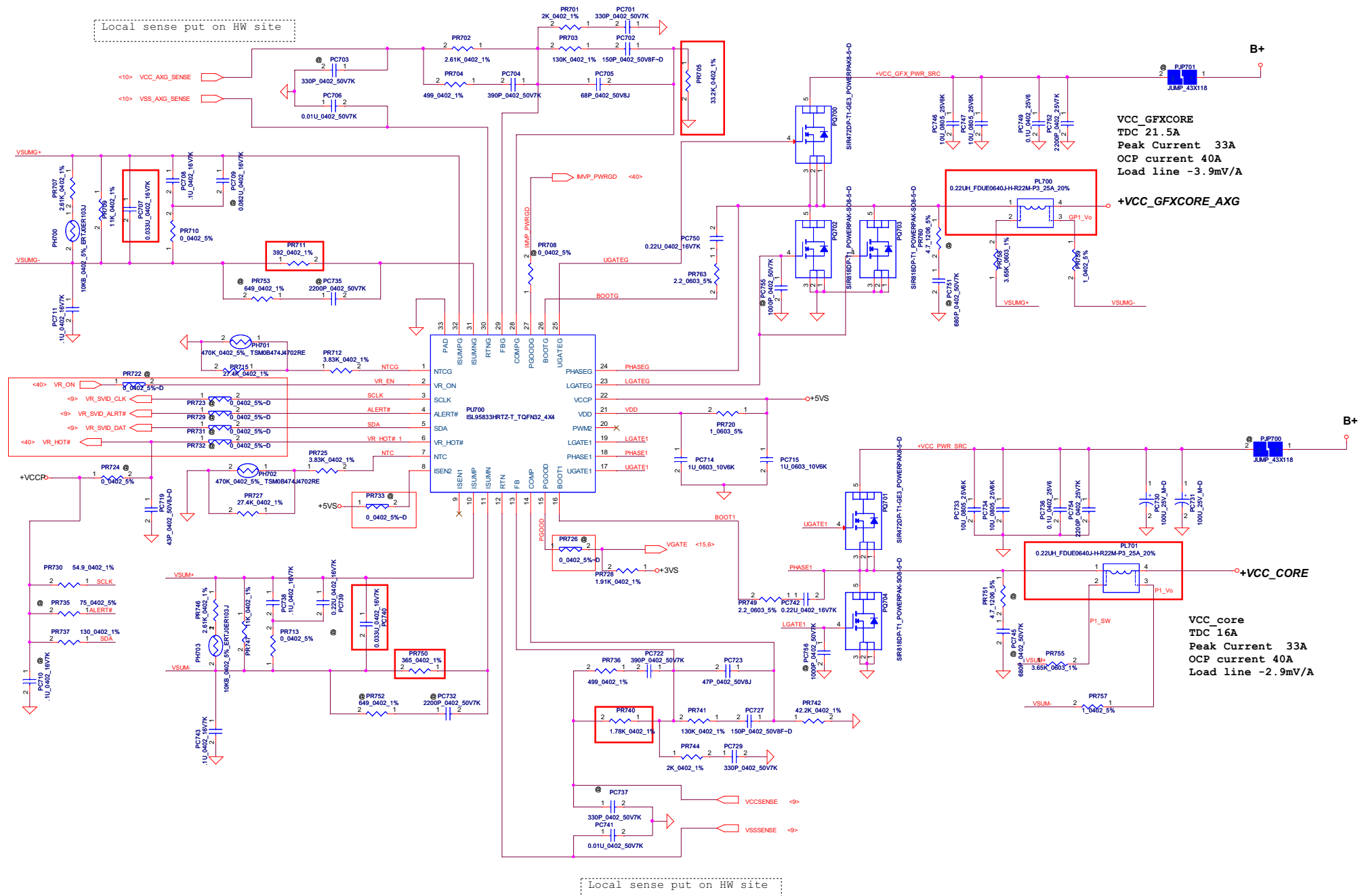


+VCCSAP
 TDC 4.2A
 Peak Current 6A
 OCP current 7.2A

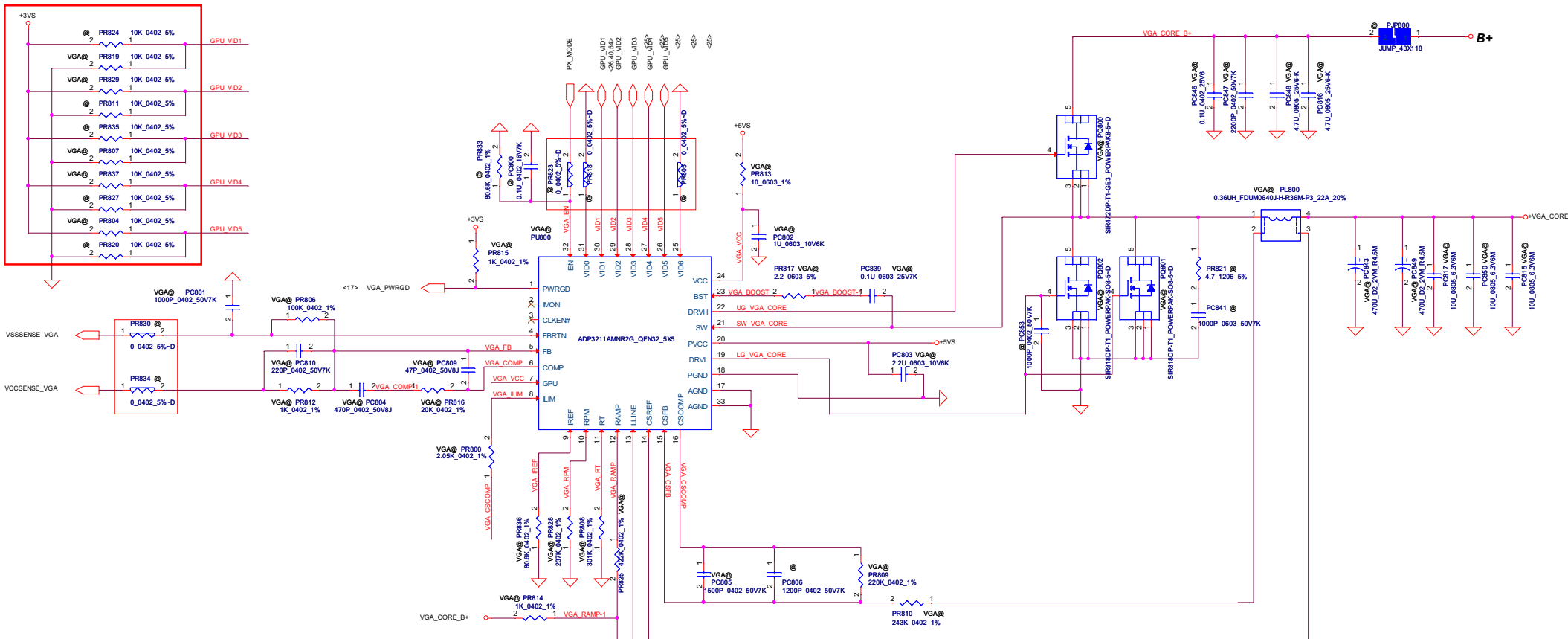
The 1k PD on the VCCSA VIDs are empty.
 These should be stuffed to ensure that
 VCCSA VID is 00 prior to VCCIO stability.



reserve for Pentium and Celeron only



Security Classification		Compal Secret Data		Title	
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Mars Pro

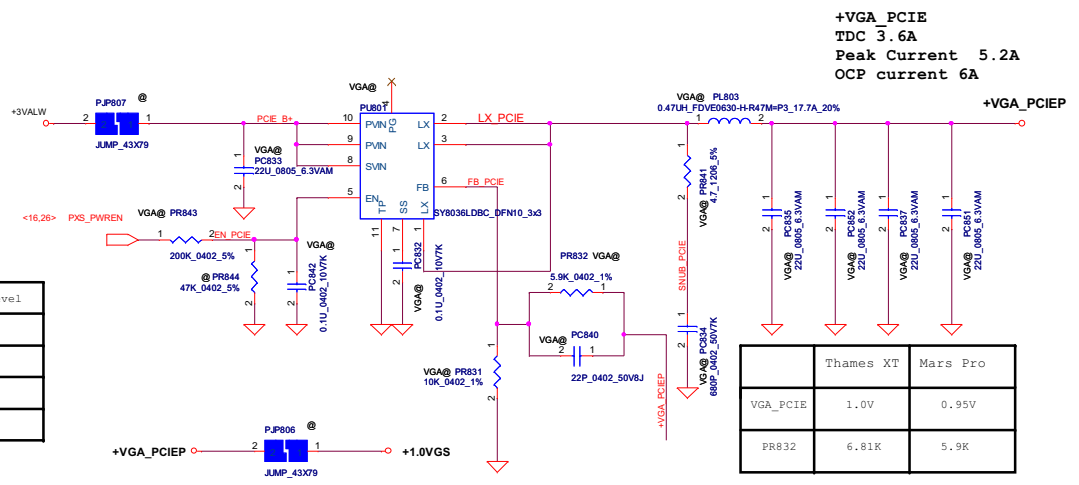
GPU_VID5 (GPIO_10)	GPU_VID4 (GPIO_14)	GPU_VID3 (GPIO_15)	GPU_VID2 (GPIO_16)	GPU_VID1 (GPIO_20)	Core Voltage Level
0	1	1	1	1	1.125V
1	0	0	0	0	1.1V
1	0	0	0	1	1.075V
1	0	0	1	0	1.05V
1	0	0	1	1	1.025V
1	0	1	0	0	1V
1	0	1	0	1	0.975V
1	0	1	1	0	0.95V
1	0	1	1	1	0.925V
1	1	0	0	0	0.9V
1	1	0	0	1	0.875V
1	1	0	1	0	0.85V
1	1	0	1	1	0.825V
1	1	1	0	0	0.8V

+VGA CORE
TDC 22A
Peak Current 30A
OCF current 36A
FSW=350kHz
DCR 1.1mohm +/-5%
Loadline = 1.5mohm

Thames XT

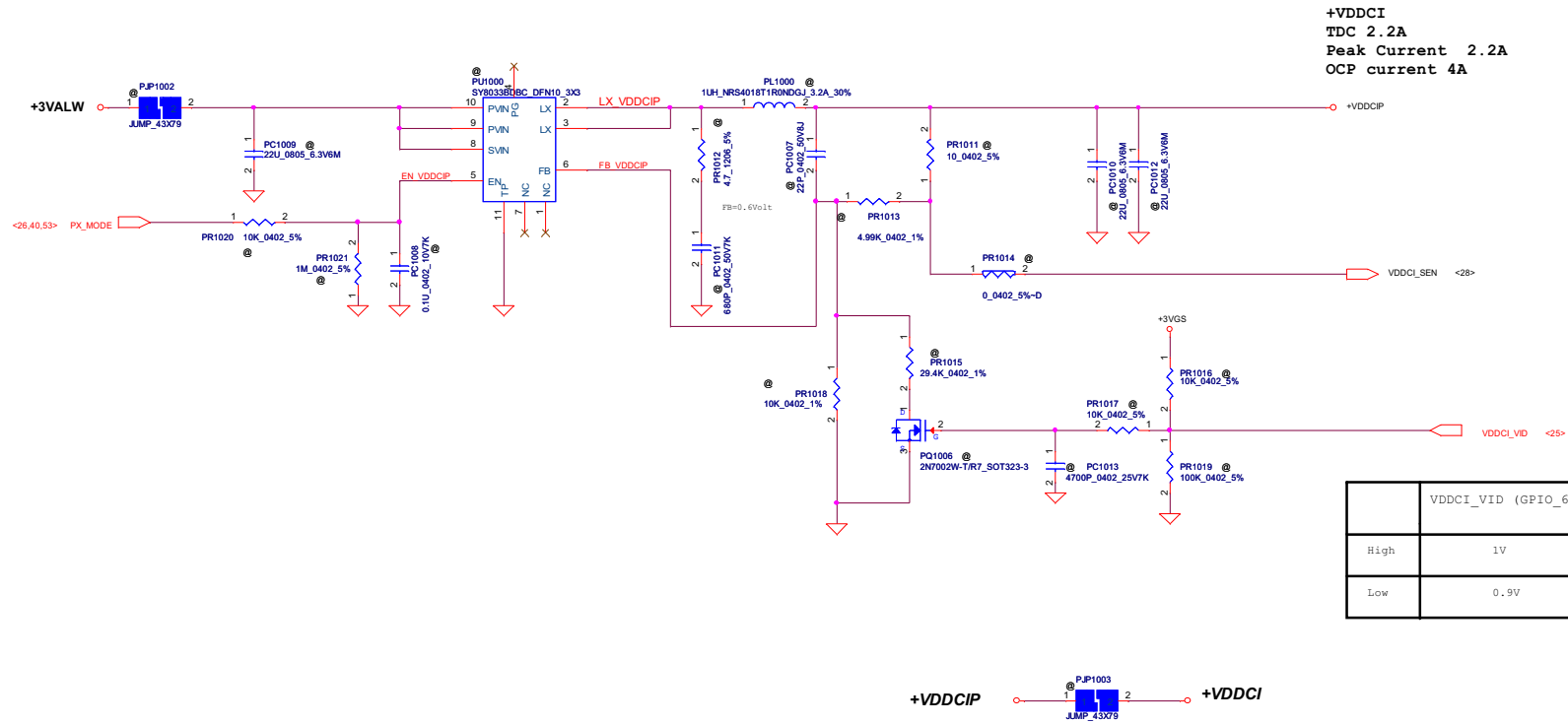
GPU_VID5 (GPIO_10)	GPU_VID4 (GPIO_14)	GPU_VID3 (GPIO_15)	GPU_VID2 (GPIO_16)	GPU_VID1 (GPIO_20)	Core Voltage Level
1	0	0	1	0	1.05V
1	0	1	0	0	1V
1	0	1	1	0	0.95V
1	1	0	0	0	0.9V
1	1	0	0	1	0.875V
1	1	0	1	0	0.85V
1	1	0	1	1	0.825V
1	1	1	0	0	0.8V

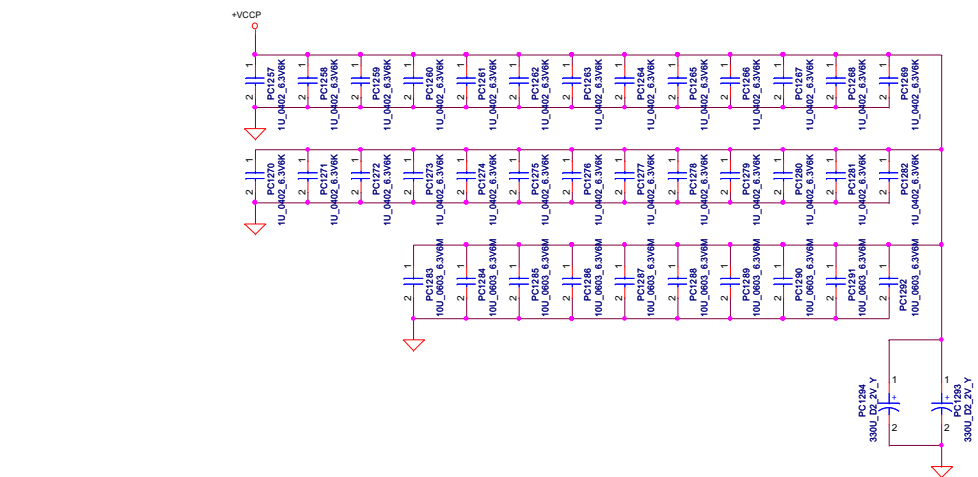
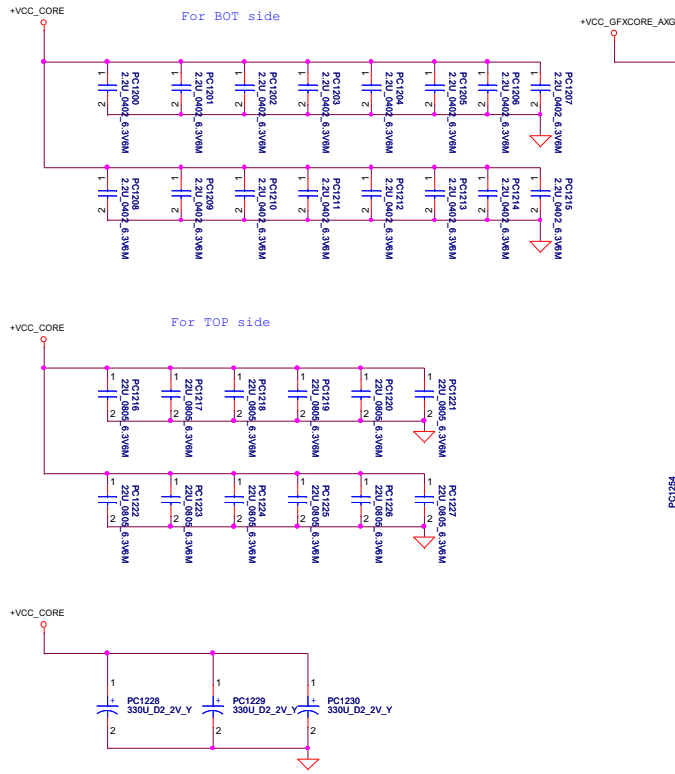
+VGA CORE
TDC 20A
Peak Current 30A
OCF current 36A
FSW=350kHz
DCR 1.1mohm +/-5%



+VGA PCIEP
TDC 3.6A
Peak Current 5.2A
OCF current 6A

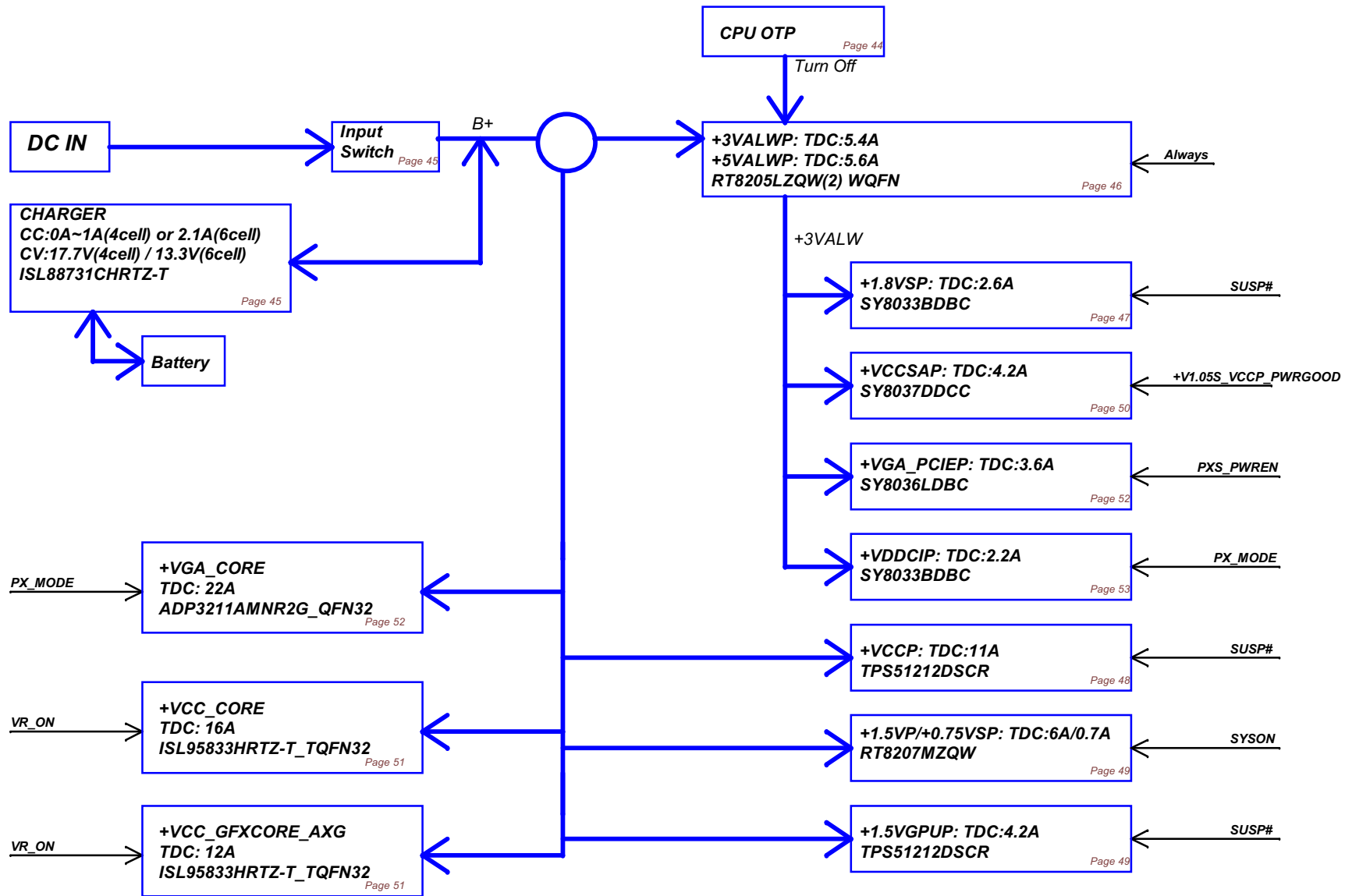
	Thames XT	Mars Pro
VGA_PCIE	1.0V	0.95V
PR832	6.81K	5.9K





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Power block



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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	52	VCORE	12/05/11	Morris	adjust VR parameter	change PL700 and PL701 from 0.36u to 0.22u change PC707 and PC740 from 0.047u to 0.033u change PR750 from 649 to 365 change PR711 from 649 to 392 change PR740 from 1.91k to 1.78k change PR705 from 150k to 33.2k	X00
2	45 46 47	DCIN/BATT CONN/OTP CHARGER 3.3VALWP/5VALWP	12/05/11	Morris	follow SSI memo for part shortage issue	change PQ112,PQ114,PQ1111,PQ206,PQ904 from SB000000CQ00 to SB000000PV00	X00
3	50	+1.5VP/1.5VDGPU/0.75VSP	12/05/15	Morris	design change	change PR302 from 12k to 8.66k	X00
4	51	+VCCSAP	12/05/23	Morris	for Pentium and Celeron special BOM	add PR607 and reserve	X00
5	50	+1.5VP/1.5VDGPU/0.75VSP	12/07/06	Morris	design change to reduce low-side mosfet induce	add PC316 1000pf	X01
6	46	CHARGER	12/07/17	Morris	from EMI request	change PR114 from 0 to 2.2 add PR141 and PC121	X01
7	46	CHARGER	12/07/17	Morris	design change to solve Battery LED is still on after unplug AC when SUT in S3S4S5 issue	change PR142 from 210k to 232k for ISL88731C (X76) change PR142 from 309k to 324k for BQ24747 (X76)	X01
8	45	DCIN/BATT CONN/OTP	12/07/17	Morris	revise OTP setting to 96C from thermal request	change PR927 from 12.1k to 11k	X01
9	52	VCORE	12/08/27	Morris	adjust initial output voltage from vendor recommend	delete PR811,PR827 add PR829,PR837	X02

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