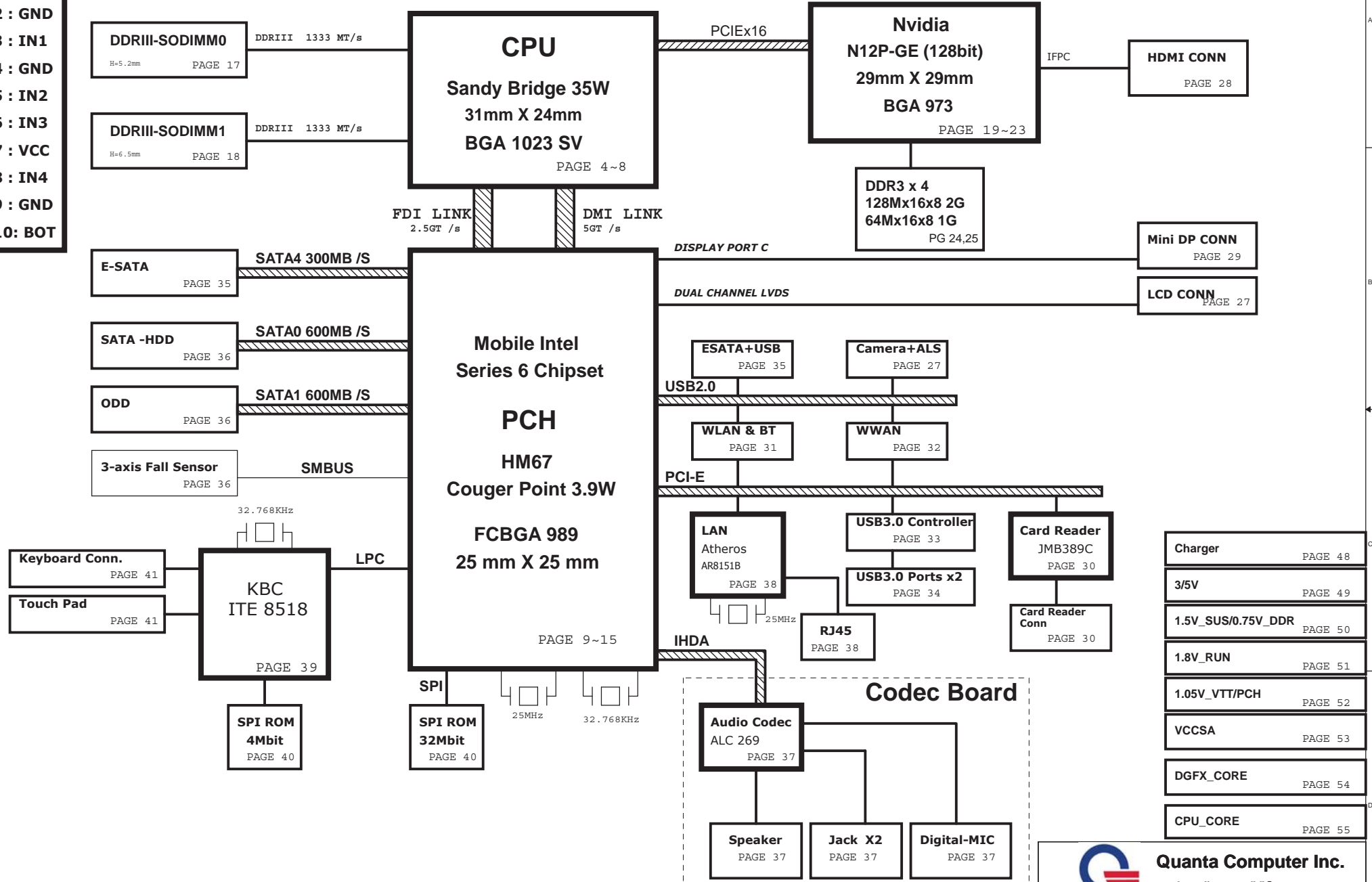


- LAYER 1 : TOP
- LAYER 2 : GND
- LAYER 3 : IN1
- LAYER 4 : GND
- LAYER 5 : IN2
- LAYER 6 : IN3
- LAYER 7 : VCC
- LAYER 8 : IN4
- LAYER 9 : GND
- LAYER 10: BOT

SS8 BLOCK DIAGRAM



Charger	PAGE 48
3/5V	PAGE 49
1.5V_SUS/0.75V_DDR	PAGE 50
1.8V_RUN	PAGE 51
1.05V_VTT/PCH	PAGE 52
VCCSA	PAGE 53
DGFX_CORE	PAGE 54
CPU_CORE	PAGE 55

power State					
S0					
S1					
S3					
S4/S5 AC					
S4/S5 DC Only					
AC/DC No Exist					



Quanta Computer Inc.

PROJECT : SS8

Size Document Number **Power Rails** Rev 3A

Date: Monday, January 03, 2011 Sheet 2 of 57

5

4

3

2

1

D

D

C

C

B

B

A

A



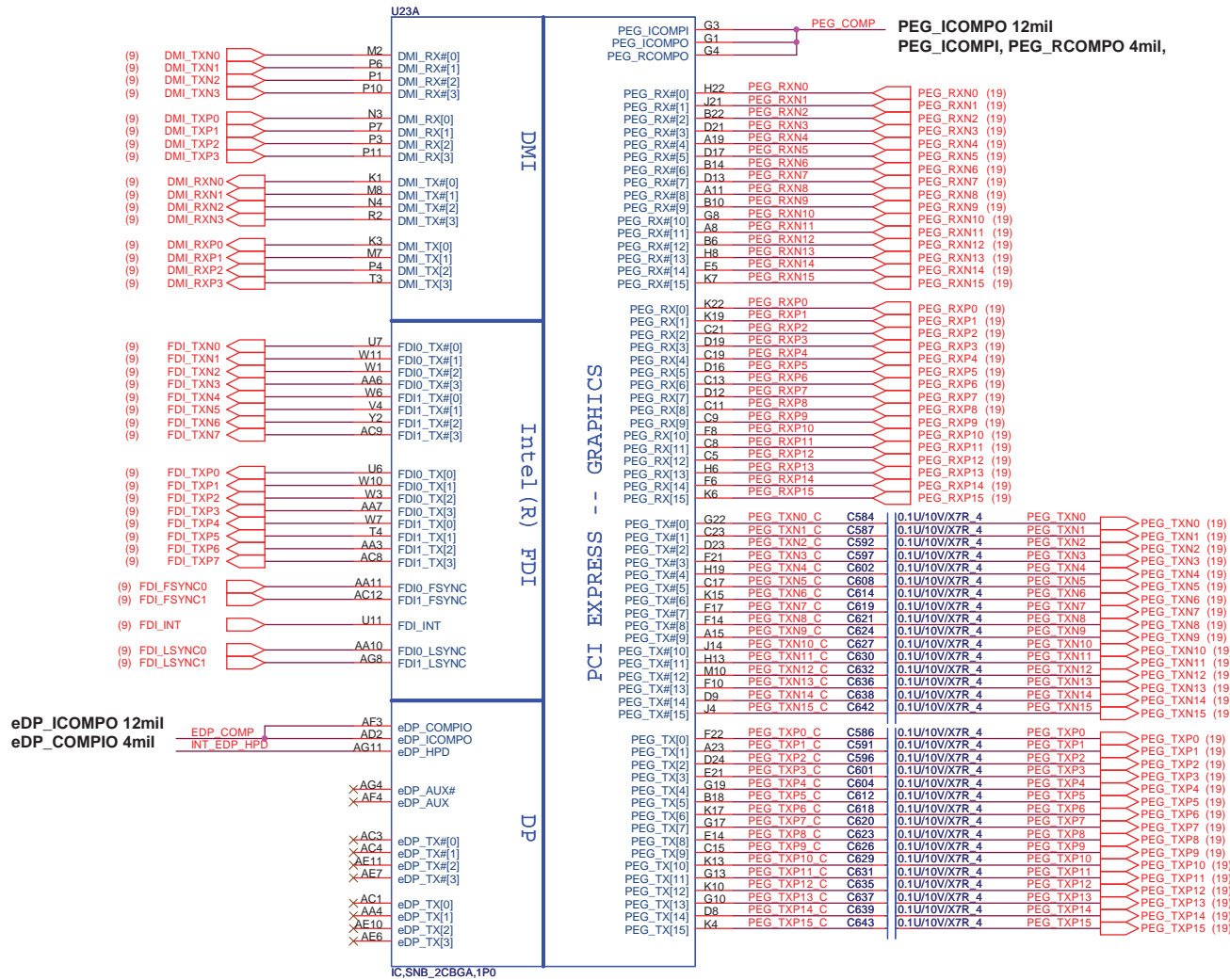
Quanta Computer Inc.

PROJECT : SS8

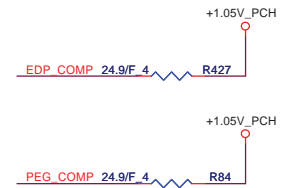
Size	Document Number	Rev
	BLANK	3A

Date: Monday, January 03, 2011 Sheet 3 of 57

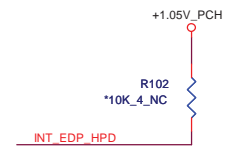
Sandy Bridge Processor (DMI, PEG, FDI)



DP & PEG Compensation

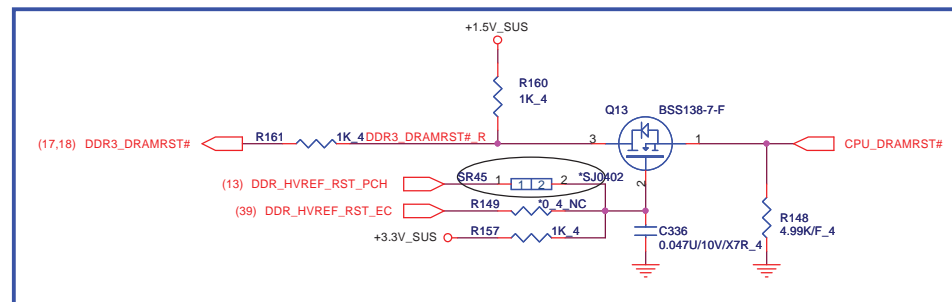


eDP Hot-plug (Disable)

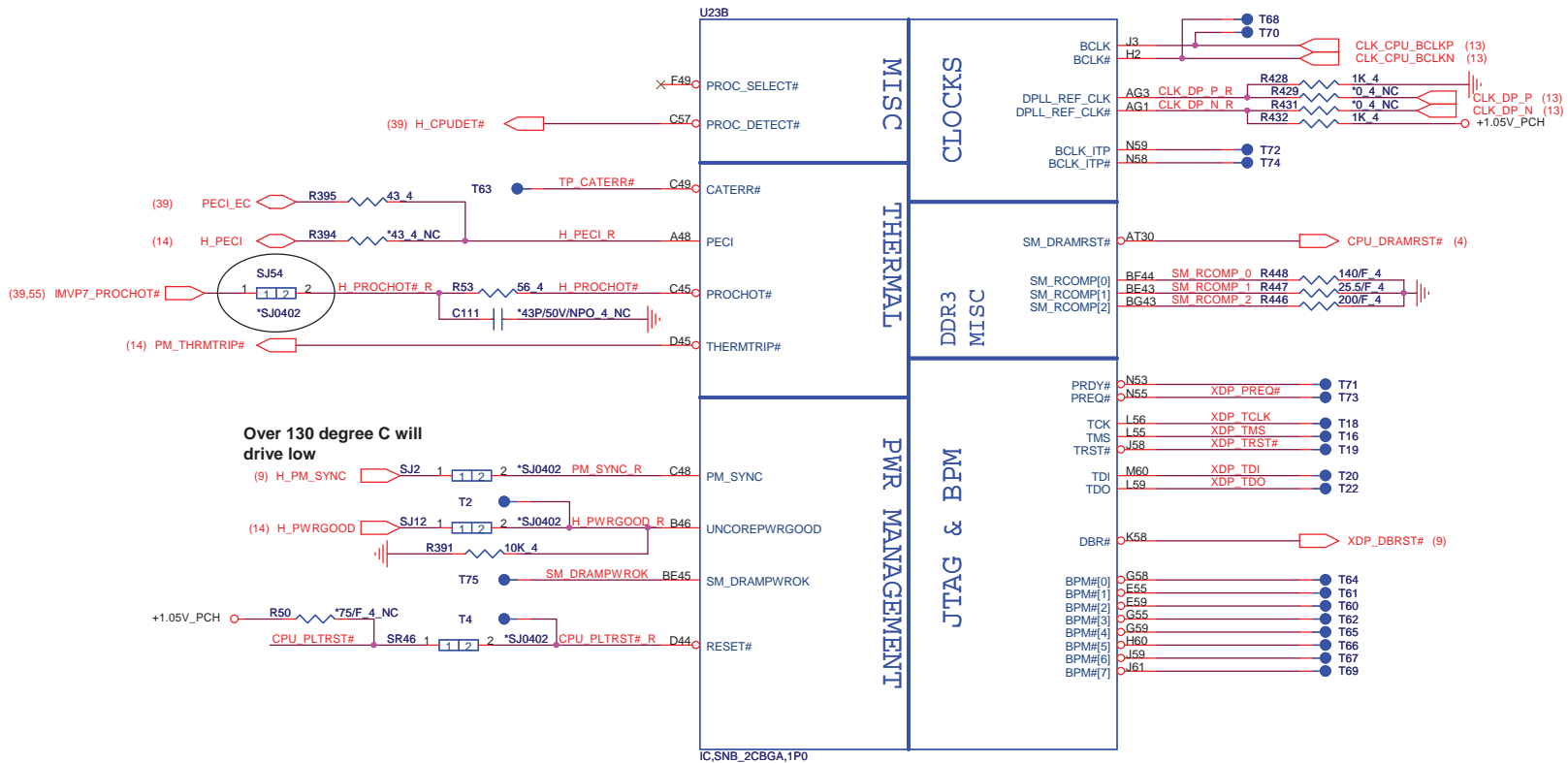


CAD Note: Place PU resistor within 2 inches of CPU

HPD PU/PD resistor values based on CRB and different to DG



Sandy Bridge Processor (CLK, MISC, JTAG)

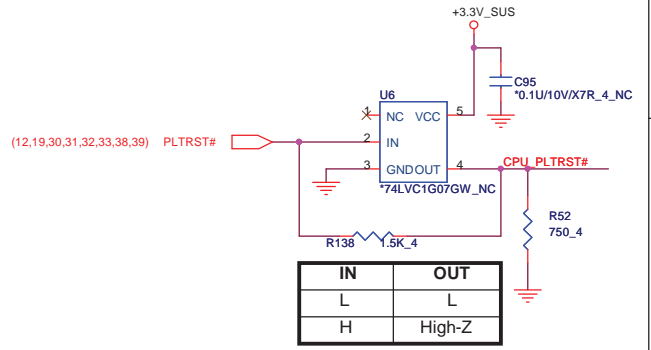
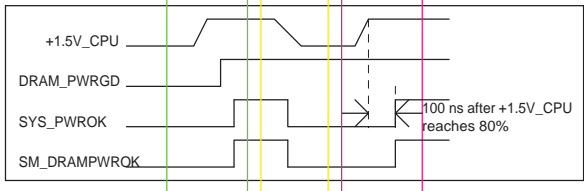
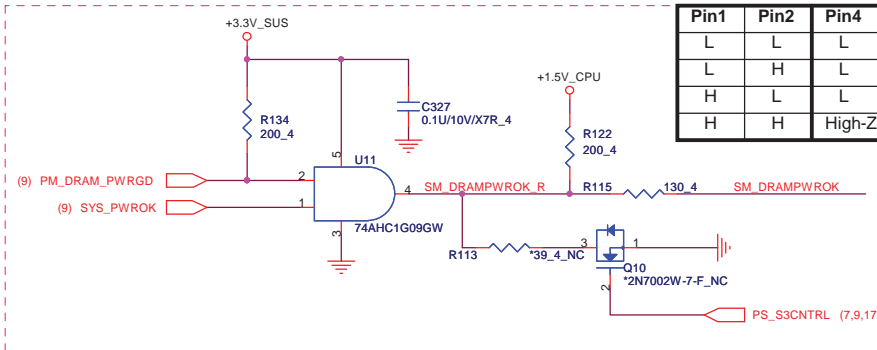


Over 130 degree C will drive low

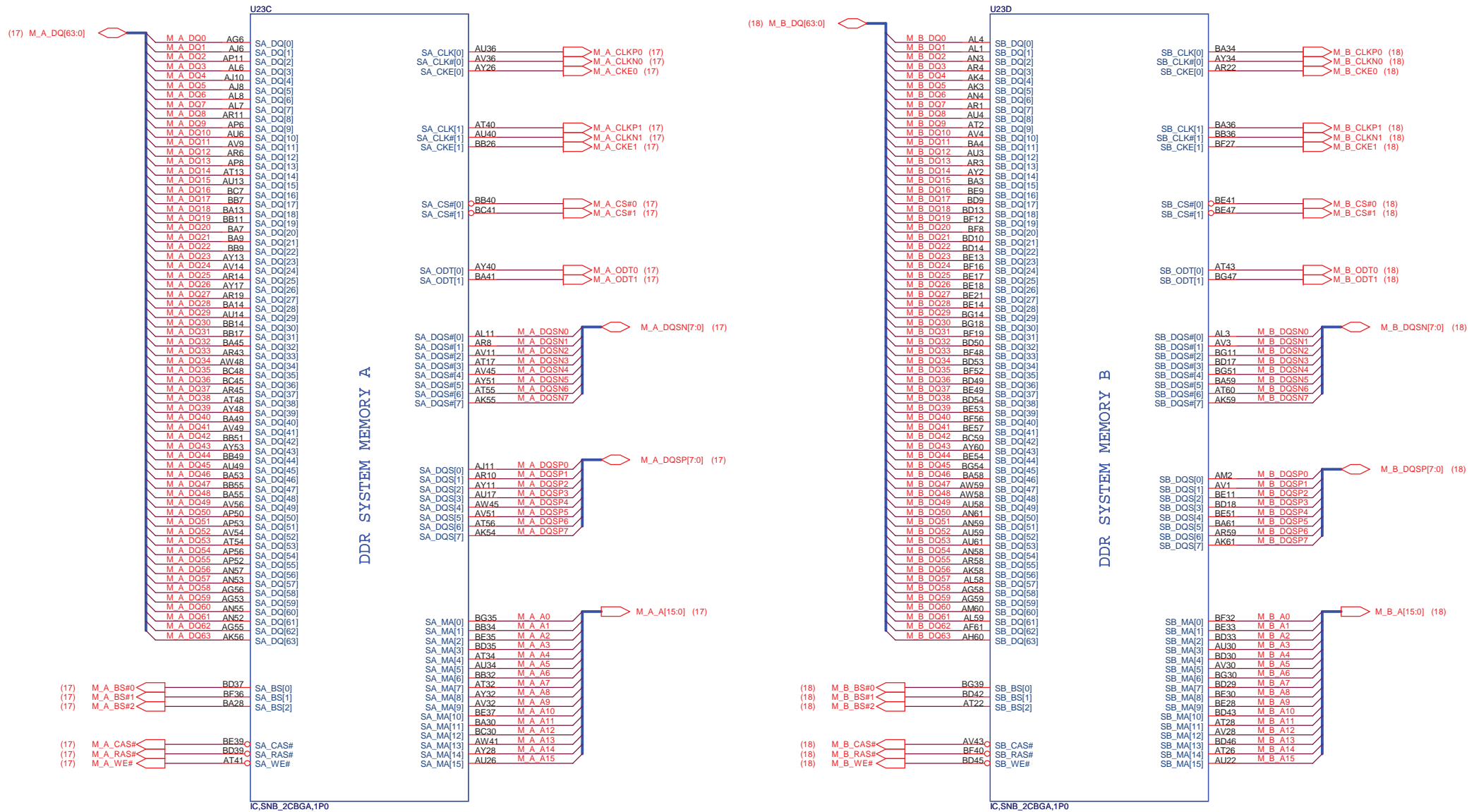
Option for Prochot# function
 68 ohm for unused, 62 ohm for used

H_PROCHOT#	R56	*68 4 NC
H_PROCHOT# R	R49	*62 4 NC
XDP TMS	R420	51 4
XDP TDI	R423	51 4
XDP TDO	R422	51 4
XDP PREQ#	R425	*51 4 NC
XDP TCLK	R421	51 4
XDP TRST#	R417	51 4

When MP, JTAG PU/PD resistor can be removed? (Yes Intel, TDI, TDO, TMS, TRST#, TCK, PREQ#, PRDY#)

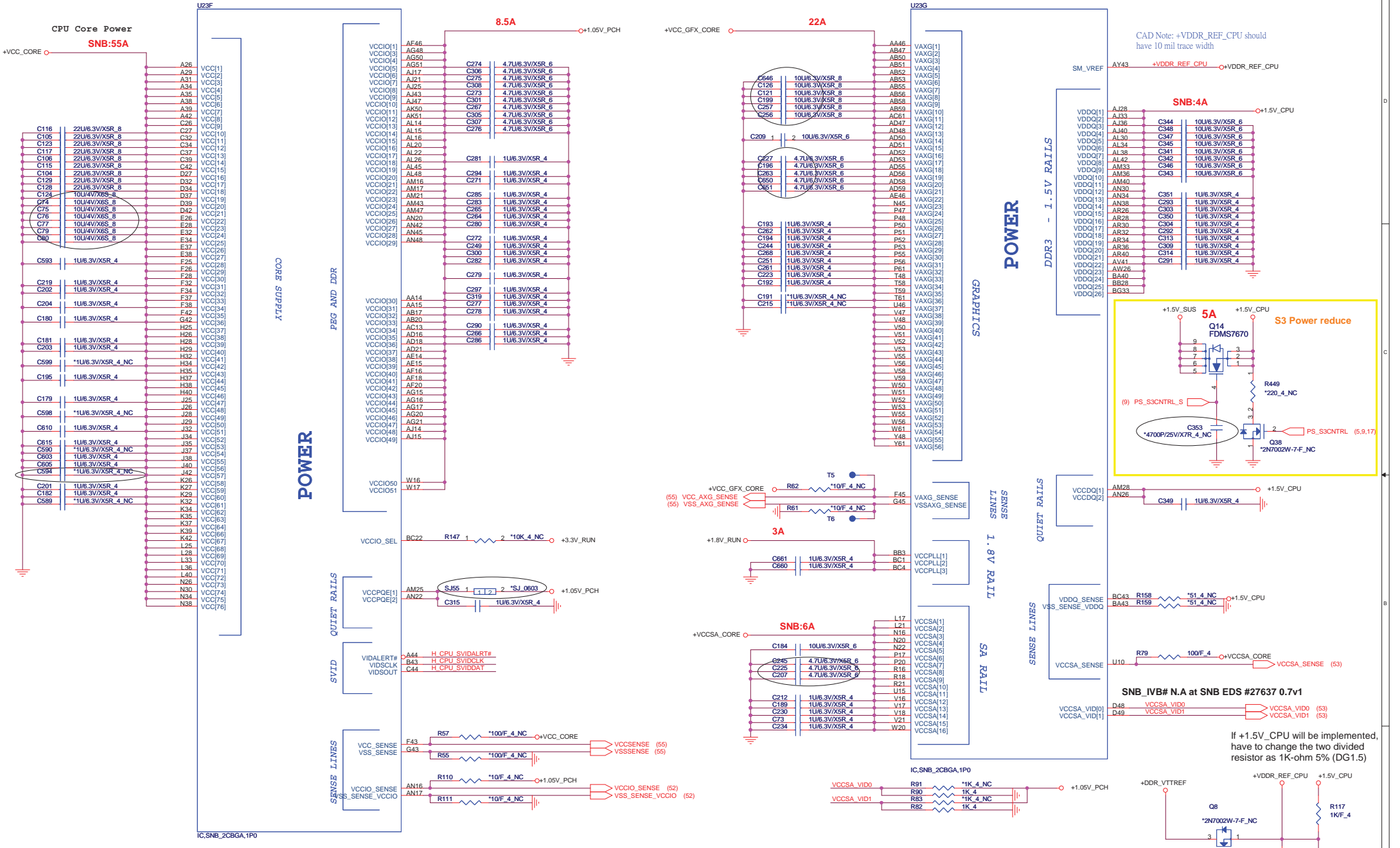


Sandy Bridge Processor (DDR3)



Sandy Bridge Processor (POWER)

Sandy Bridge Processor (GRAPHIC POWER)



CAD Note: +VDDR_REF_CPU should have 10 mil trace width

POWER

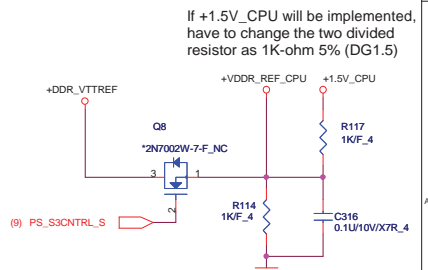
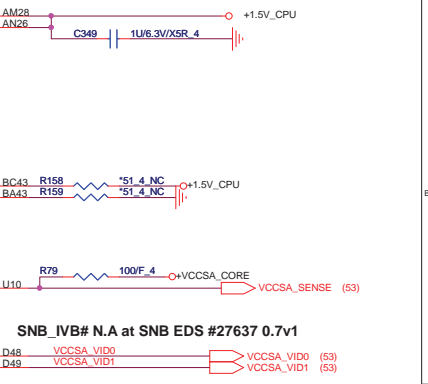
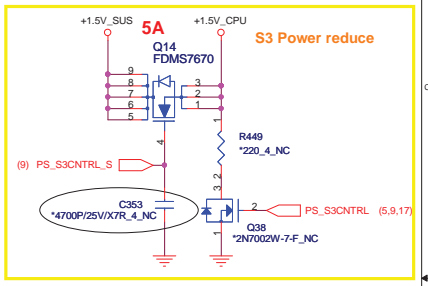
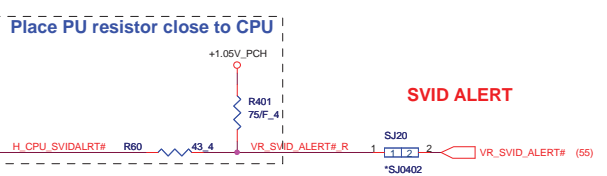
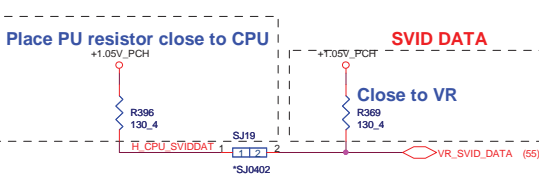
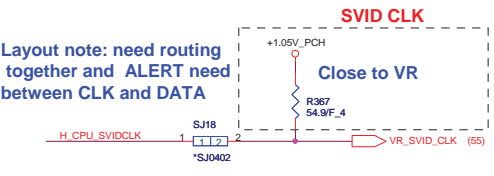
GRAPHICS

SENSE LINES 1.8V RAIL

SA RAIL

SENSE LINES

SENSE LINES



Quanta Computer Inc.

PROJECT : SS8

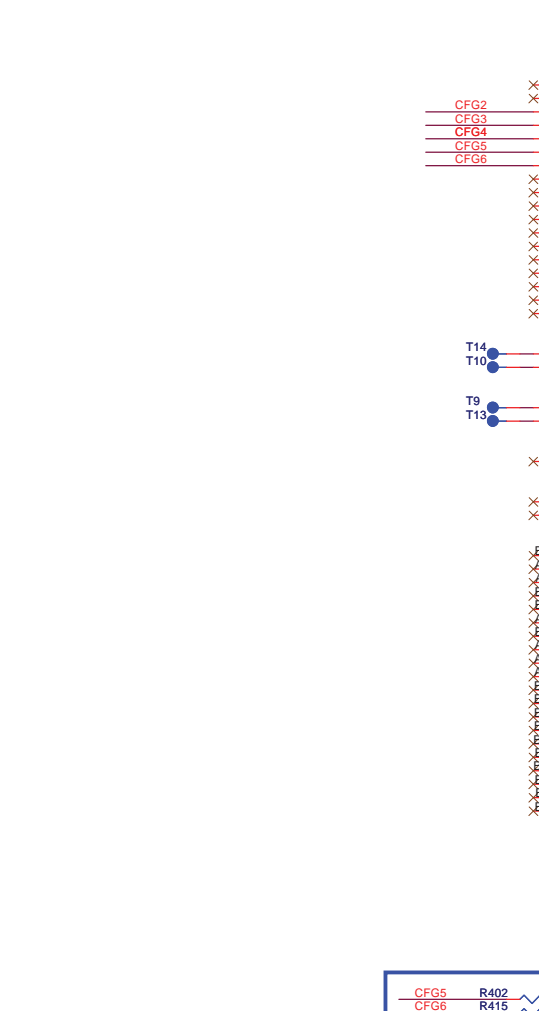
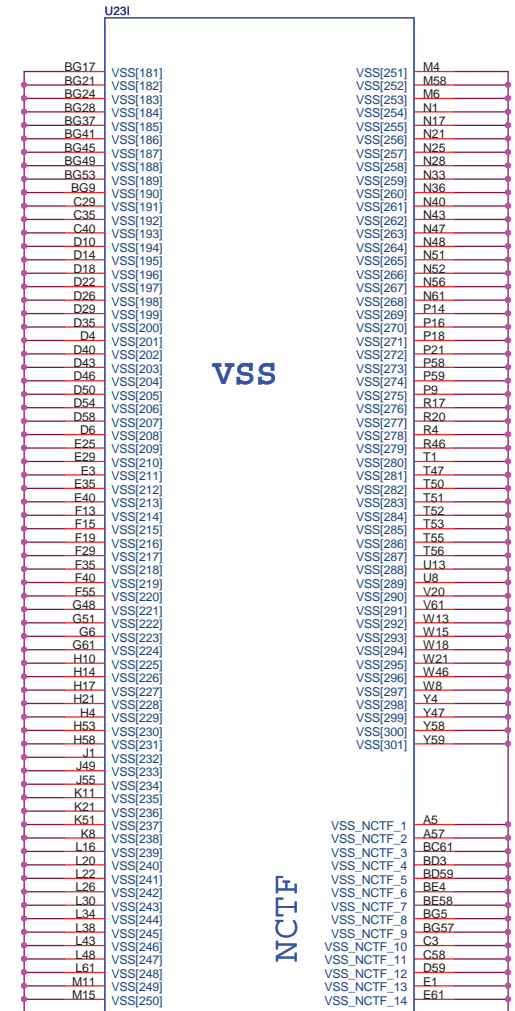
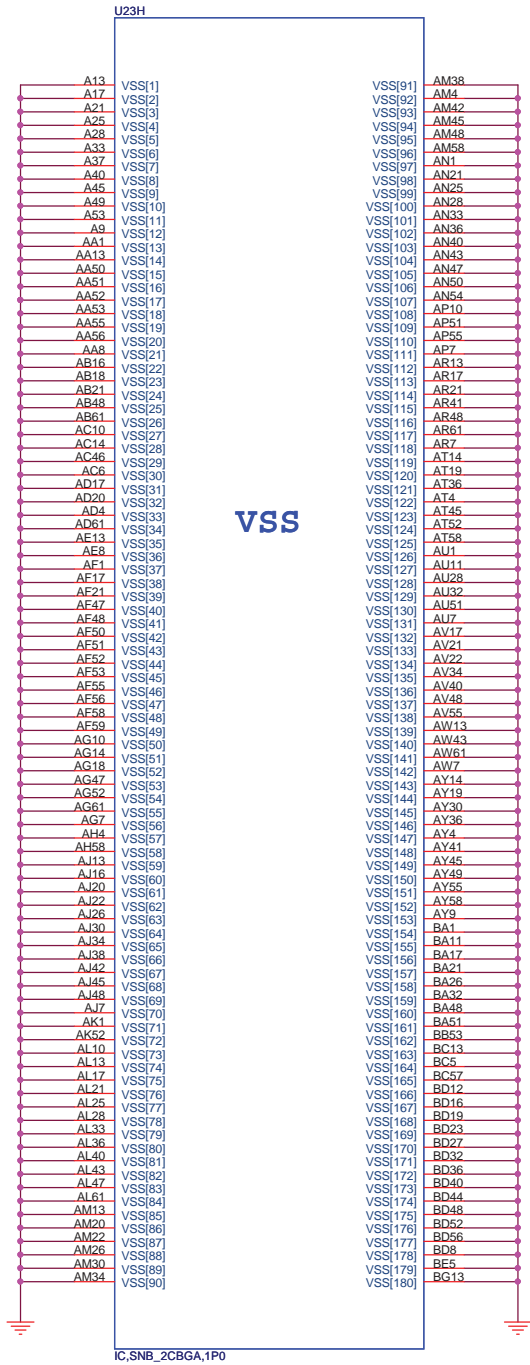
Sandy Bridge 4/5

Size: Document Number: Rev: 3A

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Sandy Bridge Processor (GND)

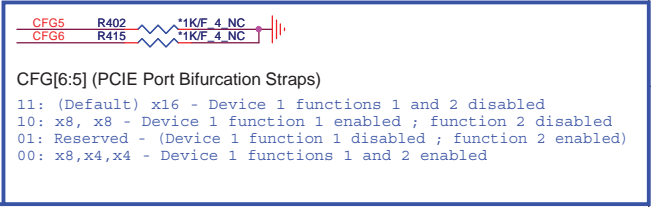
Sandy Bridge Processor (RESERVED, CFG)



Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

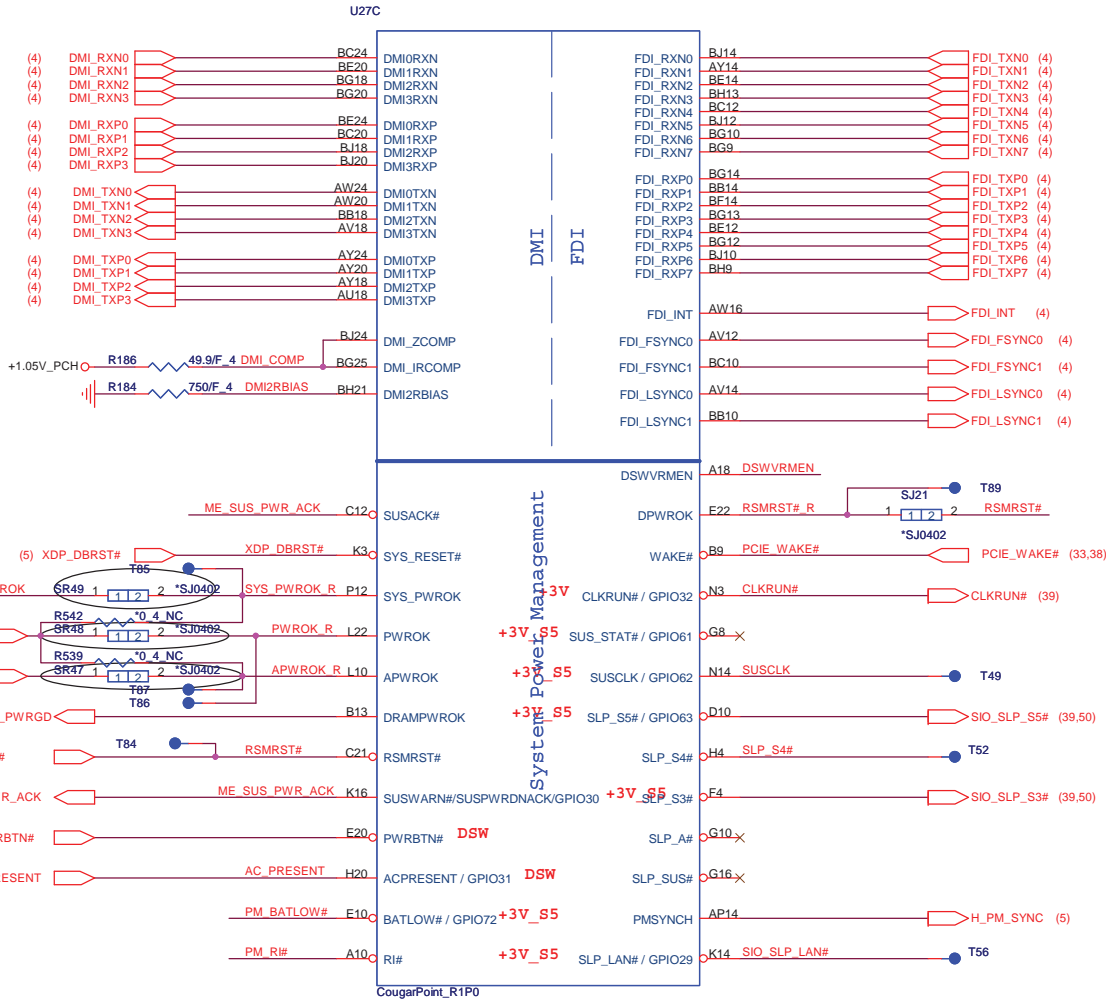
CFG	1	0
CFG2 (PCI-E Static x16 Lane Reversal)	Normal Operation	Lane Reversed
CFG3 (PCI-E Static x4 Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP



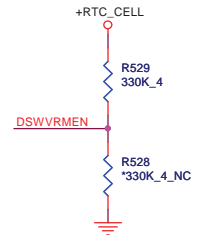
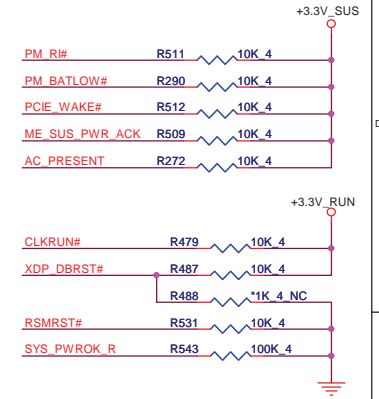
Quanta Computer Inc.
PROJECT : SS8

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Sandy Bridge 5/5
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Cougar Point (DMI, FDI, PM)

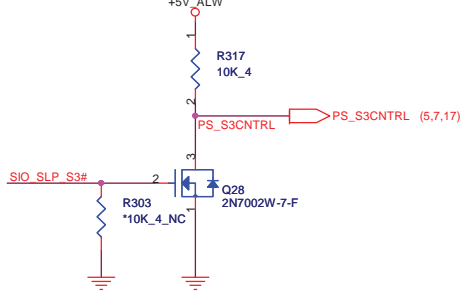


PCH Pull-high/low(CLG)

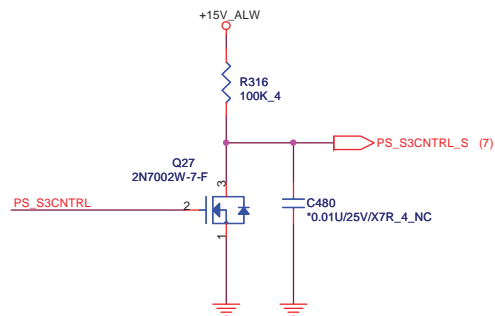


On Die DSW VR Enable
 High = Enable (Default)
 Low = Disable

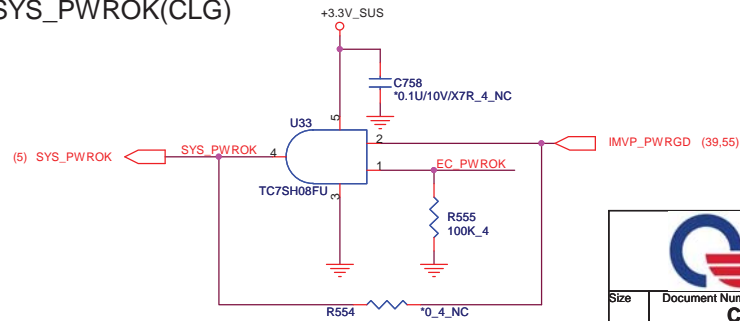
S3 Power reduce



S3 Power reduce

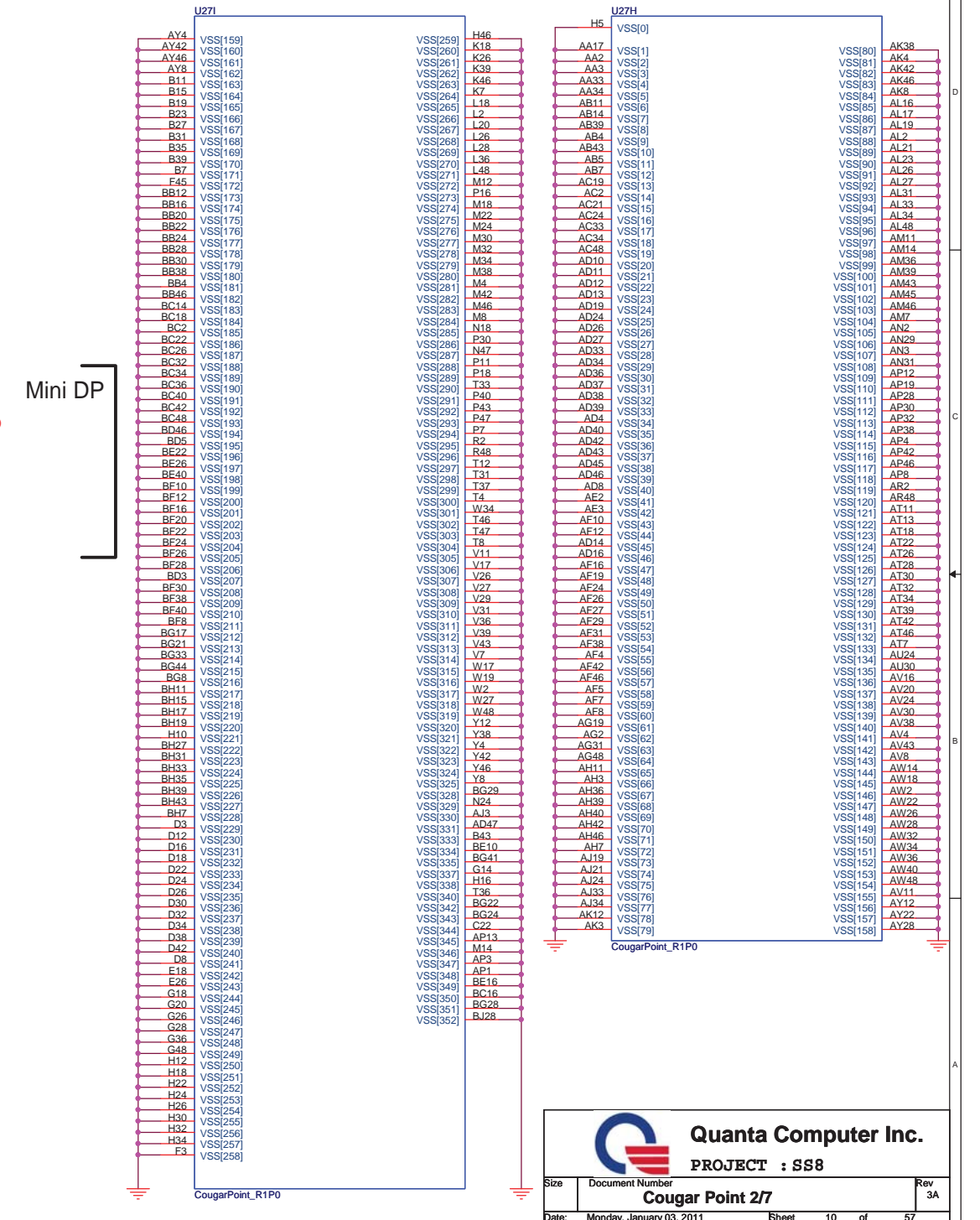
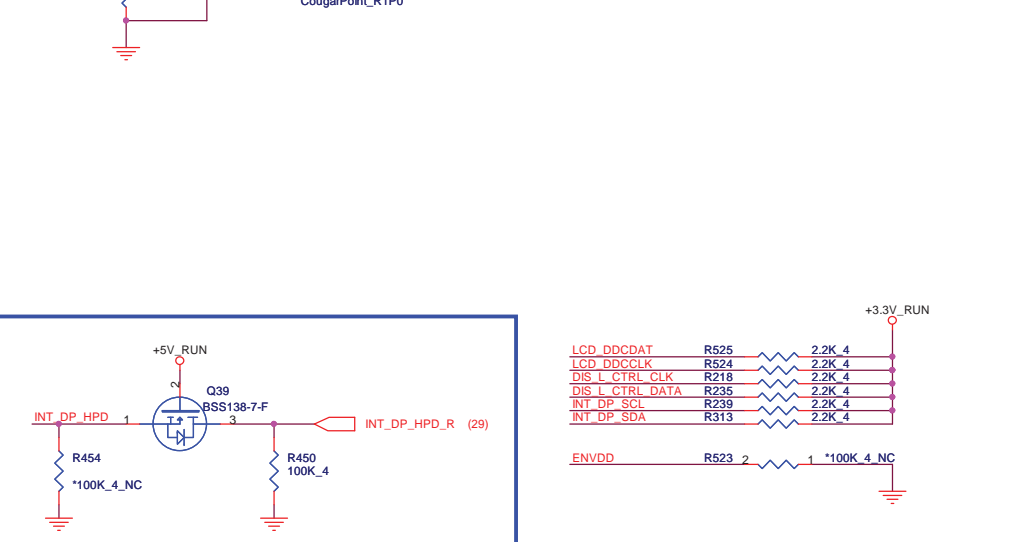
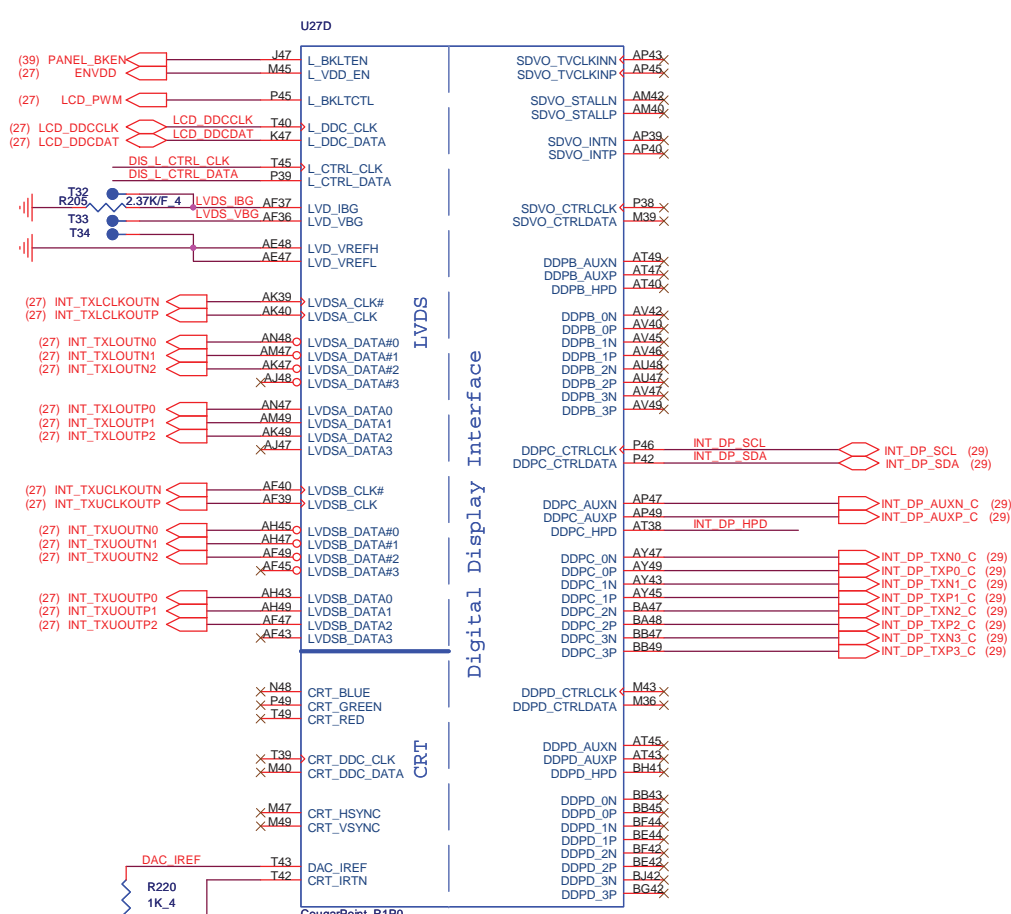



SYS_PWROK(CLG)



Cougar Point (LVDS, DDI)

Cougar Point (GND)





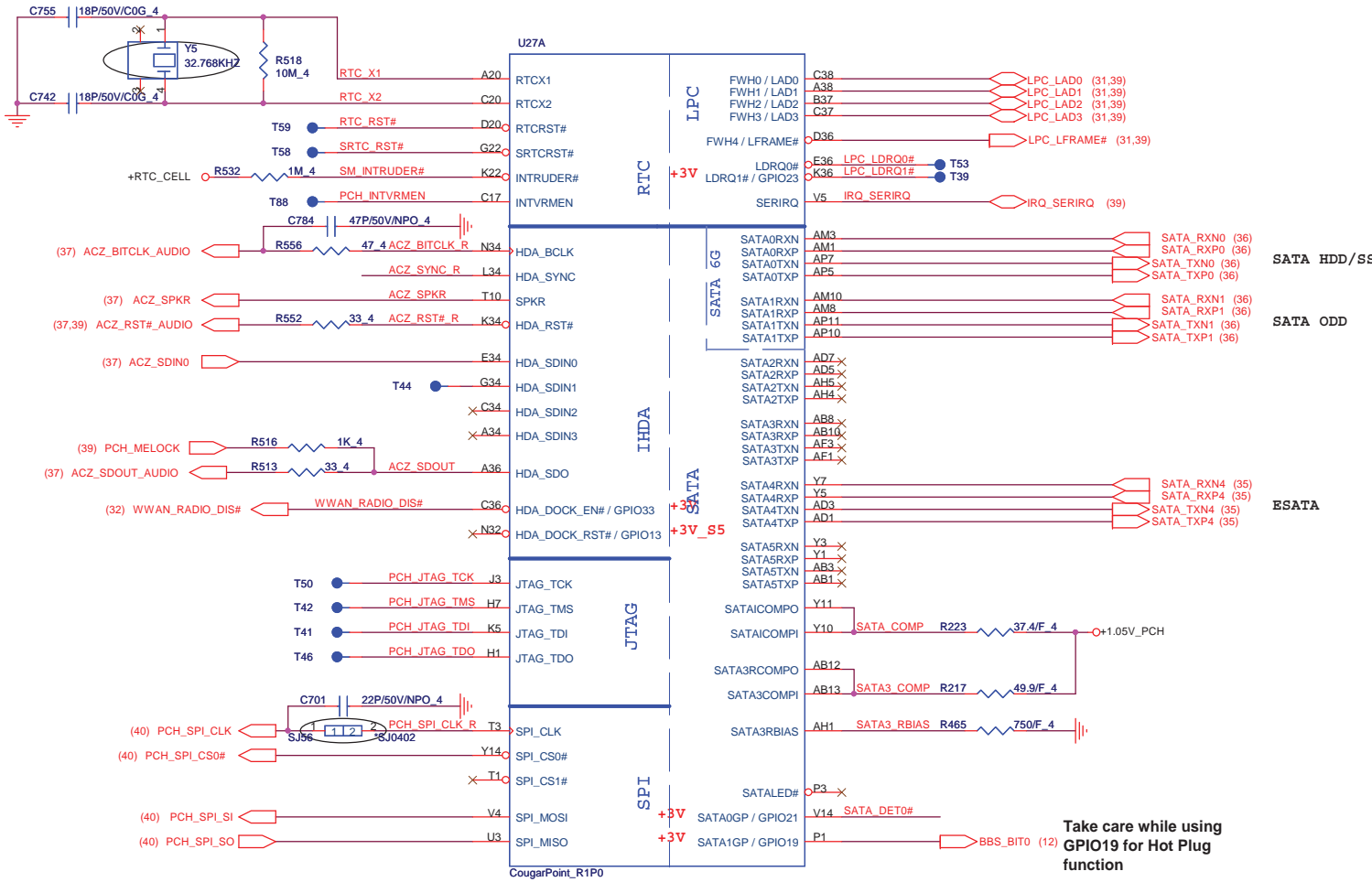
Quanta Computer Inc.

PROJECT : SS8

Cougar Point 2/7

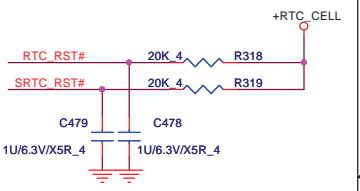
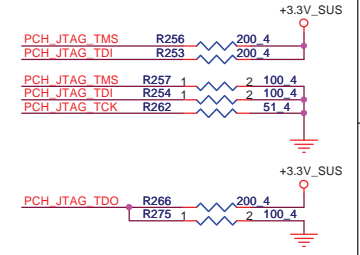
Size	Document Number	Rev	3A
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Cougar Point (HDA, JTAG, SATA)



Take care while using GPIO19 for Hot Plug function

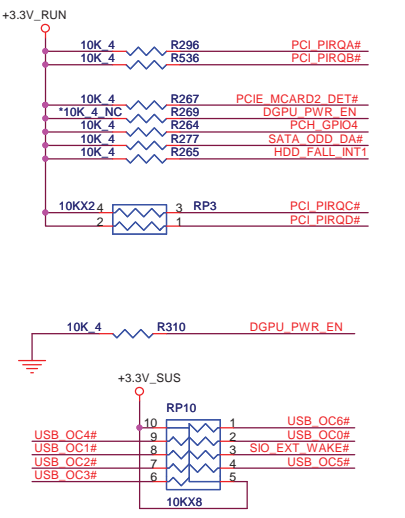
PCH JTAG Debug (CLG)



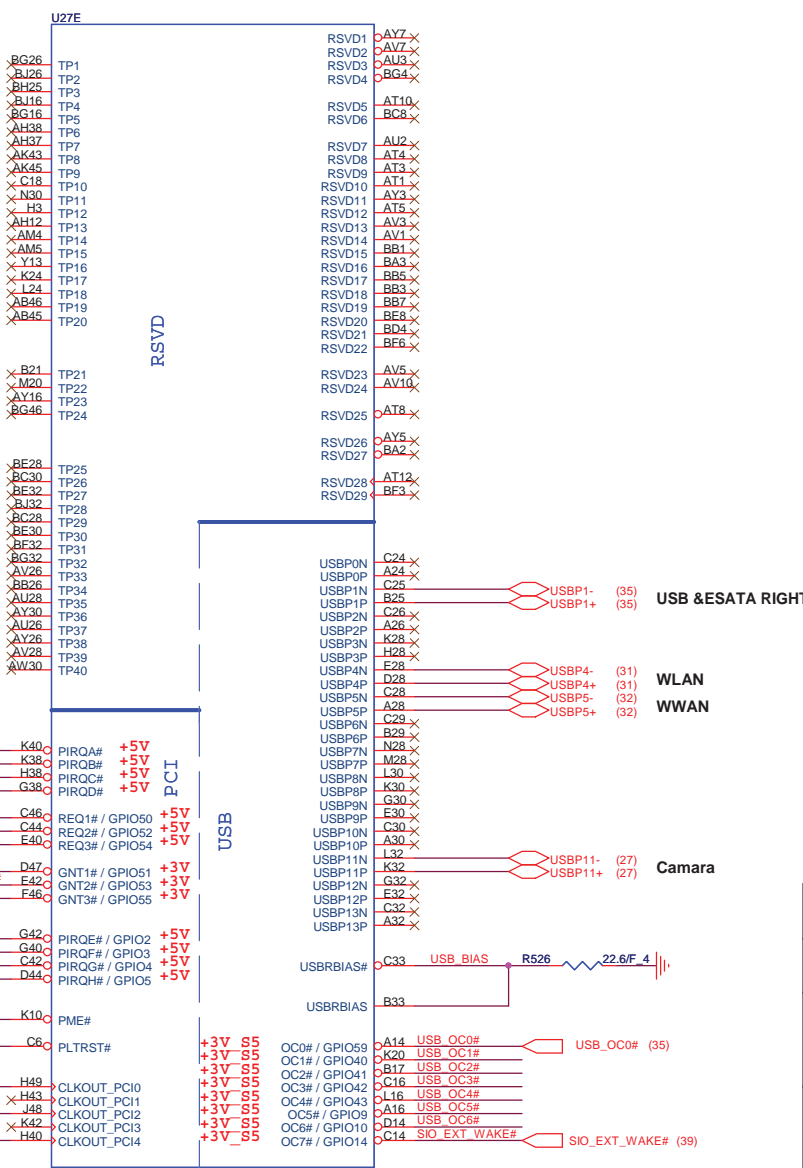
PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	note
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3.3V_RUN - R478 - 1K 4 NC - ACZ_SPKR
HDA_SDO	Flash Descriptor Security	PWROK	0 = Default (weak pull-down 20K) 1 = Override	+3.3V_SUS - R504 - 1K 4 NC - ACZ_SDOUT
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+RTC_CELL - R548 - 330K 4 - PCH_INTVRMEN
HDA_SYNC	On-Die PLL VR Volatge Select	RSMRST	0 = Support by 1.8V (weak PD) 1 = Support by 1.5V	(37) ACZ_SYNC_AUDIO - R537 - 33 4 - ACZ_SYNC_R - +3.3V_SUS

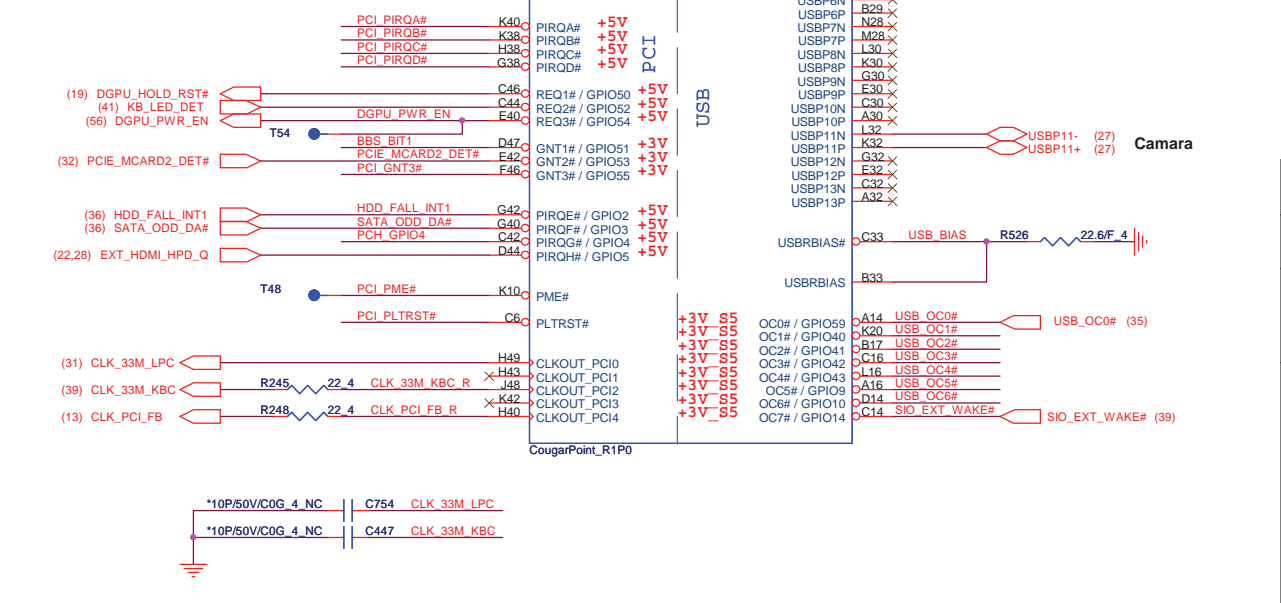
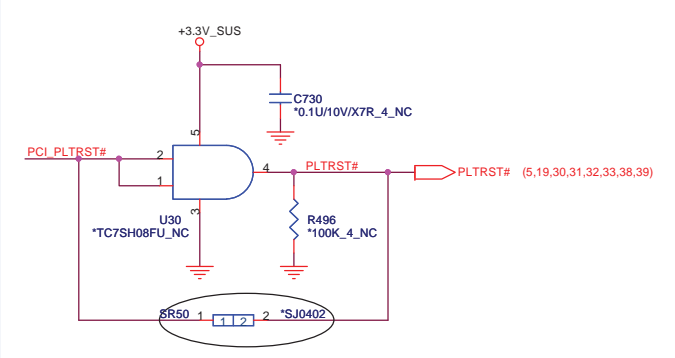
PCI/USB/OC# Pull-up(CLG)



Cougar Point-M (PCI,USB,NVRAM)



PLTRST#(CLG)



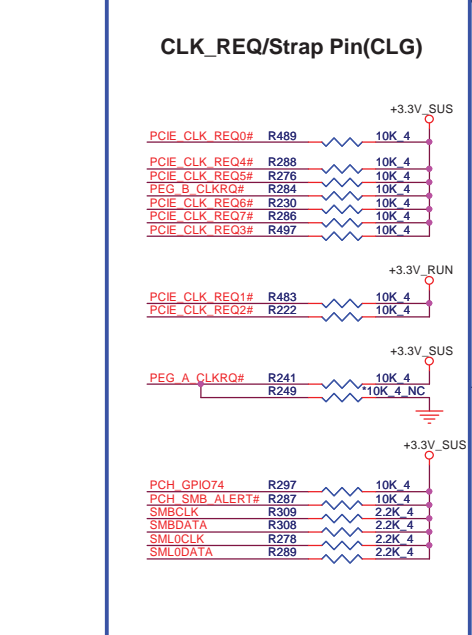
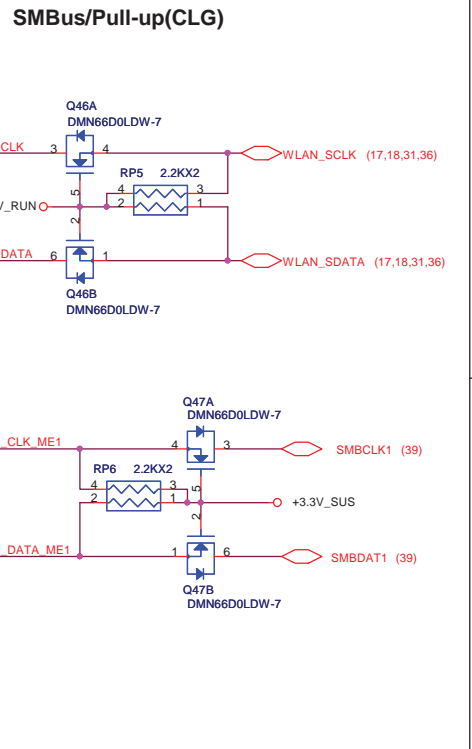
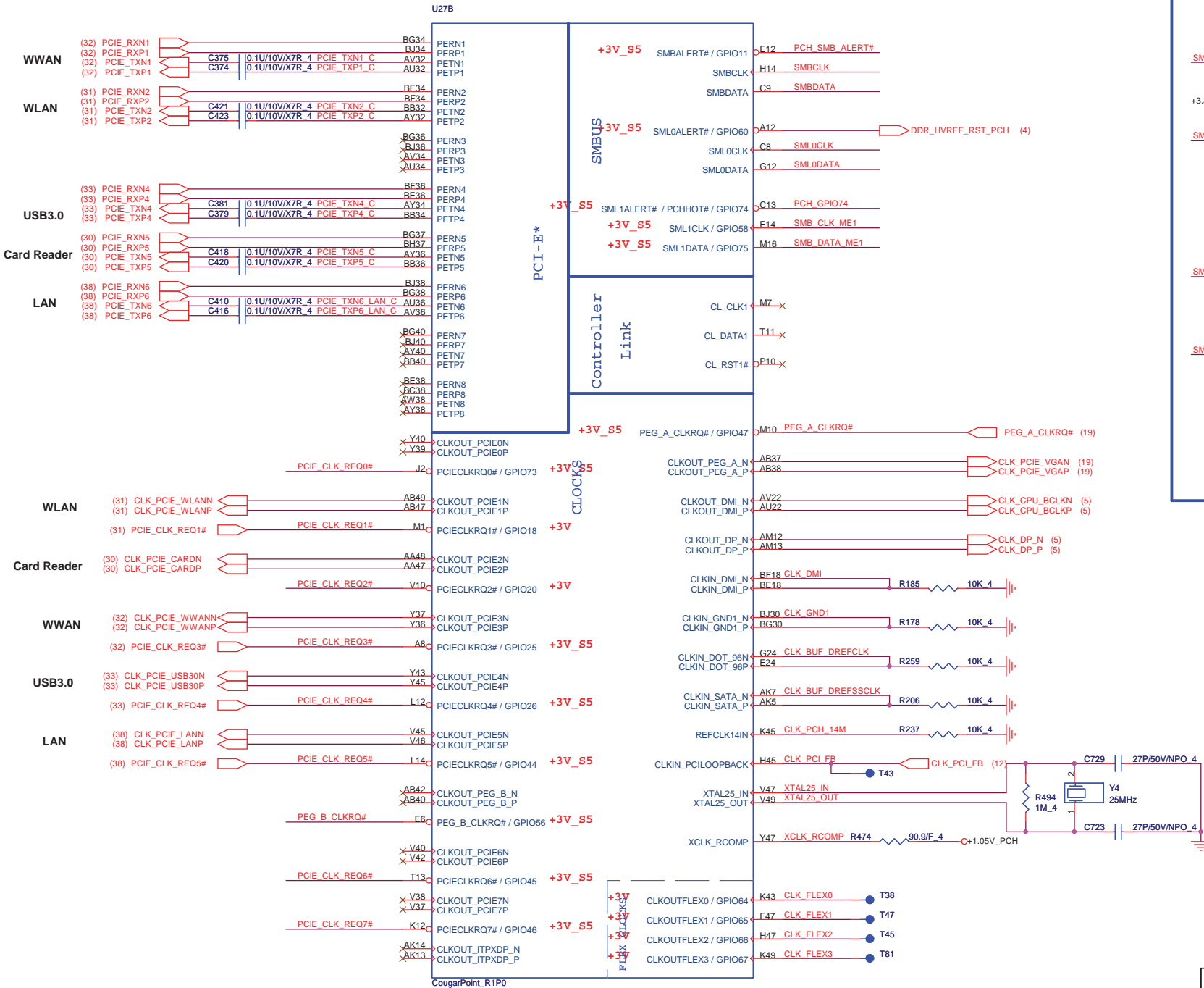
Pin Name	Strap description	Sampled	Configuration									
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)									
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)									
R533 *1K_4_NC PCI_GNT3#												
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	<table border="1"> <thead> <tr> <th>Bit 0</th> <th>Bit 1</th> <th>Boot Location</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>1</td> <td>SPI *</td> </tr> <tr> <td>0</td> <td>0</td> <td>LPC</td> </tr> </tbody> </table>	Bit 0	Bit 1	Boot Location	1	1	SPI *	0	0	LPC
Bit 0	Bit 1	Boot Location										
1	1	SPI *										
0	0	LPC										
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK										




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	Cougar Point 4/7	3A
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Cougar Point-M (PCI-E, SMBUS, CLK)



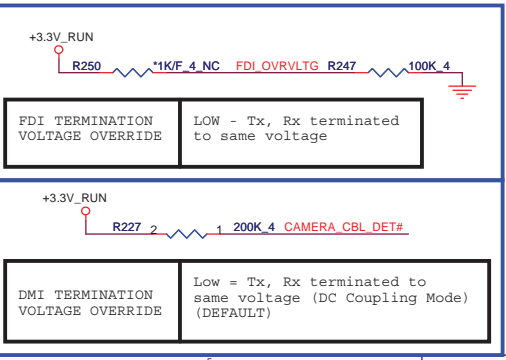
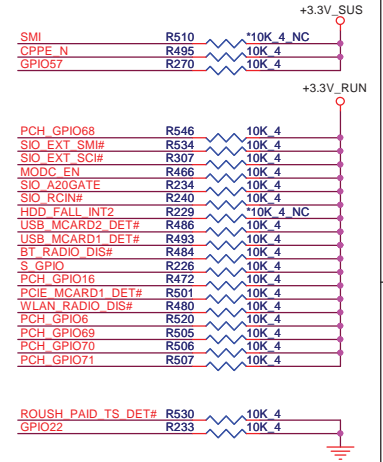
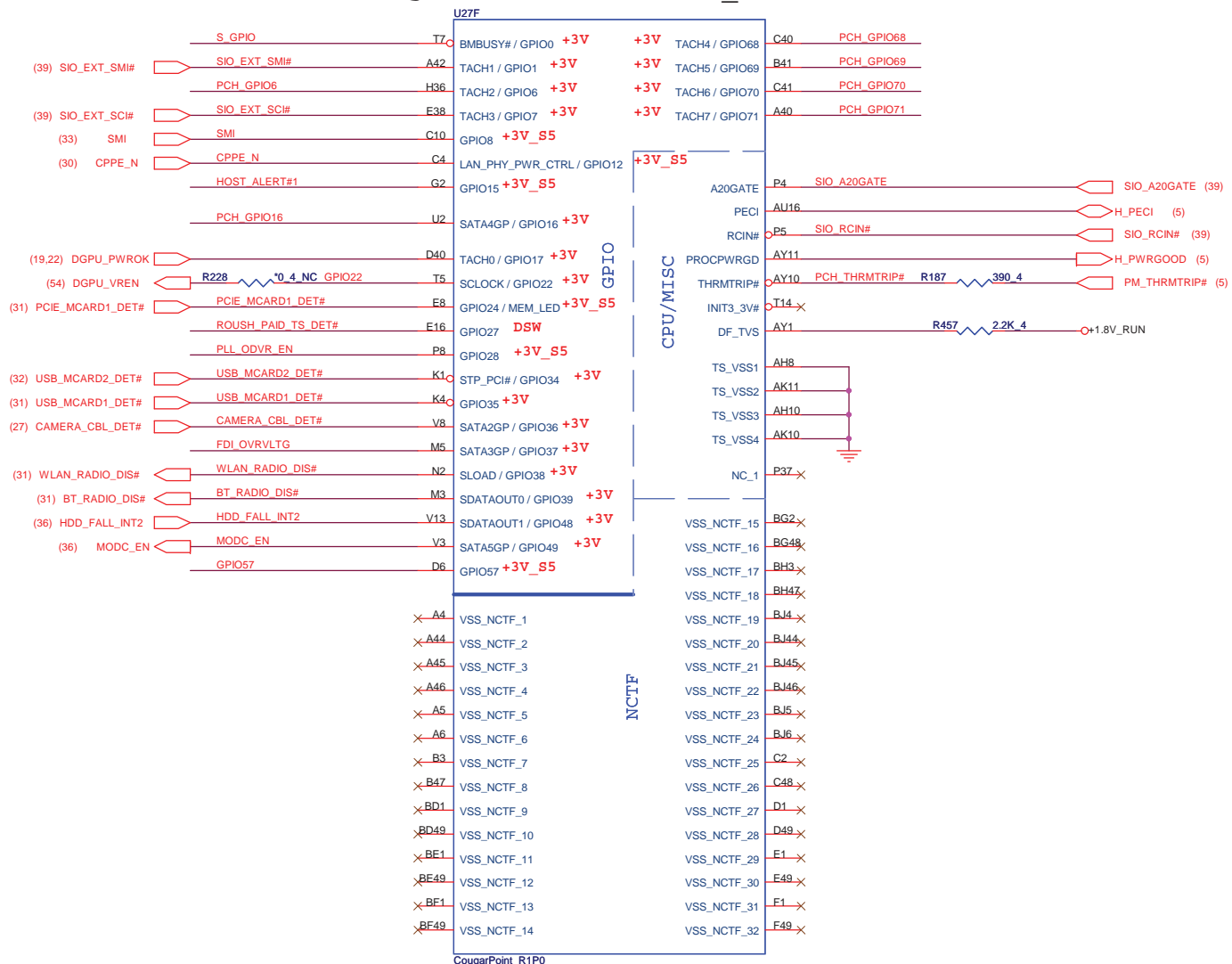


Quanta Computer Inc.
PROJECT : SS8


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Cougar Point (GPIO, VSS_NCTF, RSVD)

GPIO Pull-up/Pull-down (CLG)

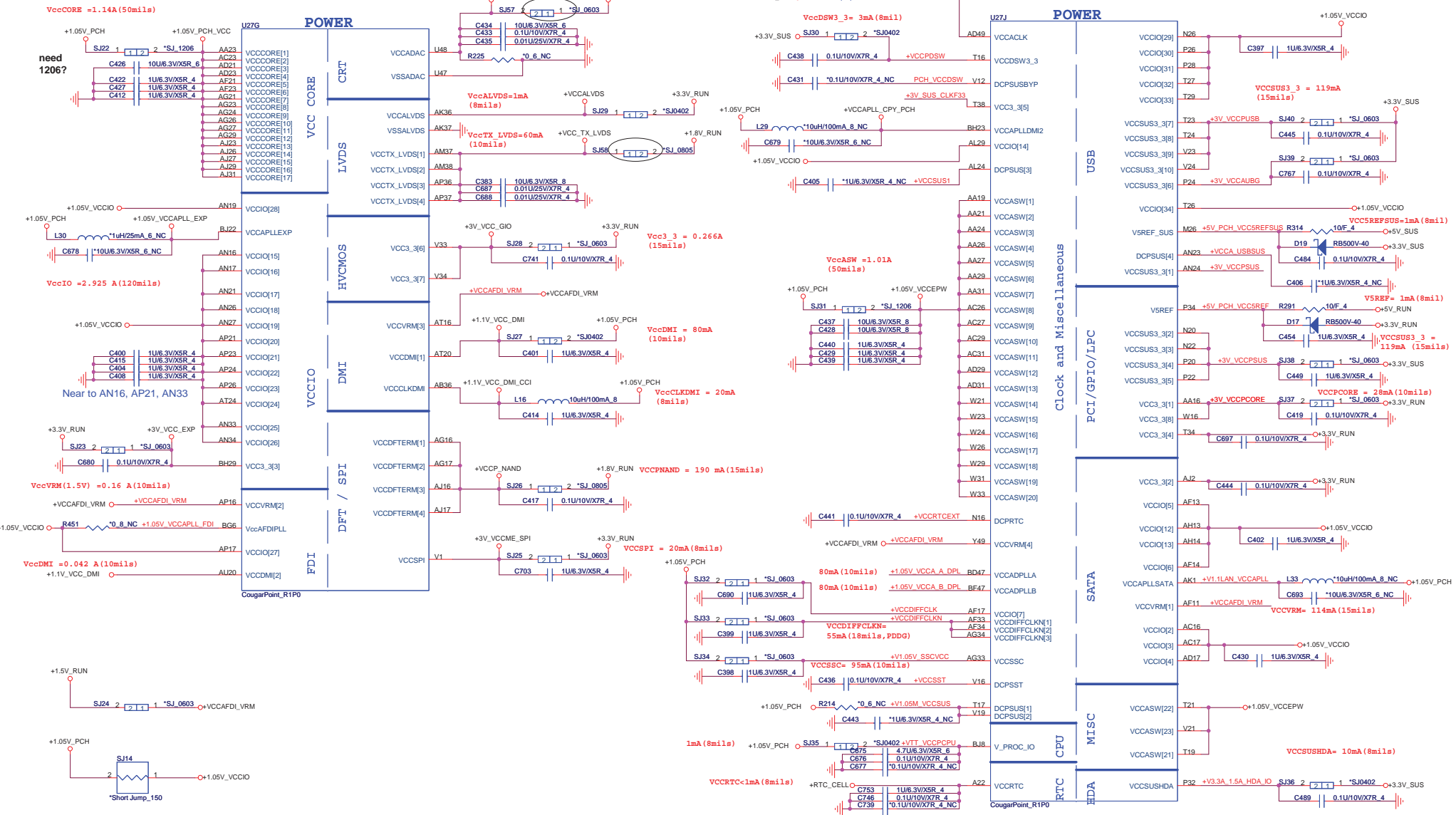


Pin Name	Strap description	Sampled	Configuration
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)
GPIO15	Intel ME Crypto Transport Layer Security (TLS) cipher suite	RSMRST#	0 = Disable (Default) 1 = Enable


Quanta Computer Inc.
PROJECT : SS8
Cougar Point 6/7
 Date: Monday, January 03, 2011 Sheet 14 of 57 Rev 3A

COUGAR POINT (POWER)

Cougar Point (POWER)





5

4

3

2

1

D

D

C


C

B

B

A

A

		Quanta Computer Inc.
		PROJECT : SS8
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5

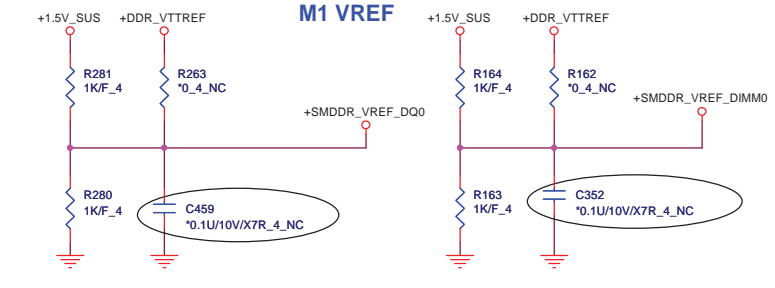
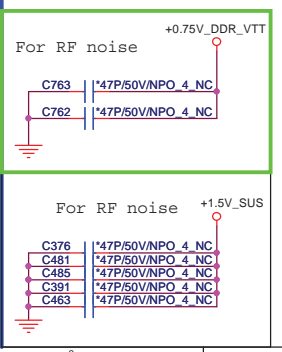
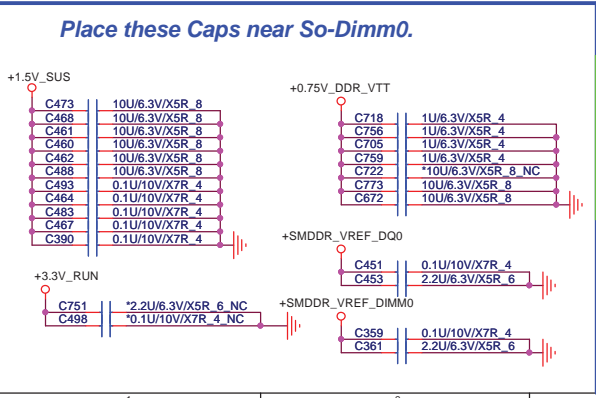
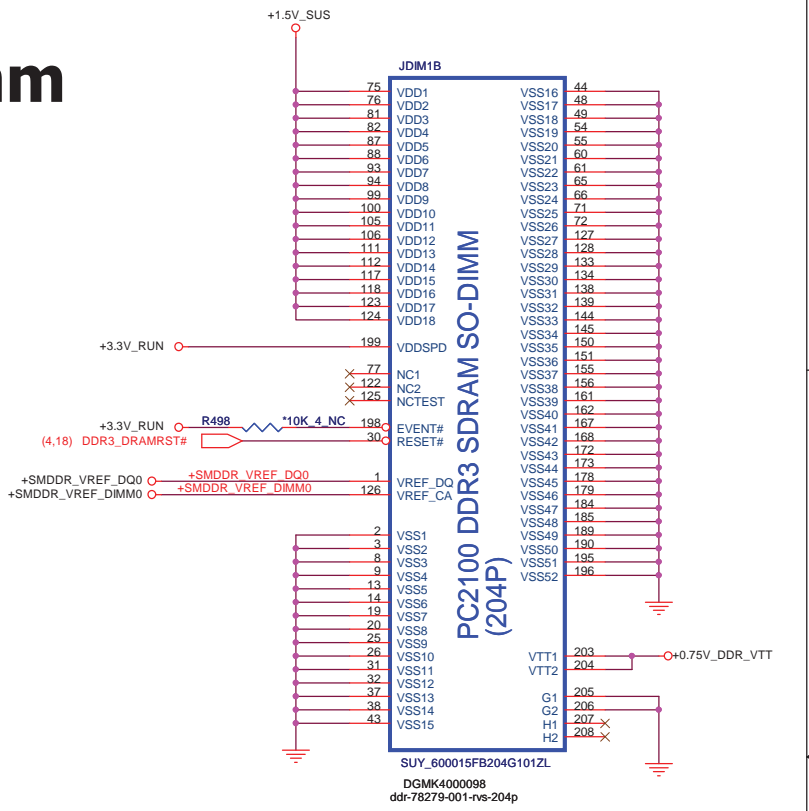
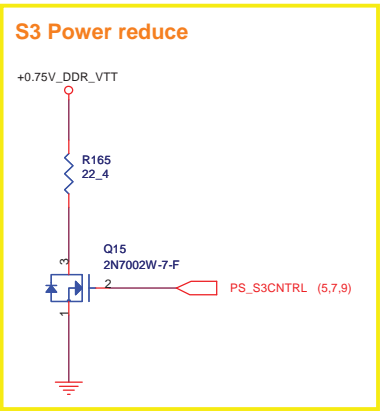
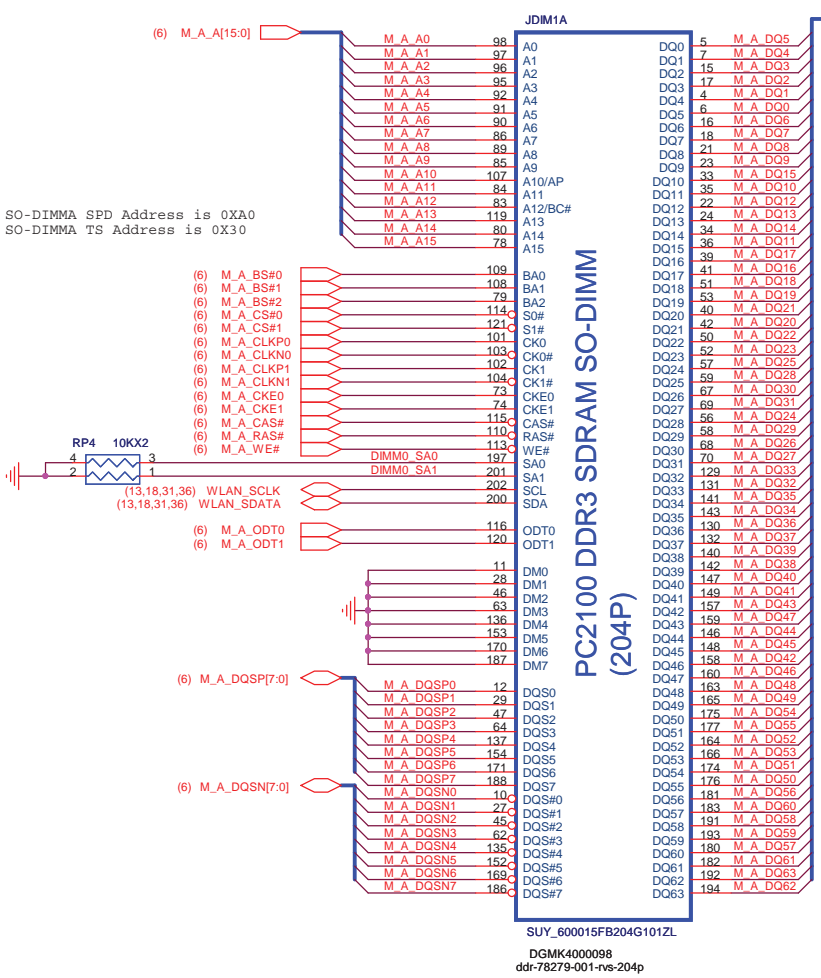
4

3

2

1

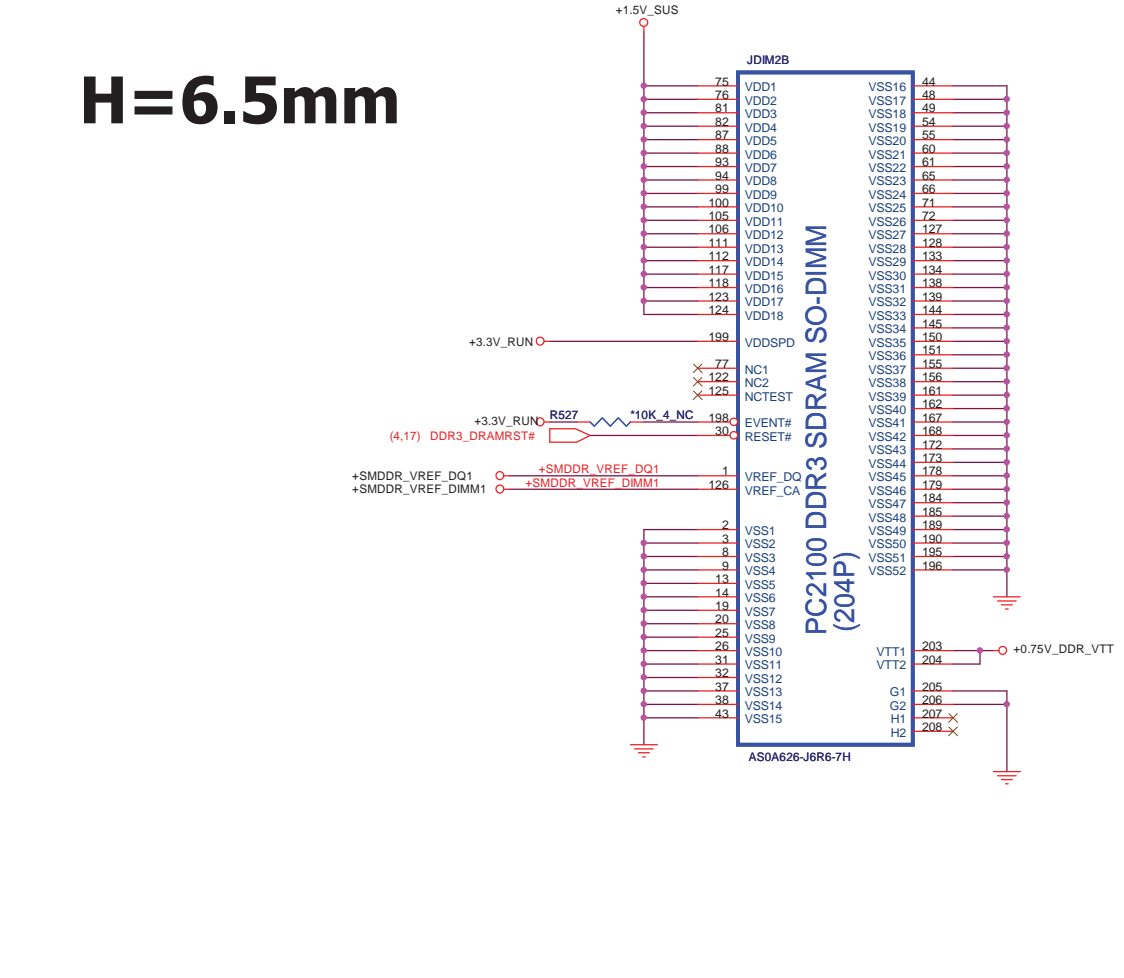
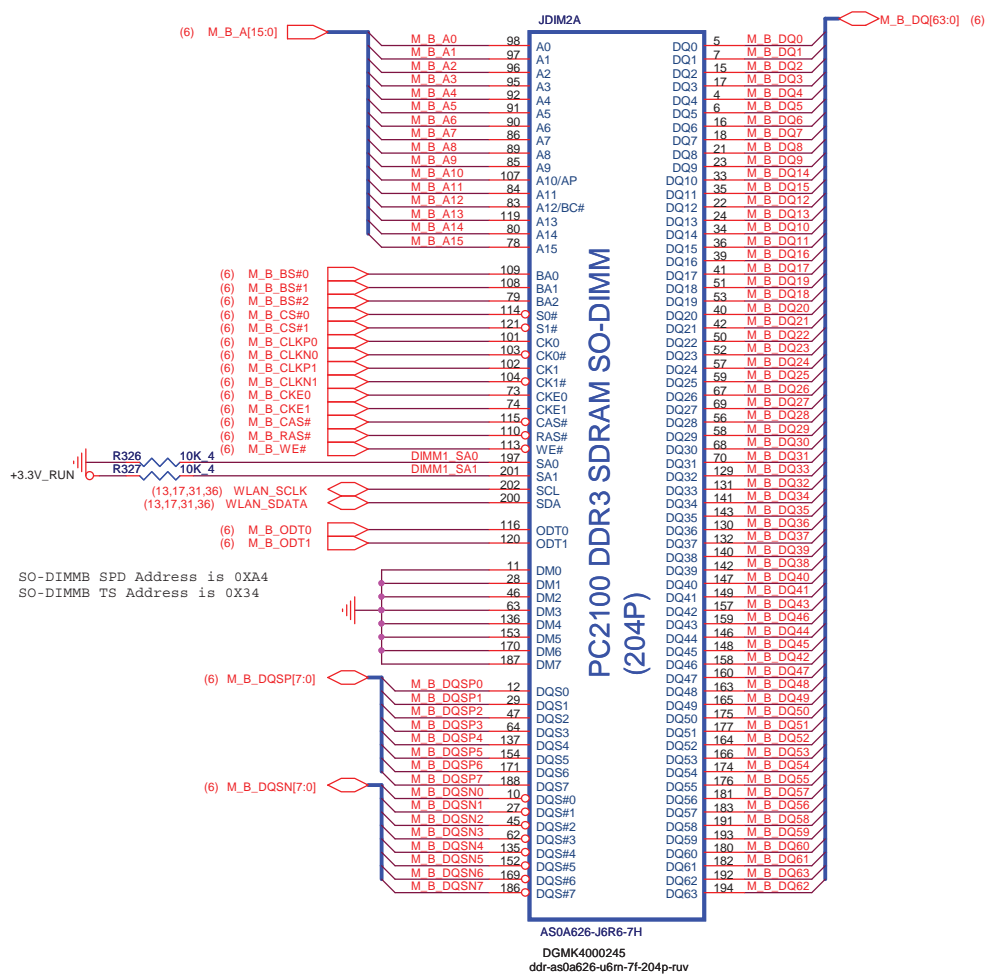
H=5.2mm



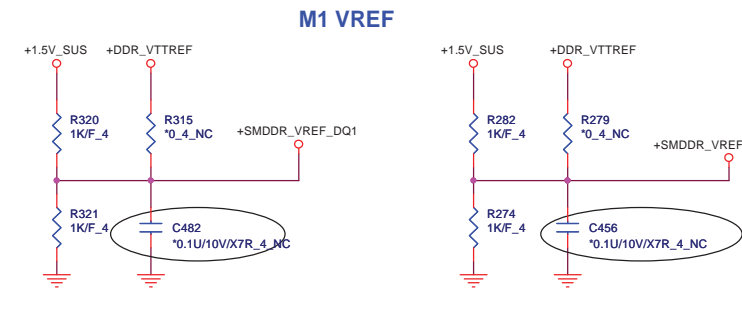
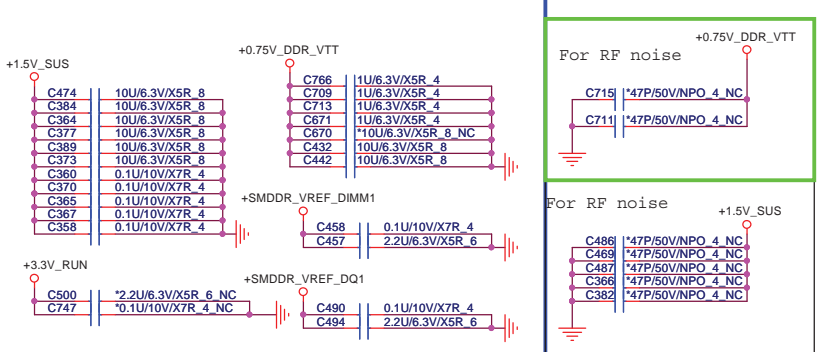
Quanta Computer Inc.
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DDR3 DIMM-0		
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H=6.5mm



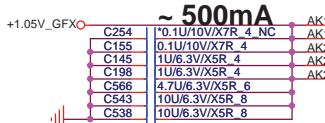
Place these Caps near So-Dimm1.



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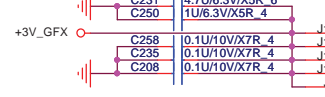
Size	Document Number	Rev
	DDR3 DIMM-1	3A
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PEX_IOVDD+PEX_IOVDDQ >2.2A



0.1u *4 under GPU
Others Near GPU

0.1u under GPU
Others Near GPU



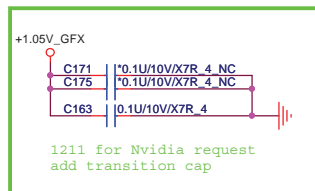
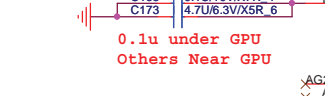
12~16 mils width
120mA

0.1u under GPU
Others Near GPU



120mA 12~16 mils width

0.1u under GPU
Others Near GPU



1211 for Nvidia request
add transition cap

U22A
N12P-GE

- PEX_IOVDD_1
- PEX_IOVDD_2
- PEX_IOVDD_3
- PEX_IOVDD_4
- PEX_IOVDD_5
- PEX_IOVDDQ_1
- PEX_IOVDDQ_2
- PEX_IOVDDQ_3
- PEX_IOVDDQ_4
- PEX_IOVDDQ_5
- PEX_IOVDDQ_6
- PEX_IOVDDQ_7
- PEX_IOVDDQ_8
- PEX_IOVDDQ_9
- PEX_IOVDDQ_10
- PEX_IOVDDQ_11
- PEX_IOVDDQ_12
- PEX_IOVDDQ_13
- PEX_IOVDDQ_14
- PEX_IOVDDQ_15
- PEX_IOVDDQ_16
- PEX_IOVDDQ_17
- PEX_IOVDDQ_18
- PEX_IOVDDQ_19
- PEX_IOVDDQ_20
- PEX_IOVDDQ_21
- PEX_IOVDDQ_22
- PEX_IOVDDQ_23
- PEX_IOVDDQ_24
- PEX_IOVDDQ_25

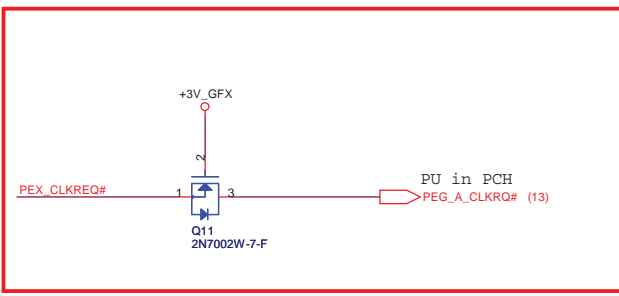
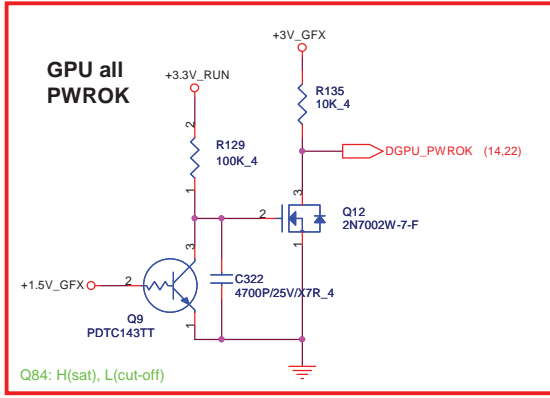
PCI EXPRESS

- VDD33_1
- VDD33_2
- VDD33_3
- VDD33_4
- VDD33_5
- VDD_SENSE
- NC_9/ VDD_SENSE
- NC_16/ VDD_SENSE
- GND_SENSE
- NC_10/ GND_SENSE
- NC_17/ GND_SENSE
- PEX_PLLVDD
- PEX_CAL_PD_VDDQ/ PEX_SVDD_3V3
- NC_12/ PEX_SVDD_3V3
- PEX_PLL_HVDD_NC
- NC_1
- NC_2
- NC_3
- NC_4
- NC_5
- NC_6
- NC_7
- NC_8
- NC_11
- NC_13
- NC_15
- NC_18
- NC_19

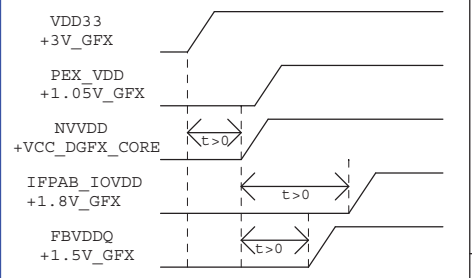
- AP17 PEG_TXP15
- AN17 PEG_TXN15
- AN19 PEG_TXP14
- AP19 PEG_TXN14
- AR19 PEG_TXP13
- AR20 PEG_TXN13
- AN20 PEG_TXP12
- AN22 PEG_TXN12
- AP22 PEG_TXP11
- AR22 PEG_TXN11
- AR23 PEG_TXP10
- AP23 PEG_TXN10
- AP23 PEG_TXP9
- AN23 PEG_TXN9
- AR25 PEG_TXP8
- AP25 PEG_TXN8
- AR25 PEG_TXP7
- AP25 PEG_TXN7
- AR26 PEG_TXP6
- AP26 PEG_TXN6
- AN26 PEG_TXP5
- AR26 PEG_TXN5
- AR28 PEG_TXP4
- AN28 PEG_TXN4
- AP29 PEG_TXP3
- AN29 PEG_TXN3
- AN31 PEG_TXP2
- AP31 PEG_TXN2
- AR31 PEG_TXP1
- AN31 PEG_TXN1
- AR32 PEG_TXP0
- AN32 PEG_TXN0
- AP34 PEG_TXP0
- AN34 PEG_TXN0

- AL17 PEG_RXP15 C C221
- AM17 PEG_RXN15 C C206
- AM18 PEG_RXP14 C C186
- AM19 PEG_RXN14 C C174
- AL18 PEG_RXP13 C C198
- AL20 PEG_RXP12 C C167
- AM20 PEG_RXN12 C C162
- AM21 PEG_RXP11 C C157
- AM22 PEG_RXN11 C C150
- AL22 PEG_RXP10 C C172
- AK22 PEG_RXN10 C C164
- AL23 PEG_RXP9 C C149
- AM23 PEG_RXN9 C C144
- AM24 PEG_RXP8 C C140
- AM25 PEG_RXN8 C C130
- AL25 PEG_RXP7 C C127
- AK25 PEG_RXN7 C C125
- AL28 PEG_RXP6 C C119
- AM26 PEG_RXN6 C C114
- AM27 PEG_RXP5 C C112
- AM28 PEG_RXN5 C C109
- AL28 PEG_RXP4 C C107
- AK28 PEG_RXN4 C C102
- AK29 PEG_RXP3 C C100
- AL29 PEG_RXN3 C C97
- AM29 PEG_RXP2 C C96
- AM30 PEG_RXN2 C C92
- AM31 PEG_RXP1 C C91
- AM32 PEG_RXN1 C C88
- AN32 PEG_RXP0 C C89
- AP32 PEG_RXN0 C C84
- PEX_TX0
- PEX_TX0*
- PEX_TX1
- PEX_TX1*
- PEX_TX2
- PEX_TX2*
- PEX_TX3
- PEX_TX3*
- PEX_TX4
- PEX_TX4*
- PEX_TX5
- PEX_TX5*
- PEX_TX6
- PEX_TX6*
- PEX_TX7
- PEX_TX7*
- PEX_TX8
- PEX_TX8*
- PEX_TX9
- PEX_TX9*
- PEX_TX10
- PEX_TX10*
- PEX_TX11
- PEX_TX11*
- PEX_TX12
- PEX_TX12*
- PEX_TX13
- PEX_TX13*
- PEX_TX14
- PEX_TX14*
- PEX_TX15
- PEX_TX15*
- PEX_TX16*
- PEX_TX17*
- PEX_TX18*
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- PEX_TX24*
- PEX_TX25*

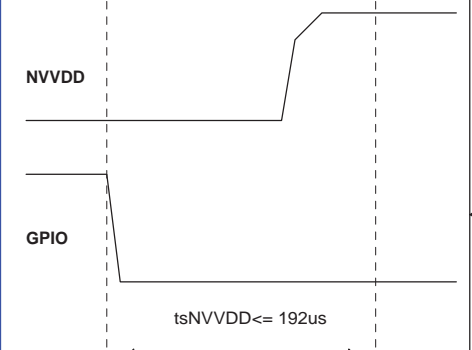
- AR16 CLK_PCIE_VGAP
- AR17 CLK_PCIE_VGAN
- AL17 PEX_TSTCLK R77
- AL18 PEX_TSTCLK#
- AM16 GPU_RST#
- AR13 PEX_CLKREQ#
- AG21 PEX_TERM
- AP35 TESTMODE



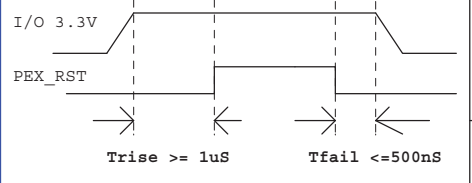
Power up sequence

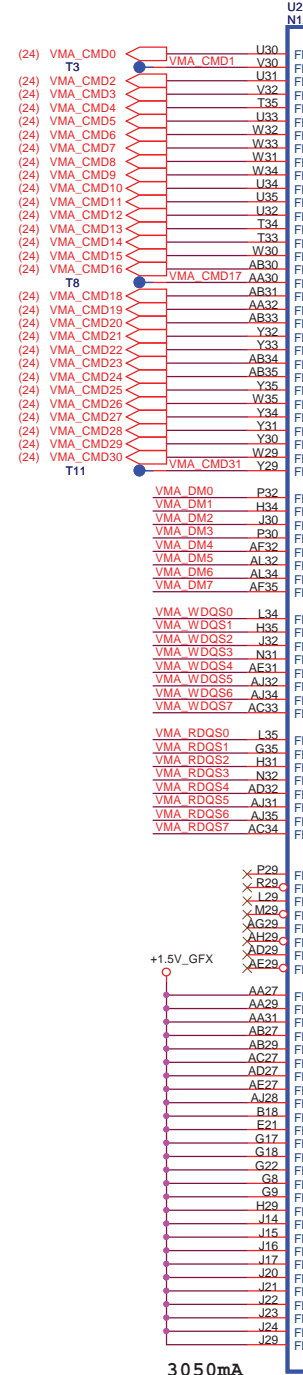


NB9M: VGACORE +0.90V (Normal), +1.09V
NVVDD Maximum Settling Time

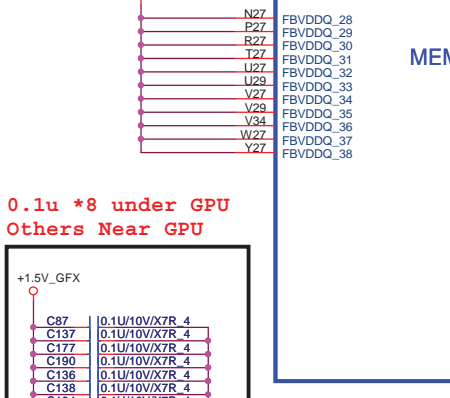
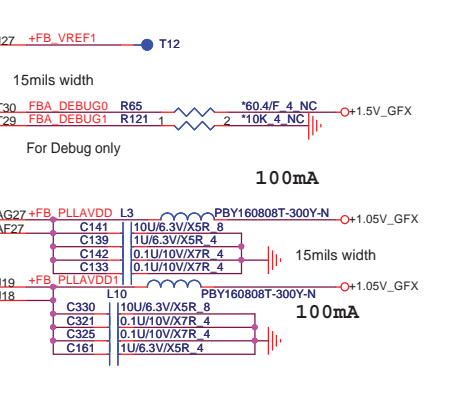
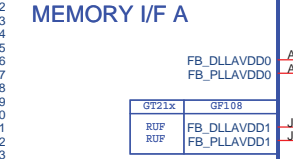
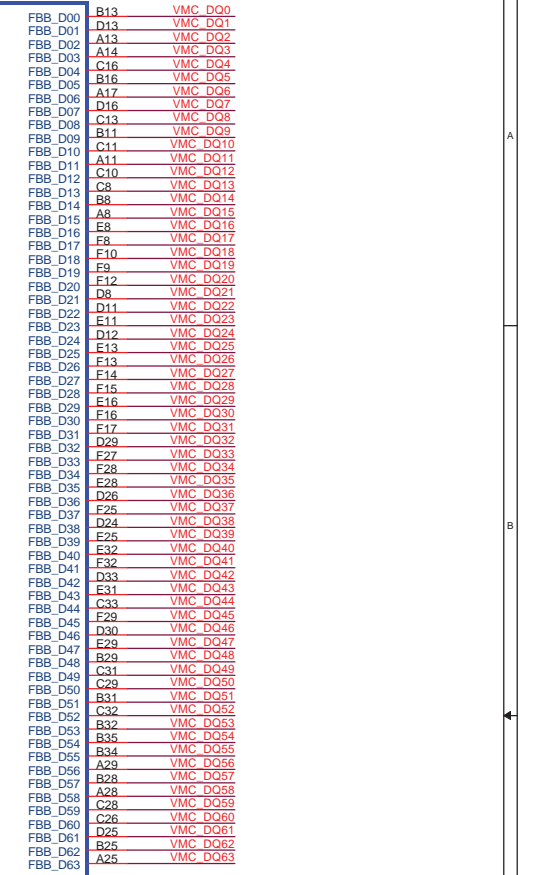
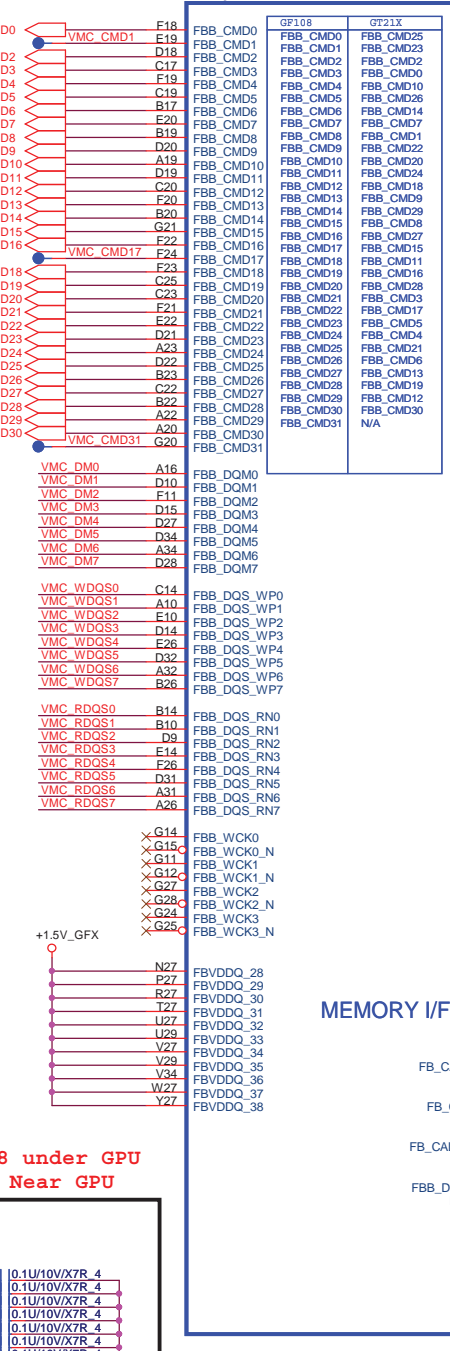
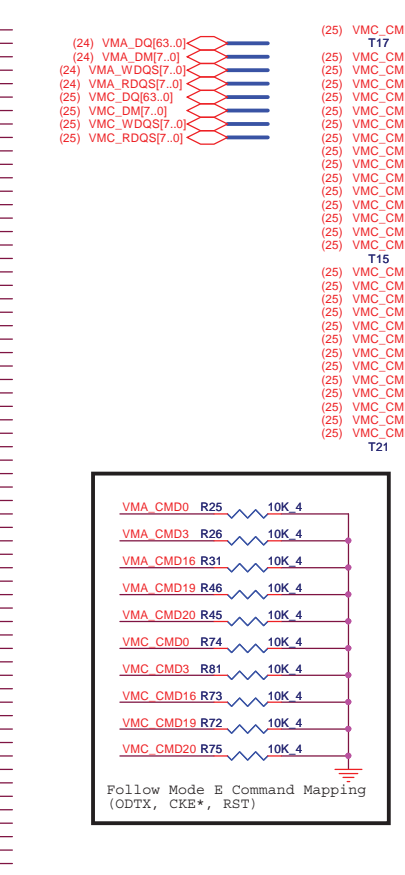


PEX_RST timing

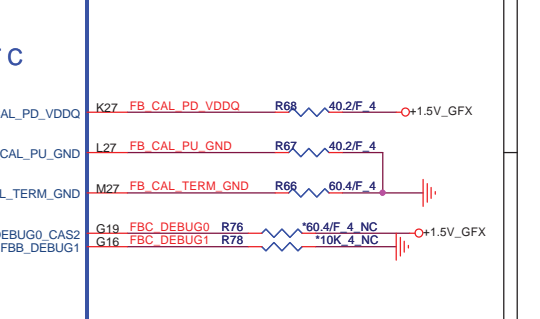





GF108	GF21X
FBA_CMD0	FBA_CMD25
FBA_CMD1	FBA_CMD23
FBA_CMD2	FBA_CMD2
FBA_CMD3	FBA_CMD3
FBA_CMD4	FBA_CMD10
FBA_CMD5	FBA_CMD26
FBA_CMD6	FBA_CMD14
FBA_CMD7	FBA_CMD7
FBA_CMD8	FBA_CMD1
FBA_CMD9	FBA_CMD22
FBA_CMD10	FBA_CMD20
FBA_CMD11	FBA_CMD18
FBA_CMD12	FBA_CMD11
FBA_CMD13	FBA_CMD9
FBA_CMD14	FBA_CMD29
FBA_CMD15	FBA_CMD8
FBA_CMD16	FBA_CMD27
FBA_CMD17	FBA_CMD15
FBA_CMD18	FBA_CMD11
FBA_CMD19	FBA_CMD16
FBA_CMD20	FBA_CMD28
FBA_CMD21	FBA_CMD3
FBA_CMD22	FBA_CMD17
FBA_CMD23	FBA_CMD5
FBA_CMD24	FBA_CMD4
FBA_CMD25	FBA_CMD21
FBA_CMD26	FBA_CMD6
FBA_CMD27	FBA_CMD13
FBA_CMD28	FBA_CMD19
FBA_CMD29	FBA_CMD12
FBA_CMD30	FBA_CMD30
FBA_CMD31	N/A



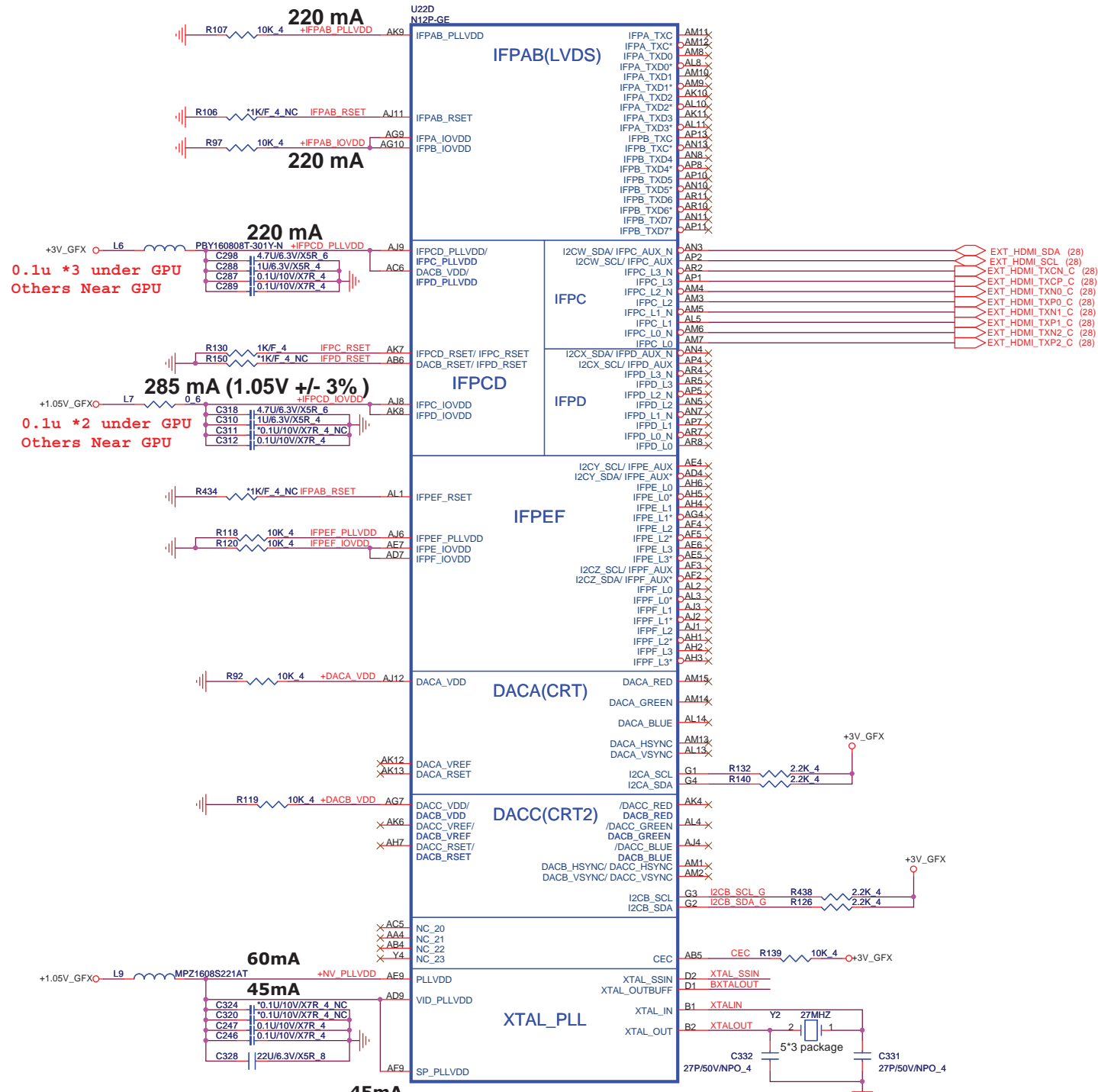
MEMORY I/F C

Quanta Computer Inc.
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Size	Document Number	Rev
	N12P-GE (MEMORY I/F) 2/5	3A

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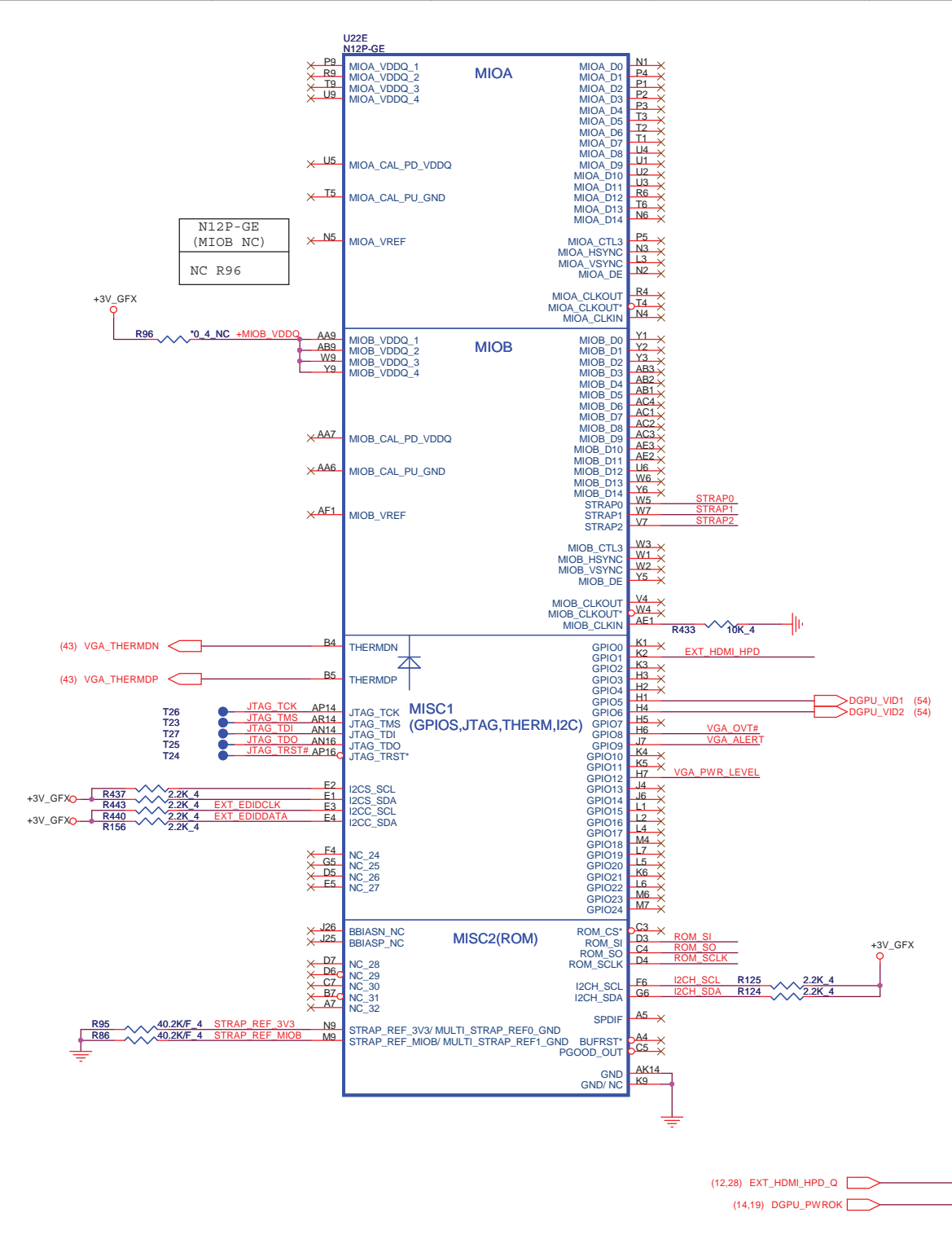


XTAL SSIN R435 10K 4
 BXTALOUT R442 10K 4

70 kΩ pull-down only if no spread chip used.

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Size	Document Number	Rev
	N12P-GE (DISPLAY) 3/5	3A
Date:	Monday, January 03, 2011	Sheet 21 of 57

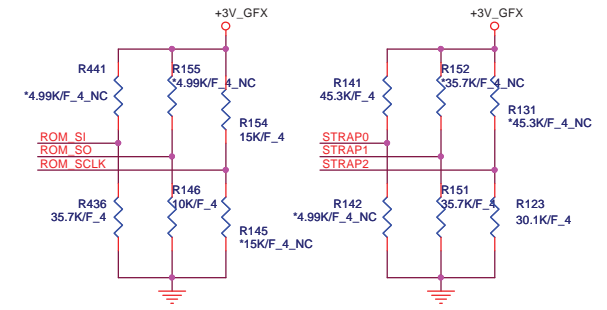


CHIP	PCI_DEVID:	STRAP2	ROM_SCLK
N12P-GE	0xDF5	0101 PD 30K	1010 PU 15K

Default: N12P-GE

Logical Strap Bit Mapping

	PU-VDD	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111



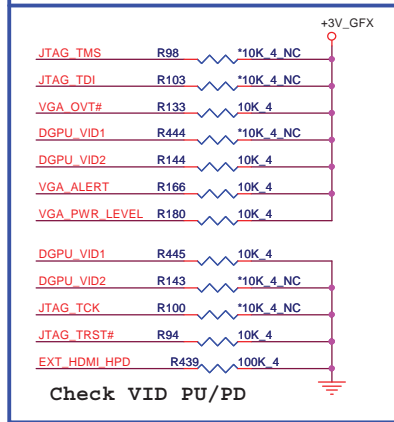
10K/F 4: CS31002FB26 [RES CHIP 10K 1/16W +1% (0402)]
 15K/F 4: CS34992FB26 [RES CHIP 15K 1/16W +1% (0402)]
 20K/F 4: CS31502FB24 [RES CHIP 20K 1/16W +1% (0402)]
 25K/F 4: CS32002FB29 [RES CHIP 25K 1/16W +1% (0402)]
 30.1K/F 4: CS33012FB18 [RES CHIP 30.1K 1/16W +1% (0402)]
 35.7K/F 4: CS33572FB13 [RES CHIP 35.7K 1/16W +1% (0402)]
 45.3K/F 4: CS34532FB18 [RES CHIP 45.3K 1/16W +1% (0402)]

	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE	0001
ROM_SCLK	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM	1010
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	0110
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	0101
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0110
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111

Default: Hynix VRAM 2G (0110) VRAM Configuration Table

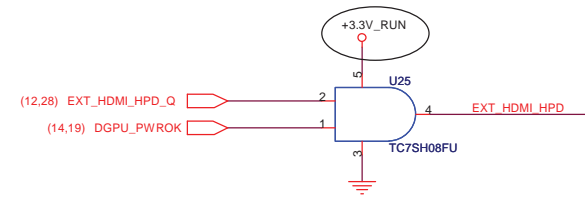
RAMCFG [3:0]	DESCRIPTION	Vendor	Quanta P/N	Vendor P/N	ROM_SI
0000		Reserved			PD 5K
0001		Reserved			PD 10K
0010	DDR3 64Mx16, 900MHz	Hynix	AKD5LZWTW02	H5TQ1G63DFR-11C	PD 15K
0011	DDR3 64Mx16, 900MHz	Samsung	AKD5LGH7500	K4W1G1646E-HC11	PD 20K
0110	DDR3 128Mx16, 900MHz	Hynix	AKD5MGWTW00	H5TQ2G63BFR-11C	PD 35K
0111	DDR3 128Mx16, 900MHz	Samsung	AKD5MGWT500	K4W2G1646C-HC11	PD 45K

GPIO ASSIGNMENTS



GPIO	I/O	ACTIVE	USAGE
0	N/A	N/A	
1	IN	N/A	Hot plug detect for IFP link C
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVDD VID0
6	OUT	N/A	NVDD VID1
7	OUT	N/A	NVDD VID2 ^{11/13}
8	I/O	LOW	OVERT
9	I/O	LOW	ALERT
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI SYNC0
12	IN	N/A	PWR_LEVEL ^{11/13}
13	OUT	N/A	MEM_VID or power supply control
14	OUT	N/A	PS CONTROL

Check VID PU/PD



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Size	Document Number	Rev
	N12P-GE (GPIO&STRAPS) 4/5	3A

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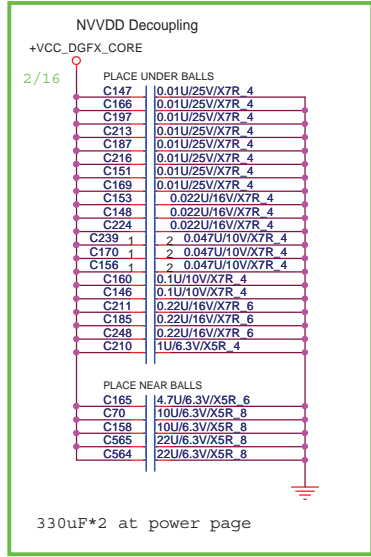
+VCC_DGFX_CORE

U22F N12P-GE		+VCC_DGFX_CORE	
AB11	VDD_001	P21	
AB13	VDD_002	P23	
AB15	VDD_003	P25	
AB17	VDD_004	R11	
AB19	VDD_005	R12	
AB21	VDD_006	R13	
AB23	VDD_007	R14	
AB25	VDD_008	R15	
AC11	VDD_009	R16	
AC12	VDD_010	R17	
AC13	VDD_011	R18	
AC14	VDD_012	R19	
AC15	VDD_013	R20	
AC16	VDD_014	R21	
AC17	VDD_015	R22	
AC18	VDD_016	R23	
AC19	VDD_017	R24	
AC20	VDD_018	R25	
AC21	VDD_019	T12	
AC22	VDD_020	T14	
AC23	VDD_021	T16	
AC24	VDD_022	T18	
AC25	VDD_023	T20	
AD12	VDD_024	T22	
AD14	VDD_025	T24	
AD16	VDD_026	V11	
AD18	VDD_027	V13	
AD22	VDD_028	V15	
AD24	VDD_029	V17	
L11	VDD_030	V19	
L12	VDD_031	V21	
L13	VDD_032	V23	
L14	VDD_033	V25	
L15	VDD_034	W11	
L16	VDD_035	W12	
L17	VDD_036	W13	
L18	VDD_037	W14	
L19	VDD_038	W15	
L20	VDD_039	W16	
L21	VDD_040	W18	
L22	VDD_041	W19	
L23	VDD_042	W20	
L24	VDD_043	W22	
L25	VDD_044	W24	
M12	VDD_045	W26	
M14	VDD_046	W28	
M16	VDD_047	W30	
M18	VDD_048	W32	
M20	VDD_049	W34	
M22	VDD_050	Y14	
M24	VDD_051	Y16	
P11	VDD_052	Y18	
P13	VDD_053	Y20	
P15	VDD_054	Y22	
P17	VDD_055	Y24	
P19	VDD_056	Y26	

NVVDD

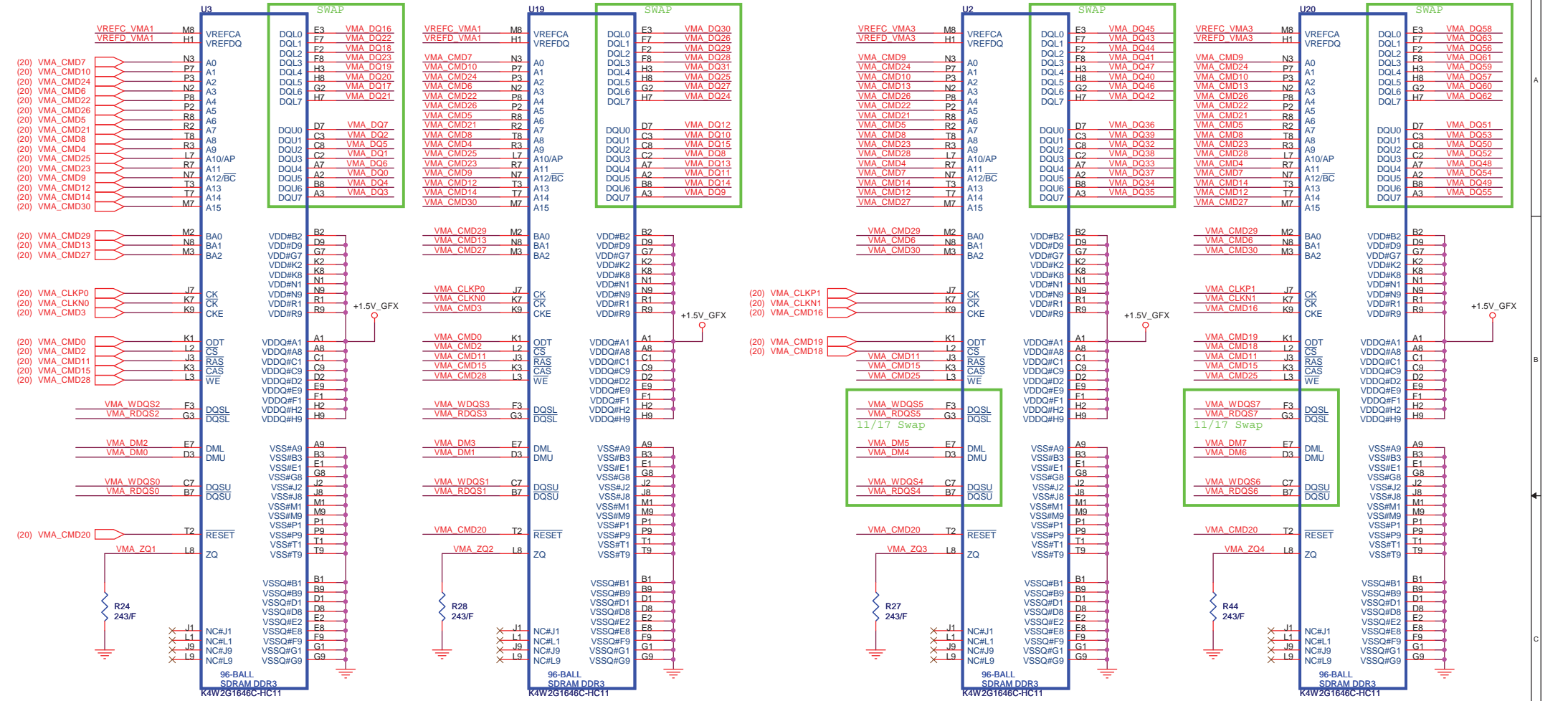
U22G
N12P-GE


U22G N12P-GE		GROUND	
AA11	GND_1	GND_096	E15
AA12	GND_2	GND_097	E18
AA13	GND_3	GND_098	E24
AA14	GND_4	GND_099	E27
AA15	GND_5	GND_100	E30
AA16	GND_6	GND_101	E6
AA17	GND_7	GND_102	E9
AA18	GND_8	GND_103	F2
AA19	GND_9	GND_104	F31
AA2	GND_10	GND_105	F34
AA20	GND_11	GND_106	F5
AA21	GND_12	GND_107	J2
AA22	GND_13	GND_108	J31
AA23	GND_14	GND_109	J34
AA24	GND_15	GND_110	J5
AA25	GND_16	GND_111	L9
AA34	GND_17	GND_112	M11
AA5	GND_18	GND_113	M13
AB12	GND_19	GND_114	M15
AB14	GND_20	GND_115	M17
AB16	GND_21	GND_116	M19
AB18	GND_22	GND_117	M2
AB20	GND_23	GND_118	M21
AB22	GND_24	GND_119	M23
AB24	GND_25	GND_120	M25
AC9	GND_26	GND_121	M31
AD11	GND_27	GND_122	M34
AD13	GND_28	GND_123	M5
AD15	GND_29	GND_124	N11
AD17	GND_30	GND_125	N12
AD2	GND_31	GND_126	N13
AD21	GND_32	GND_127	N14
AD23	GND_33	GND_128	N15
AD25	GND_34	GND_129	N16
AD31	GND_35	GND_130	N17
AD34	GND_36	GND_131	N18
AD5	GND_37	GND_132	N19
AE11	GND_38	GND_133	N20
AE12	GND_39	GND_134	N21
AE13	GND_40	GND_135	N22
AE14	GND_41	GND_136	N23
AE15	GND_42	GND_137	N24
AE16	GND_43	GND_138	N25
AE17	GND_44	GND_139	P12
AE18	GND_45	GND_140	P14
AE19	GND_46	GND_141	P16
AE20	GND_47	GND_142	P18
AE21	GND_48	GND_143	P20
AE22	GND_49	GND_144	P22
AE23	GND_50	GND_145	P24
AE24	GND_51	GND_146	R2
AE25	GND_52	GND_147	R34
AG2	GND_53	GND_148	R5
AG31	GND_54	GND_149	R31
AG34	GND_55	GND_150	T11
AG5	GND_56	GND_151	T13
AK2	GND_57	GND_152	T15
AK31	GND_58	GND_153	T17
AK34	GND_59	GND_154	T19
AK5	GND_60	GND_155	T21
AL12	GND_61	GND_156	T23
AL15	GND_62	GND_157	T25
AL18	GND_63	GND_158	U11
AL21	GND_64	GND_159	U12
AL24	GND_65	GND_160	U13
AL27	GND_66	GND_161	U14
AL30	GND_67	GND_162	U15
AL6	GND_68	GND_163	U16
AL9	GND_69	GND_164	U17
AN2	GND_70	GND_165	U18
AN34	GND_71	GND_166	U19
AP12	GND_72	GND_167	U20
AP15	GND_73	GND_168	U21
AP18	GND_74	GND_169	U22
AP21	GND_75	GND_170	U23
AP24	GND_76	GND_171	U24
AP27	GND_77	GND_172	U25
AP3	GND_78	GND_173	V12
AP30	GND_79	GND_174	V14
AP33	GND_80	GND_175	V16
AP6	GND_81	GND_176	V18
AP9	GND_82	GND_177	V2
B12	GND_83	GND_178	V20
B15	GND_84	GND_179	V22
B21	GND_85	GND_180	V24
B24	GND_86	GND_181	V31
B27	GND_87	GND_182	V5
B3	GND_88	GND_183	V9
B30	GND_89	GND_184	Y11
B33	GND_90	GND_185	Y13
B6	GND_91	GND_186	Y15
B9	GND_92	GND_187	Y17
C2	GND_93	GND_188	Y19
C34	GND_94	GND_189	Y21
E12	GND_95	GND_190	Y23
		GND_191	Y25



(20) VMA_DQ[63..0]
 (20) VMA_DM[7..0]
 (20) VMA_WDQS[7..0]
 (20) VMA_RDQS[7..0]

CHANNEL A: 512MB/1024MB DDR3



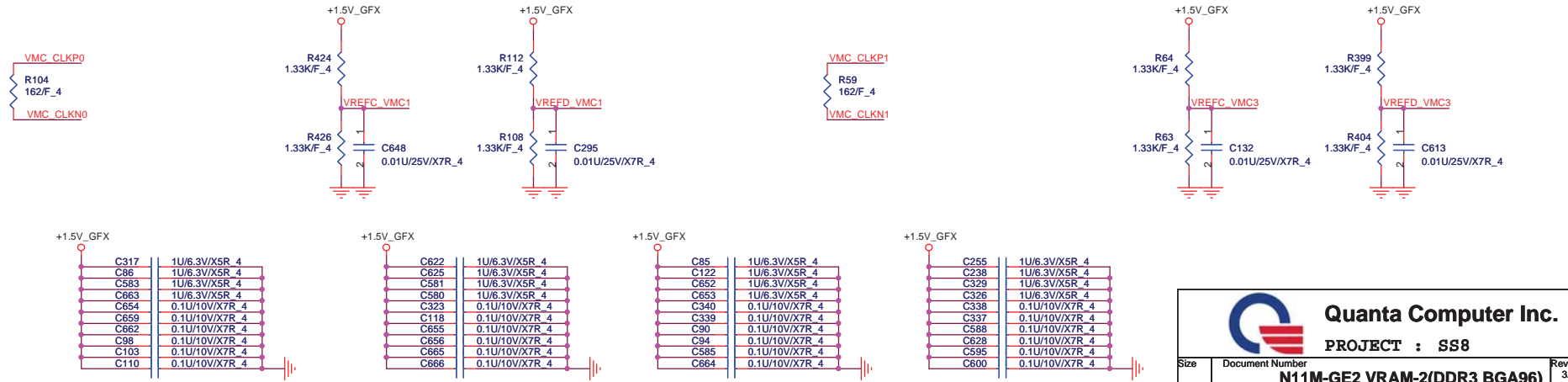
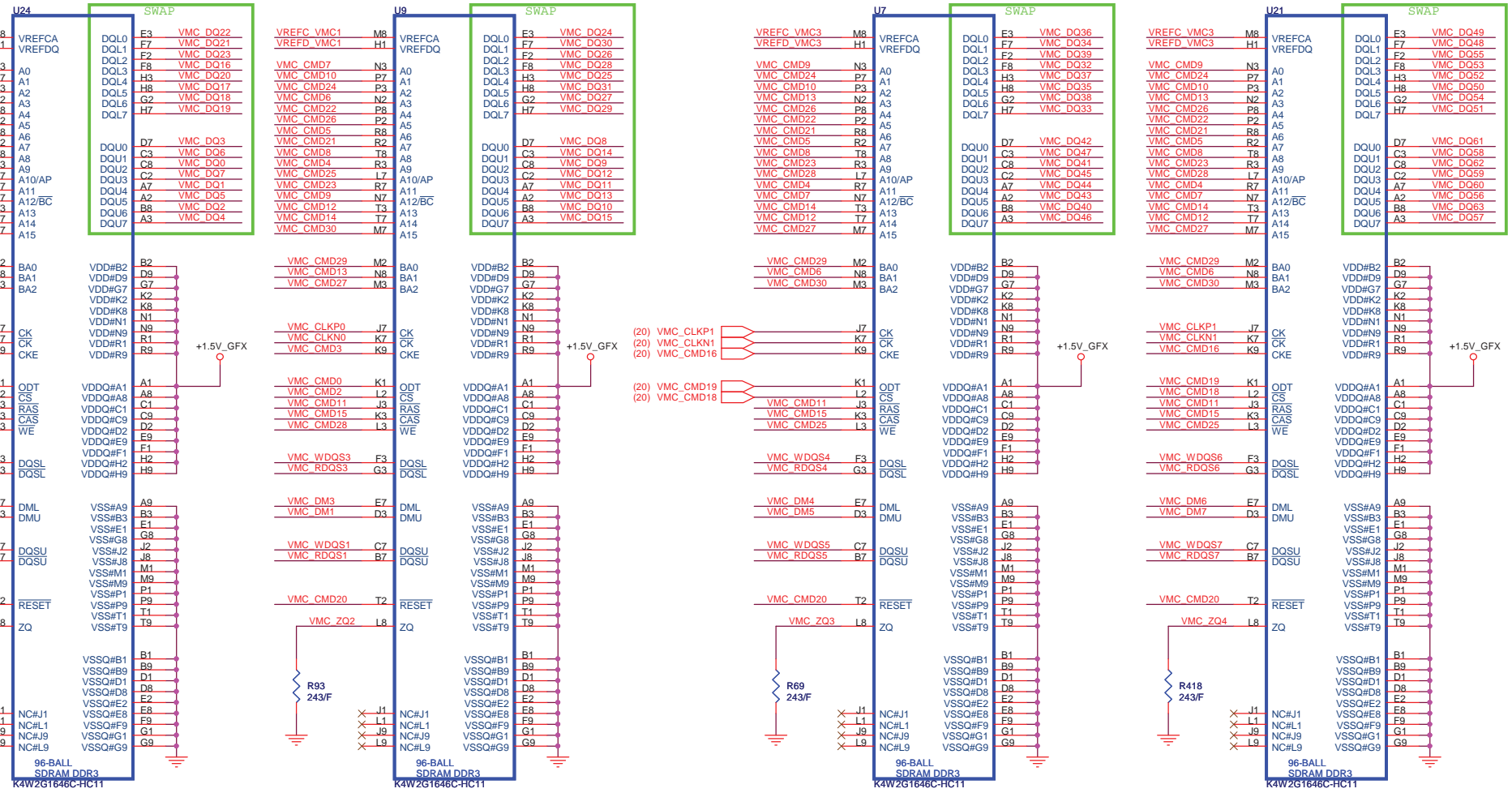

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Size Document Number
N11M-GE2 VRAM-1(DDR3 BGA96) Rev 3A

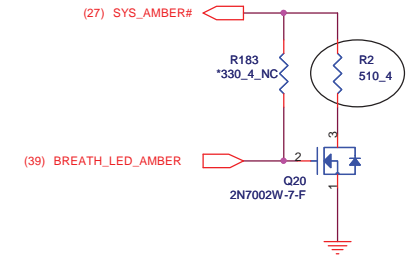
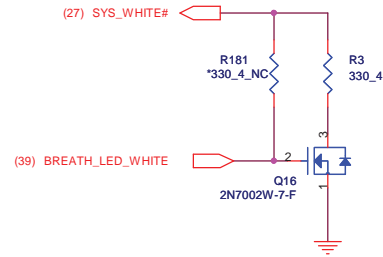
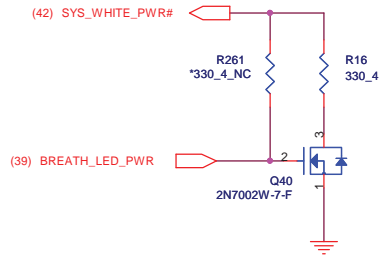
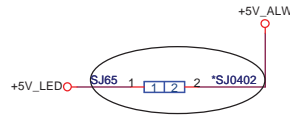
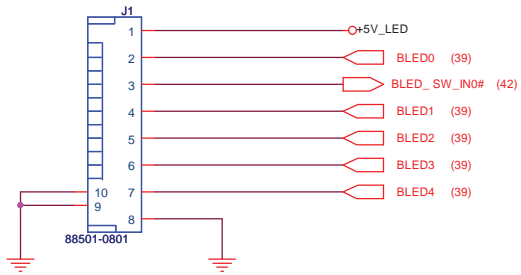
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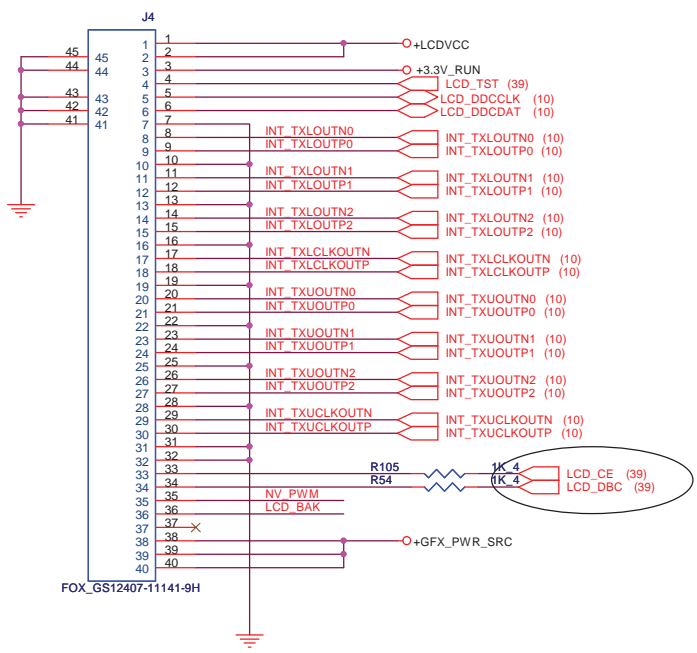
(20) VMC_DQ[63..0] (20) VMC_DM[7..0] (20) VMC_WDQS[7..0] (20) VMC_RDQS[7..0]

CHANNEL B: 512MB/1024MB DDR3



Conn to BLED Board

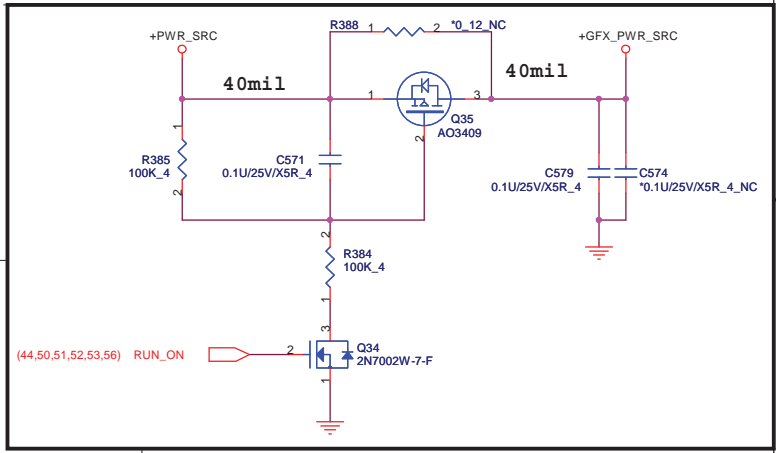
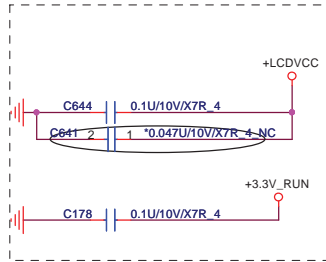
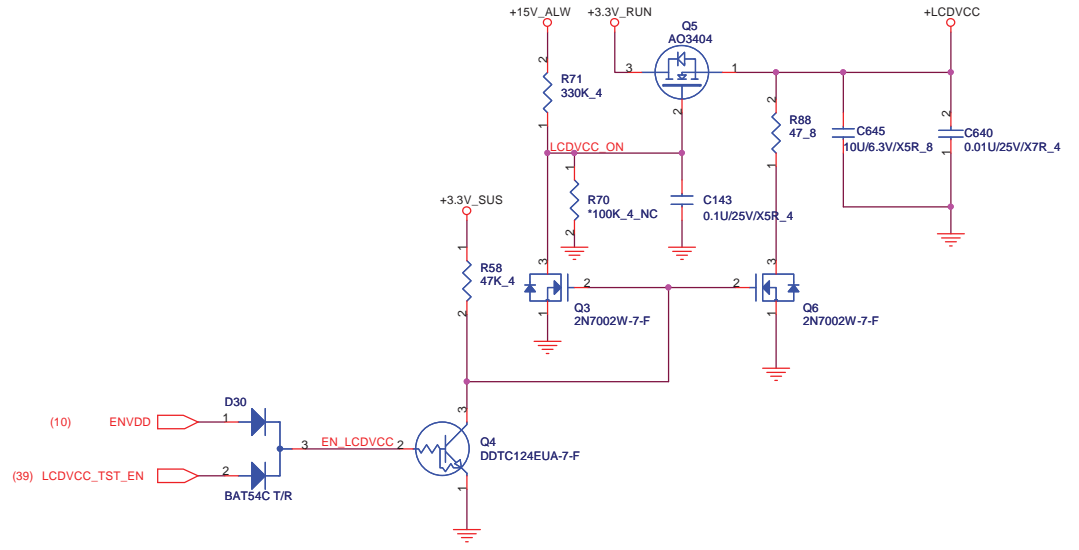
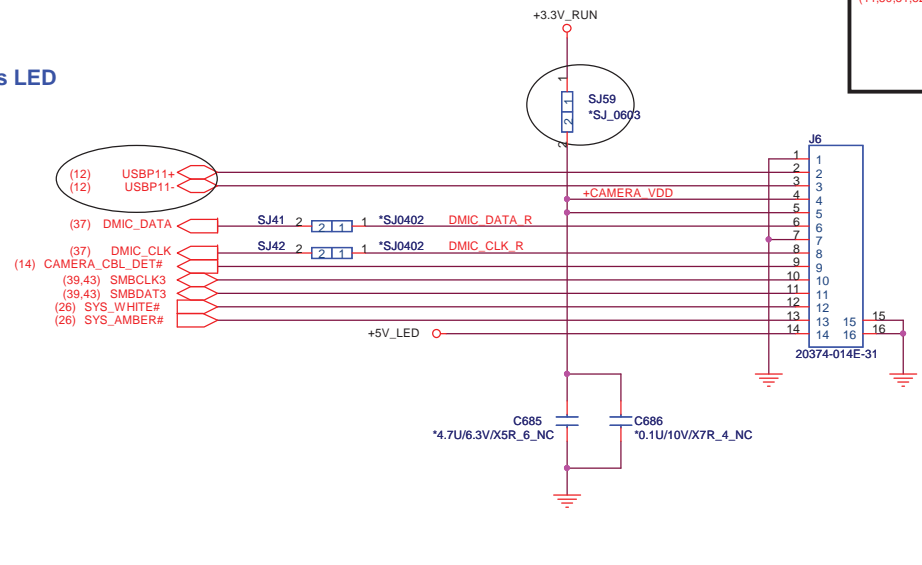
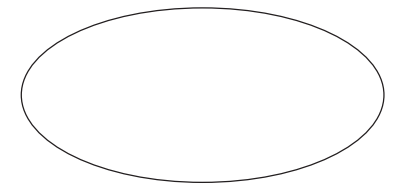




EMC Reserve

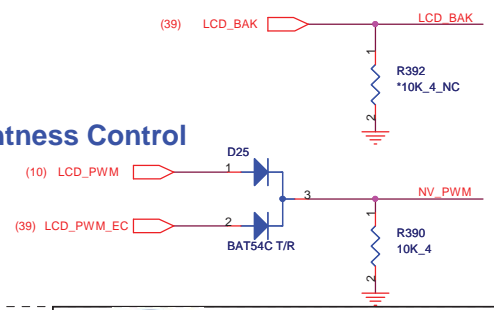
INT_TXLCLKOUTN	R411	1	2	*100 4 NC	INT_TXLCLKOUTP
INT_TXL*OUTN2	R412	1	2	*100 4 NC	INT_TXL*OUTP2
INT_TXL*OUTN1	R416	1	2	*100 4 NC	INT_TXL*OUTP1
INT_TXL*OUTN0	R419	1	2	*100 4 NC	INT_TXL*OUTP0
INT_TXUCLKOUTN	R400	1	2	*100 4 NC	INT_TXUCLKOUTP
INT_TXU*OUTN2	R407	1	2	*100 4 NC	INT_TXU*OUTP2
INT_TXU*OUTN1	R408	1	2	*100 4 NC	INT_TXU*OUTP1
INT_TXU*OUTN0	R410	1	2	*100 4 NC	INT_TXU*OUTP0

Array Microphone & Camera & System Status LED

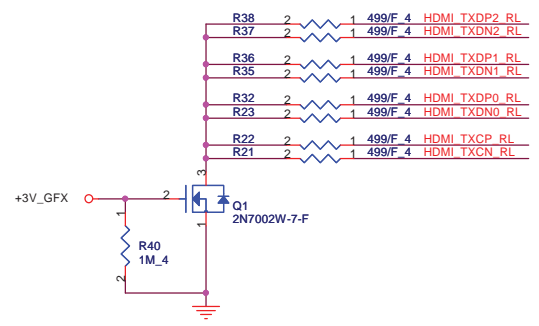
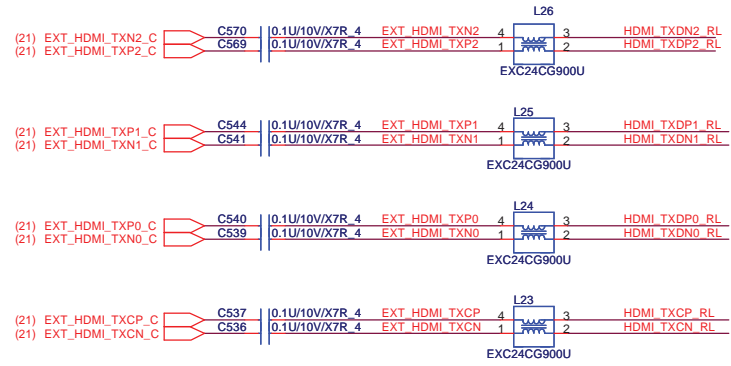
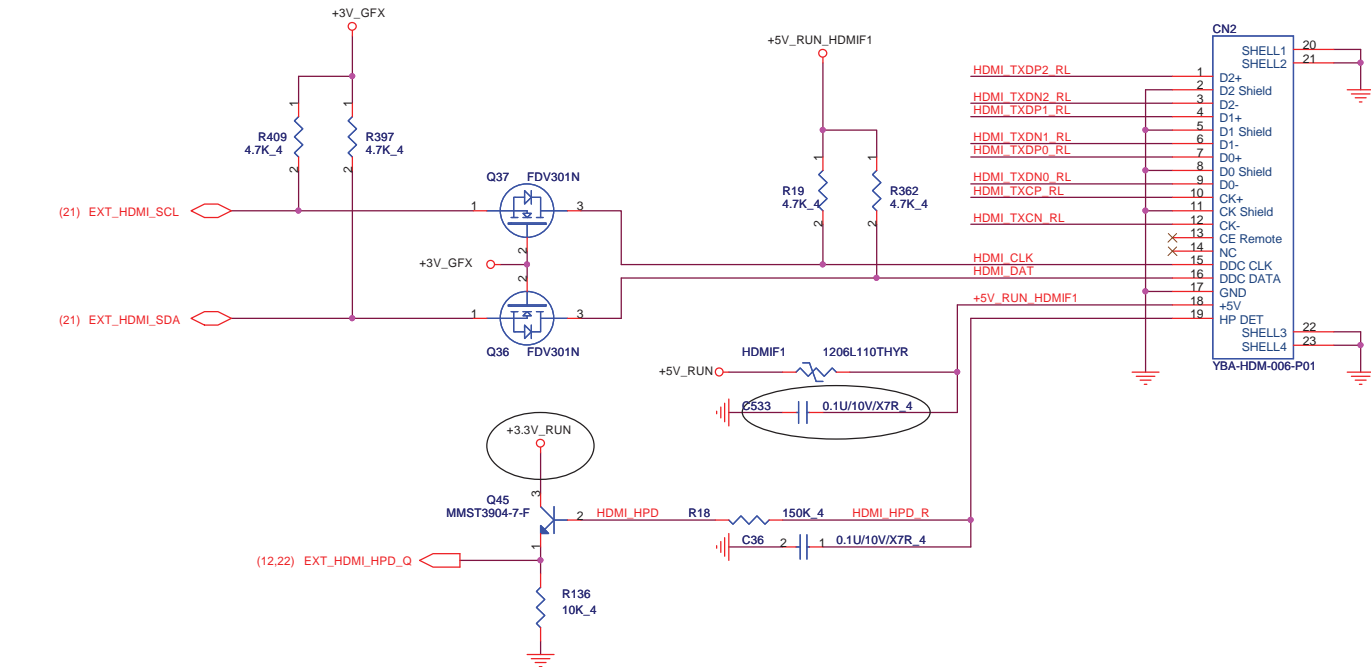


Backlight Enable

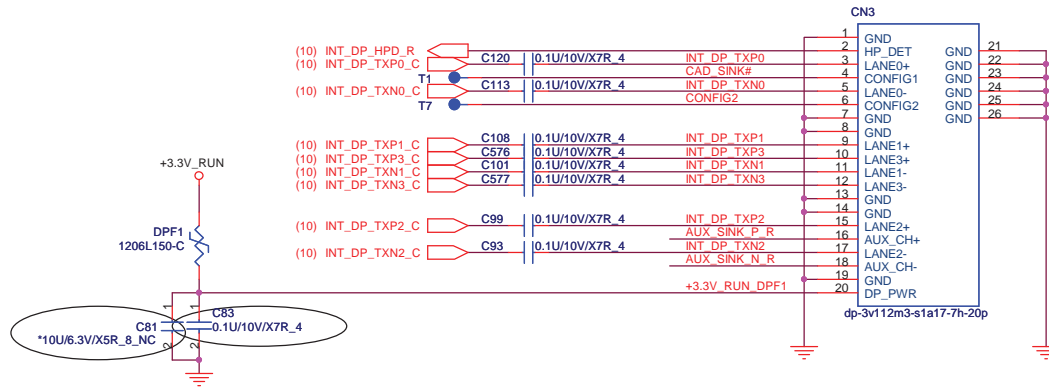
Brightness Control



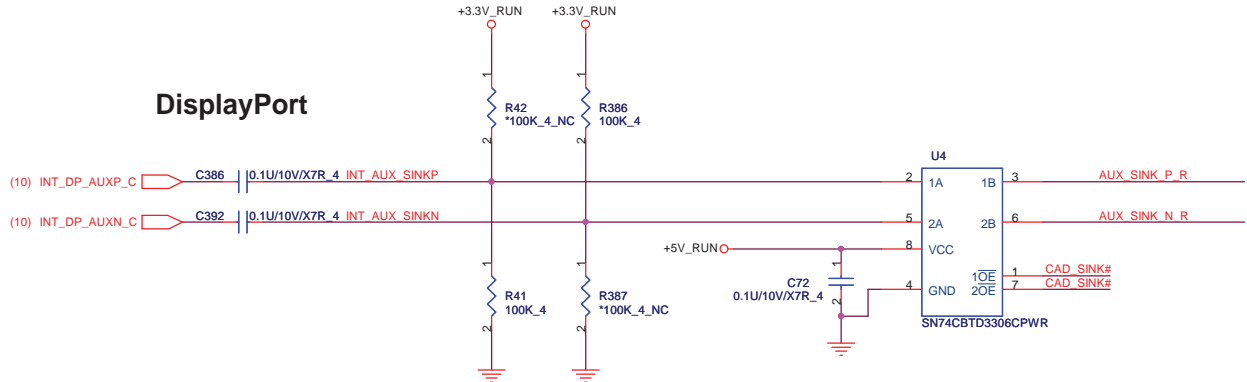
HDMI



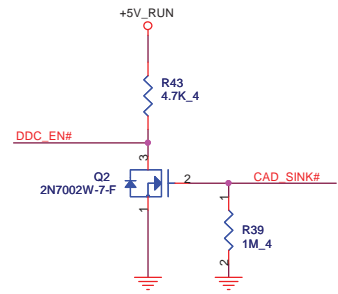
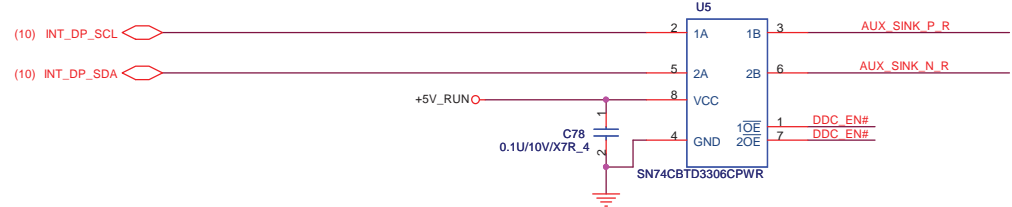
MINI DISPLAY PORT CONNECTOR

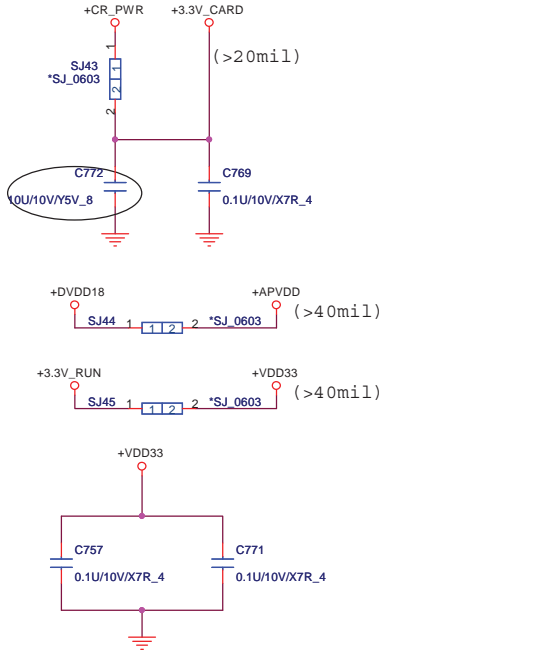


DisplayPort



HDMI

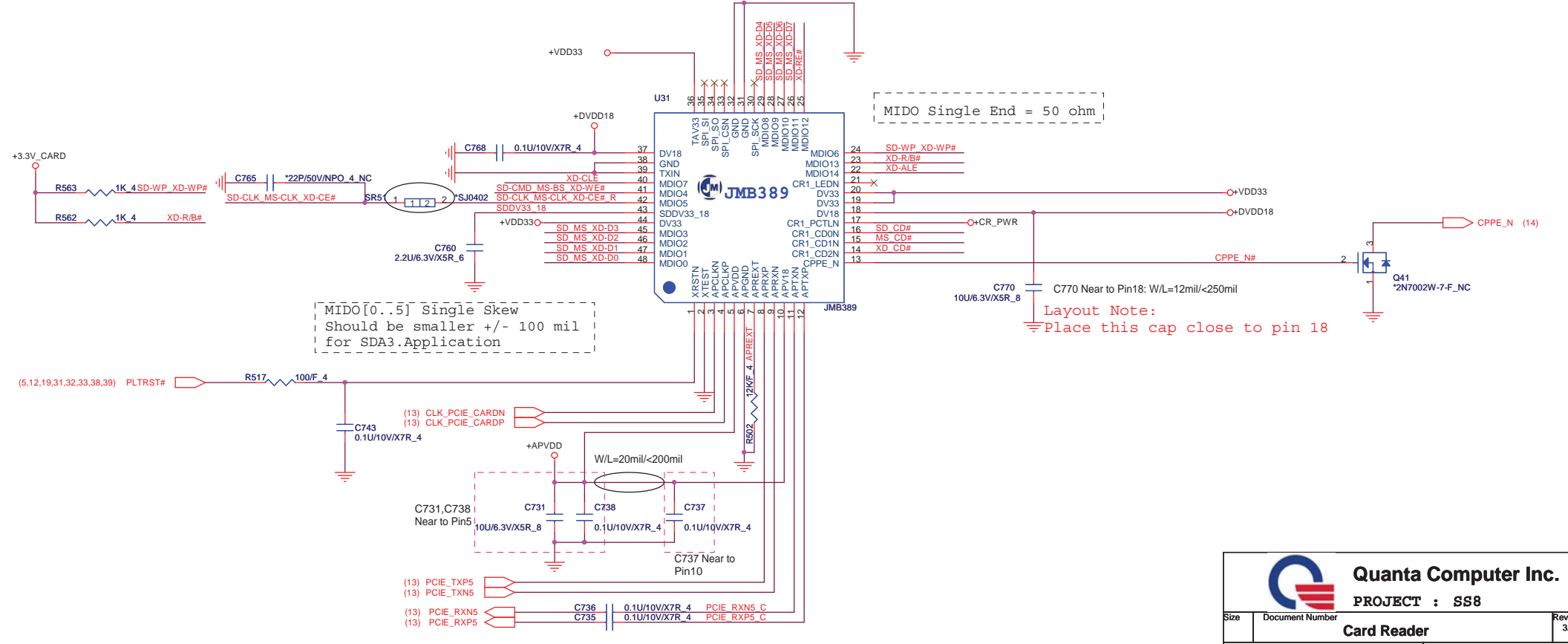
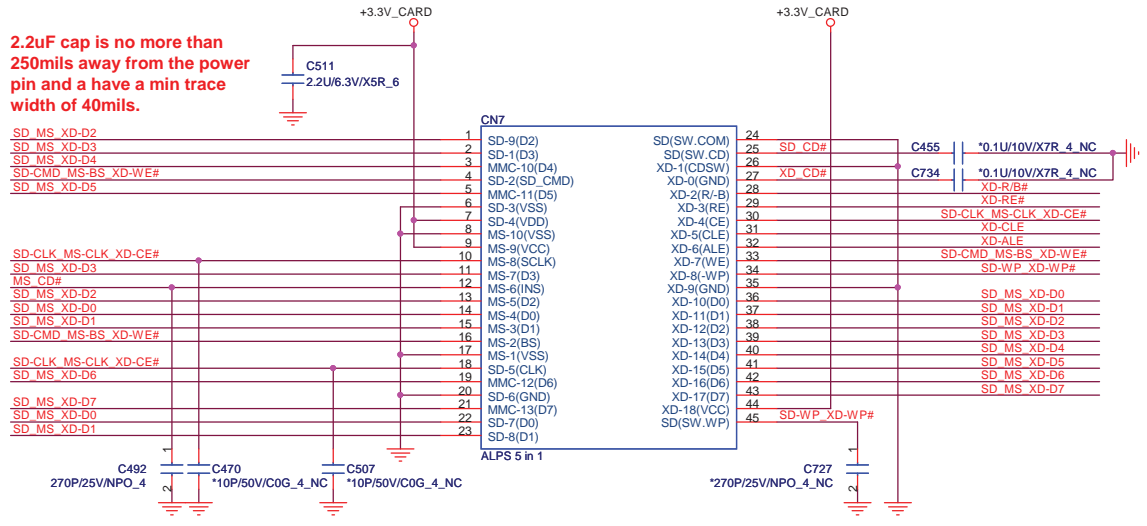




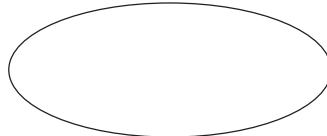
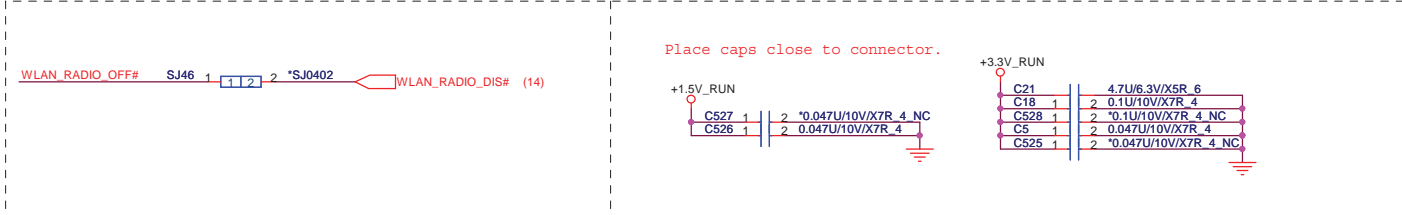
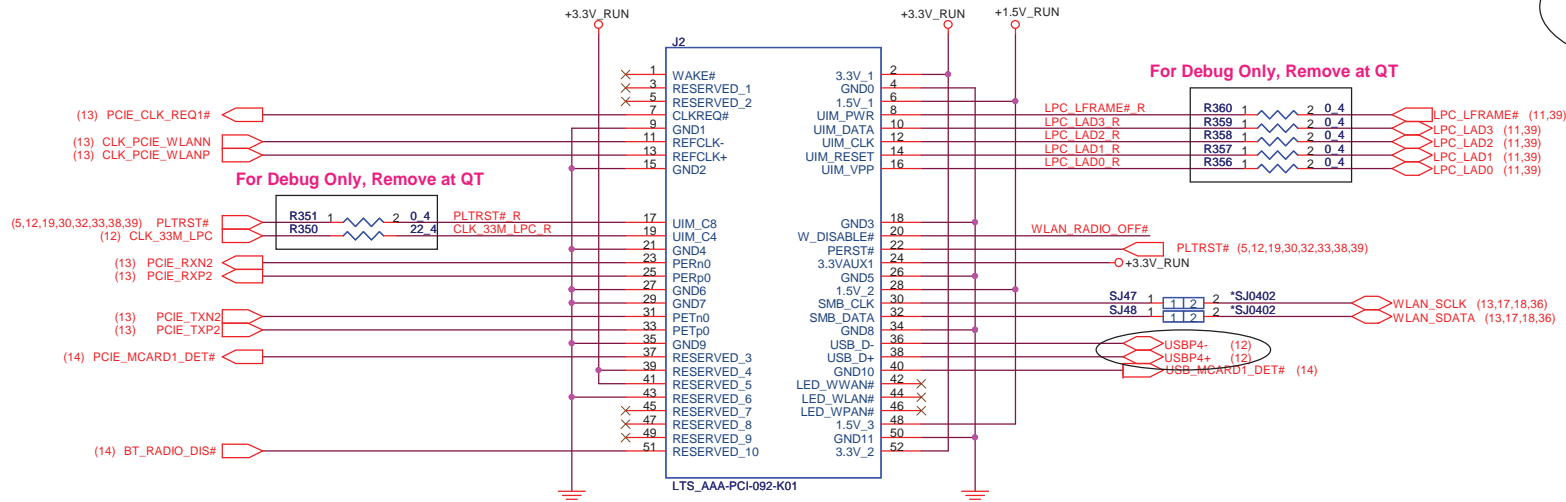
Card Reader interface signal mapping

PIN	Default	SD / MMC	MS	XD
MDIO00	SD/NMC/MS/xD	SD D0	MS D0	XD D0
MDIO01		SD D1	MS D1	XD D1
MDIO02		SD D2	MS D2	XD D2
MDIO03		SD D3	MS D3	XD D3
MDIO04		SD CMD	MS BS	XD WE#
MDIO05		SD CLK	MS CLK	XD CE#
MDIO06		SD WP		XD WP#
MDIO07				XD CLE
MDIO08		NMC D4	MS D4	XD D4
MDIO09		NMC D5	MS D5	XD D5
MDIO10		NMC D6	MS D6	XD D6
MDIO11		NMC D7	MS D7	XD D7
MDIO12				XD RS#
MDIO13				XD R/B#
MDIO14				XD ALE
CR1_LEDN		SD LED#	MS LED#	XD LED#
CR1_PCTAN		SD PWR#	MS PWR#	XD PWR#
CR1_CD0		SD CD#		
CR1_CD1			MS CD#	
CR1_CD2				XD CD#

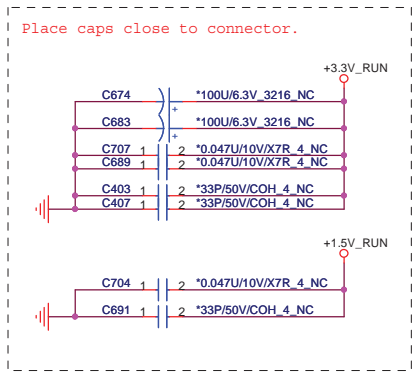
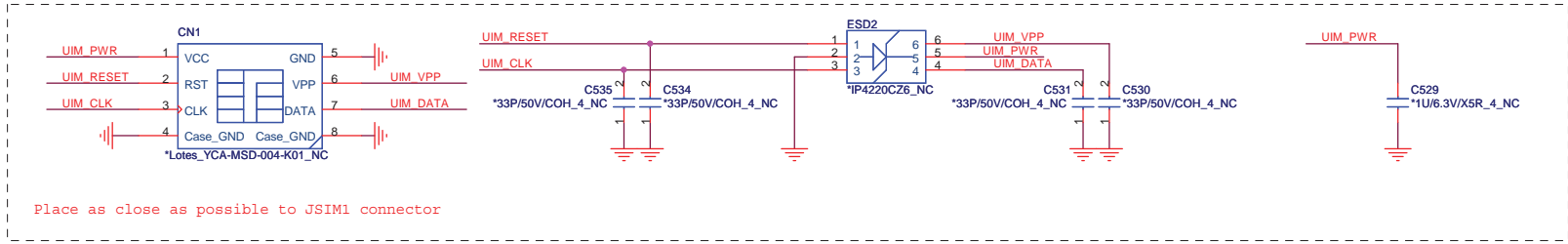
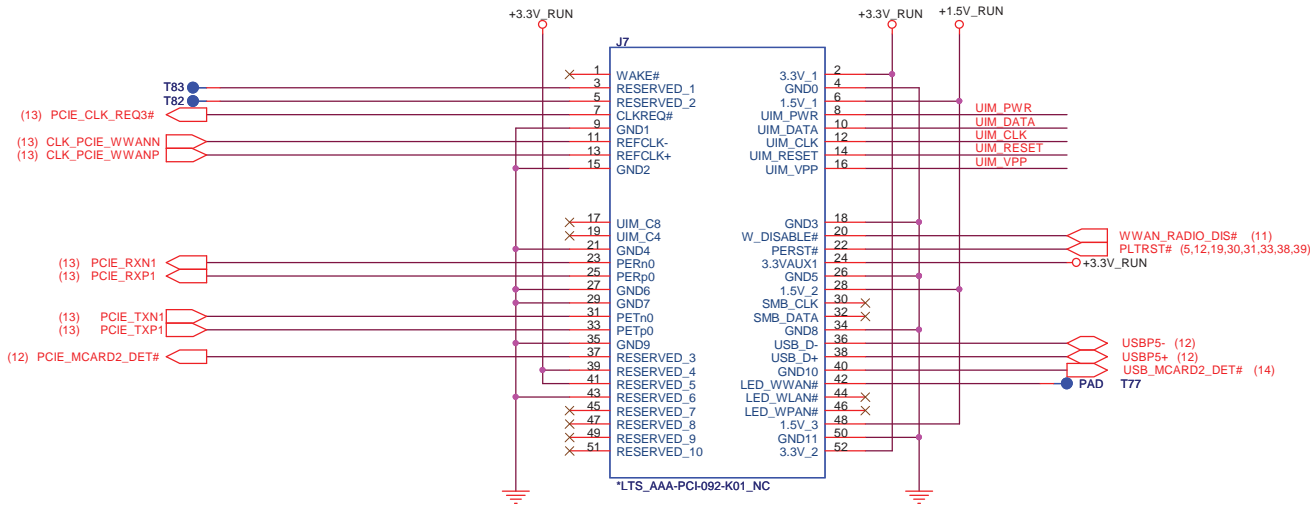
2.2uF cap is no more than 250mils away from the power pin and a have a min trace width of 40mils.



MiniCard WLAN connector

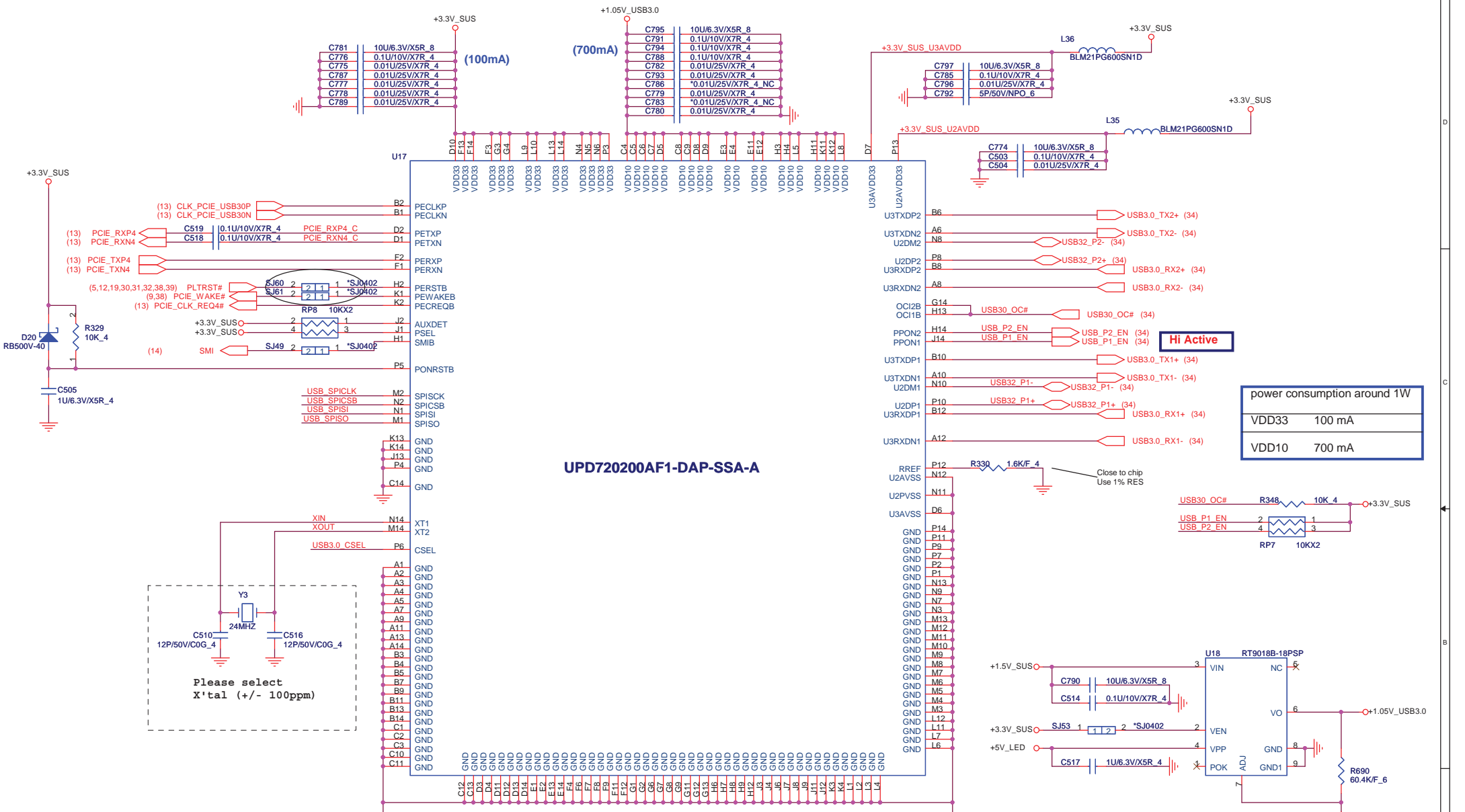


MiniCard WWAN connector



Place as close as possible to JSIM1 connector

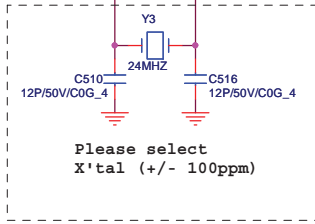
Place caps close to connector.



UPD720200AF1-DAP-SSA-A

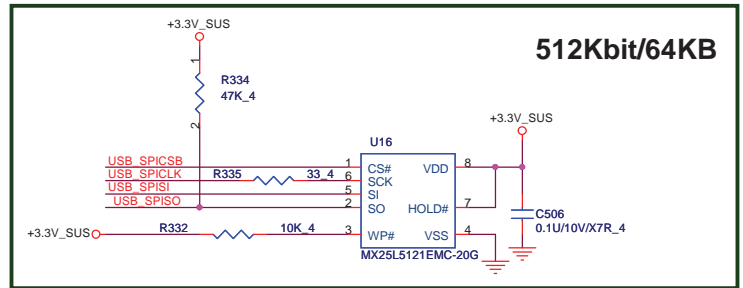
power consumption around 1W	
VDD33	100 mA
VDD10	700 mA

Hi Active

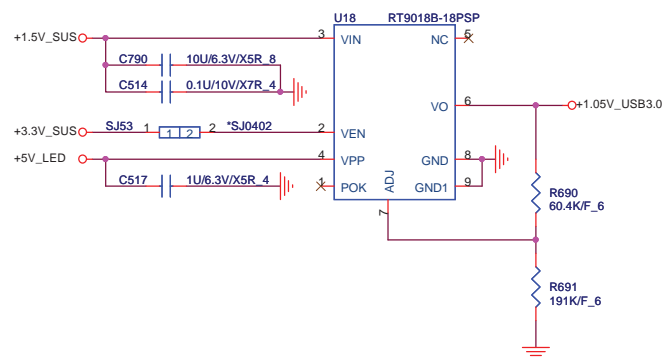


Please select X'tal (+/- 100ppm)

Clock select signal	
USB3.0_CSEL	High = External 48Mhz
	Low = 24MHz X'tal



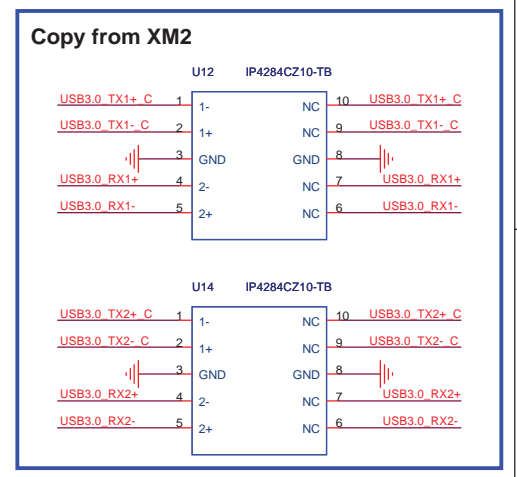
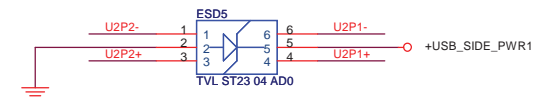
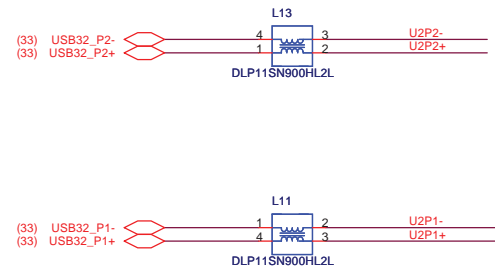
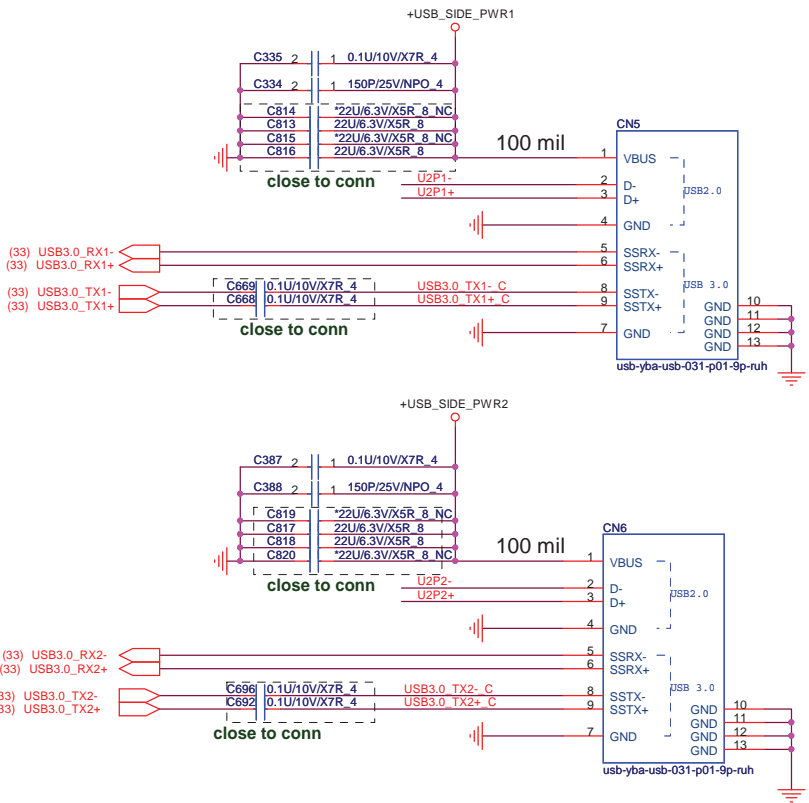
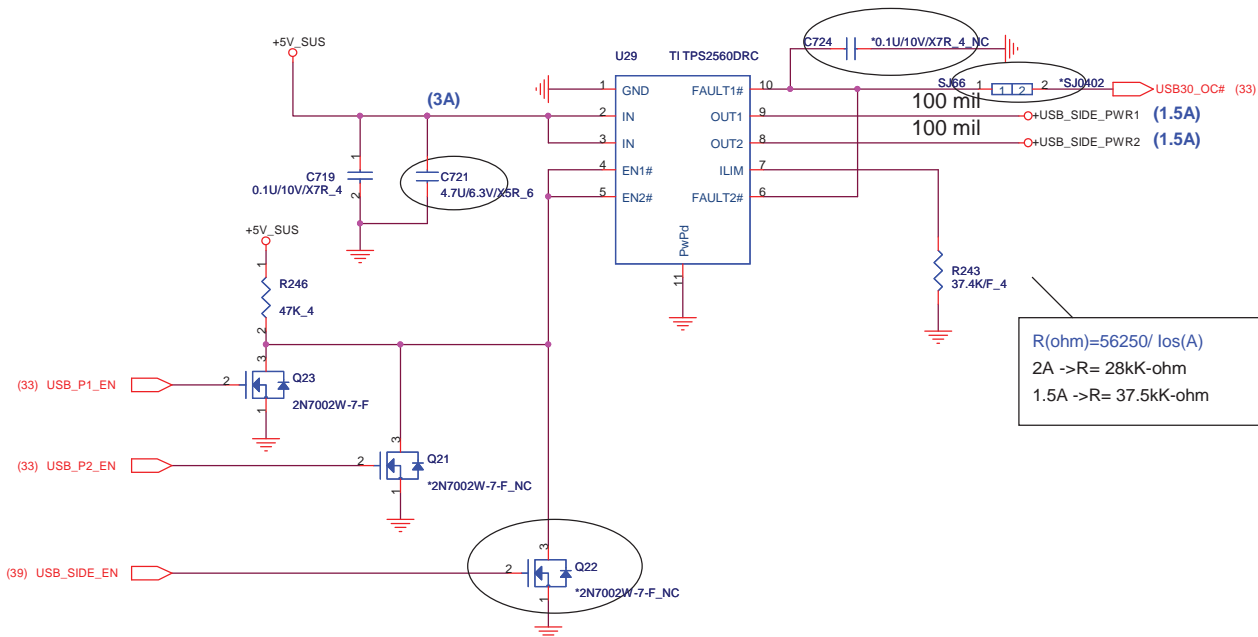
512Kbit/64KB



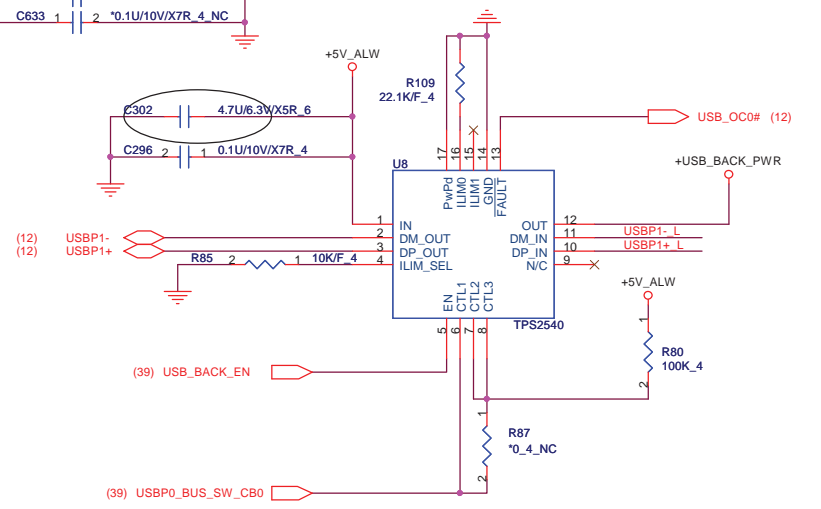
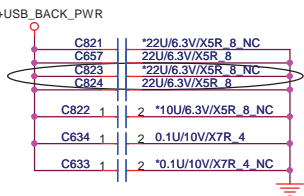
Quanta Computer Inc.
PROJECT : SS8
NEC USB 3.0

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ESATA + USB Conn + Power share



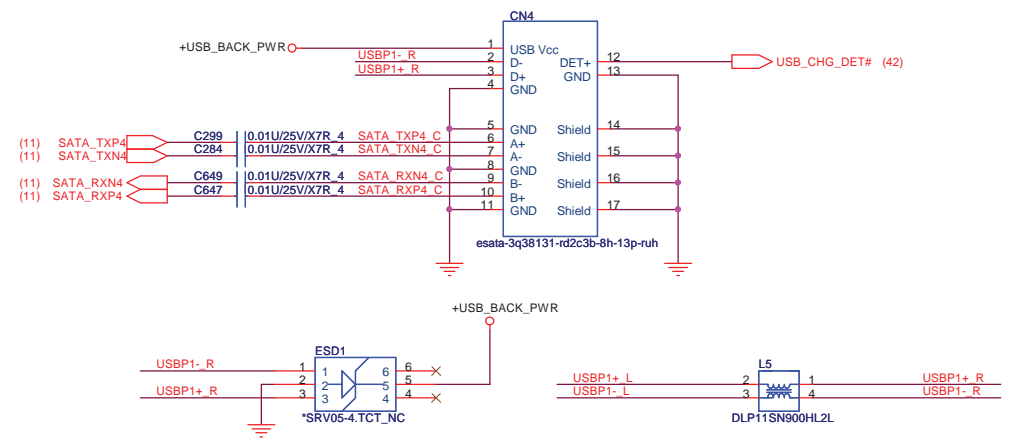
ES(PG1.0): Stuff R87, Un-Stuff R80
MP(PG1.1): Un-Stuff R87, Stuff R80

USBP0_BUS_SW_CB0	Mode
Low	DCP, Auto-detect
High	CDP, BC Spec 1.1

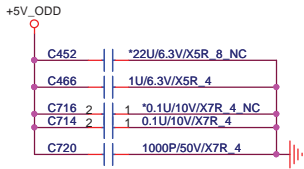
OC limitation	R109	mA
	100k ohm	480
	22.1k ohm	2171

Applied Now

E-SATA Conn

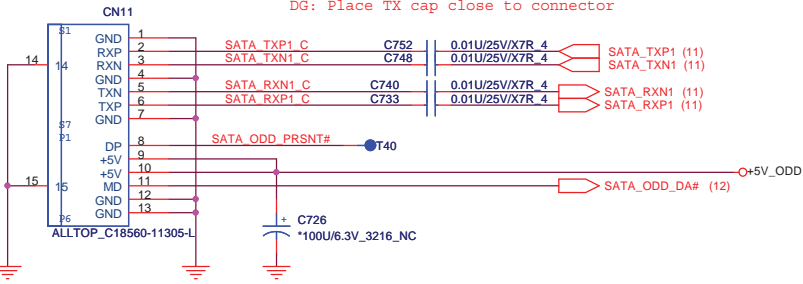


Place caps close to CN11.

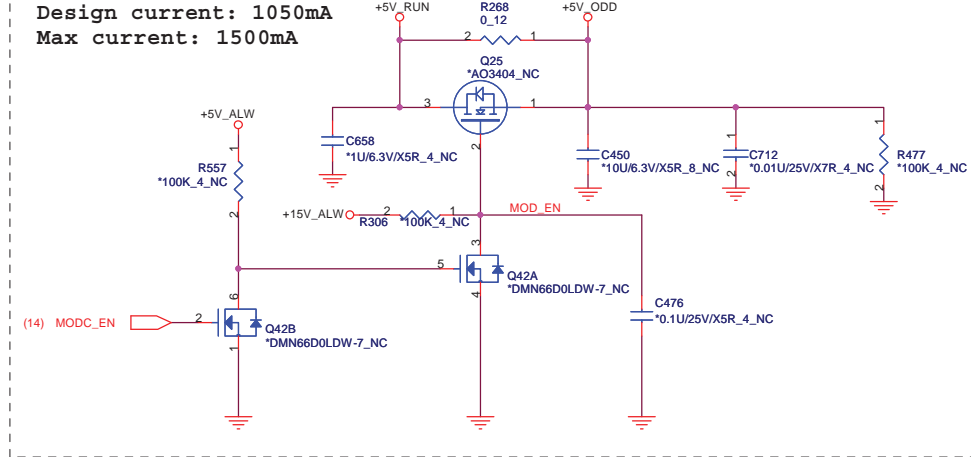


ODD Connector

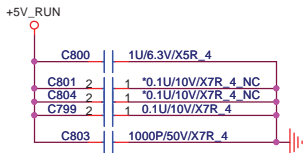
DG: Place TX cap close to connector



Design current: 1050mA
Max current: 1500mA

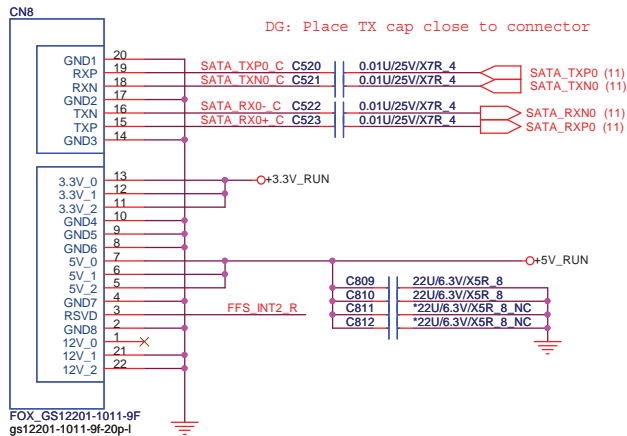


Place caps close to CN8.

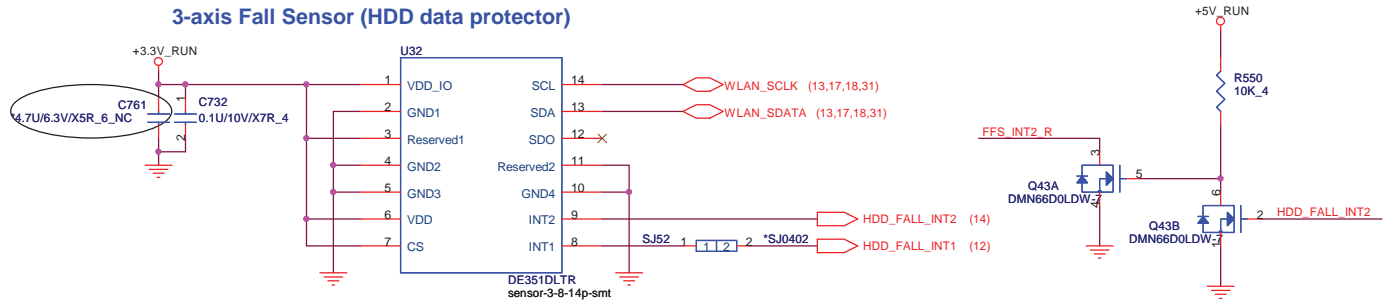



SATA Connector.

DG: Place TX cap close to connector



3-axis Fall Sensor (HDD data protector)

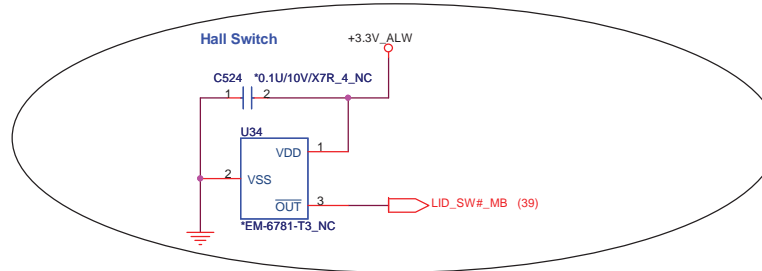
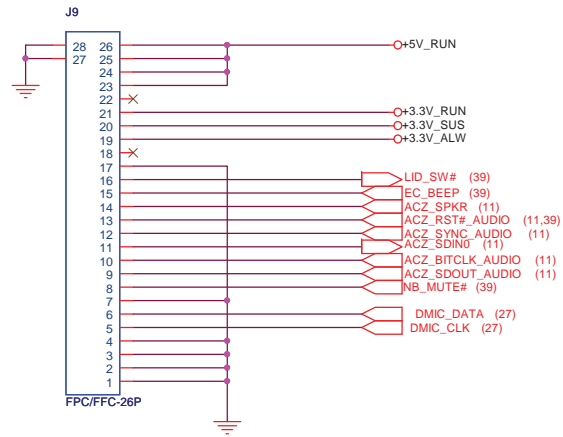




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CONNECT TO AUDIO BOARD

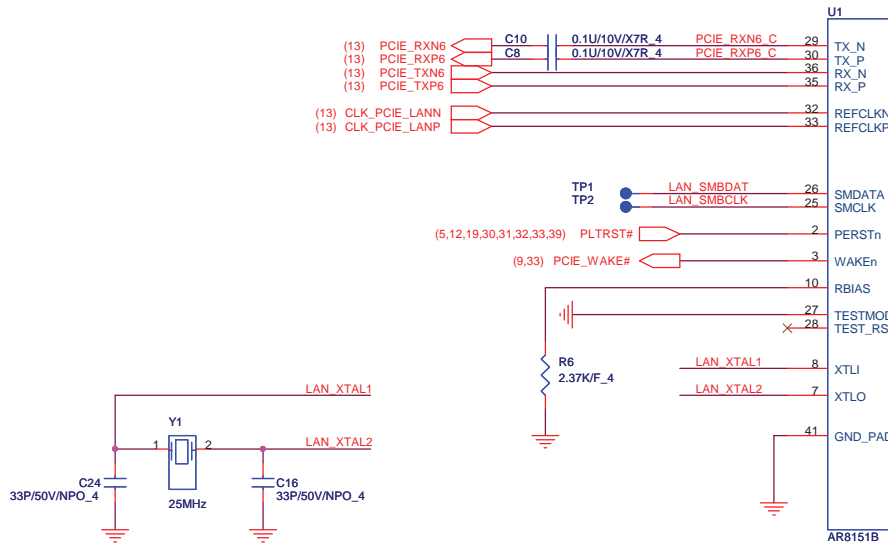
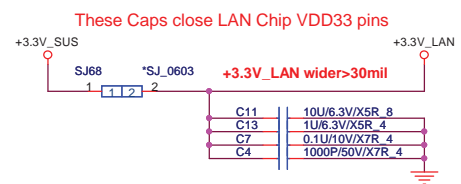


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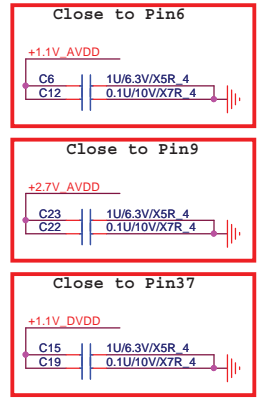
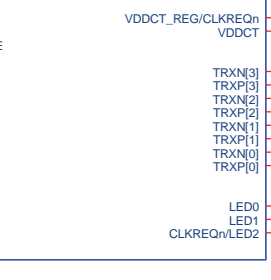
PROJECT : SS8

Azelia CODEC

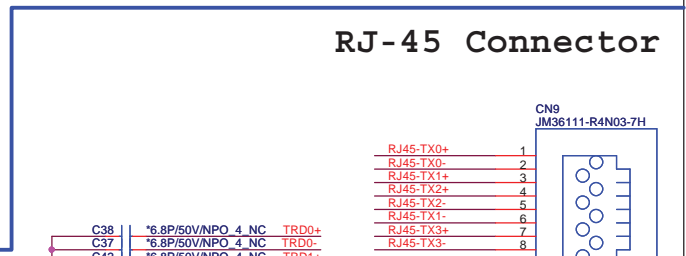
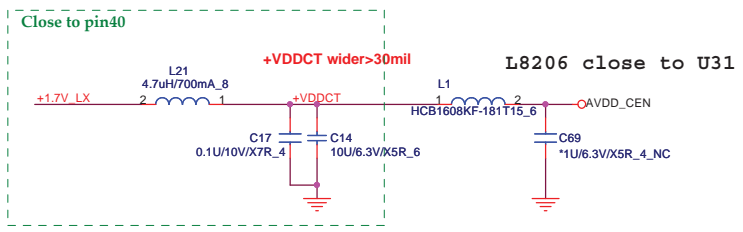
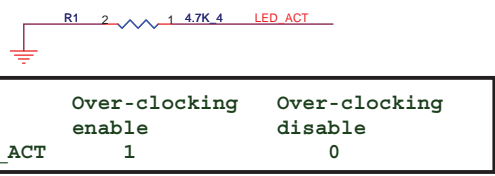
Size	Document Number	Rev
		3A



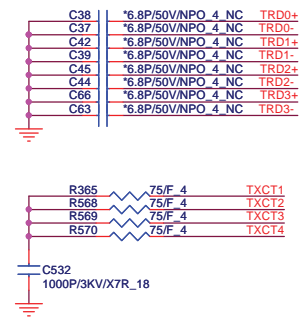
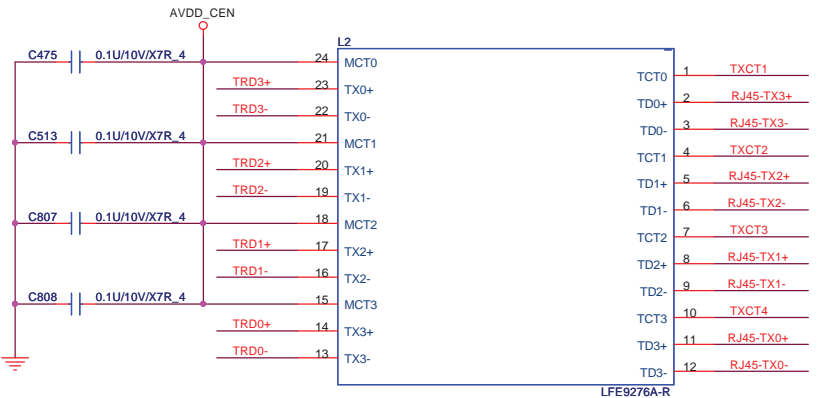
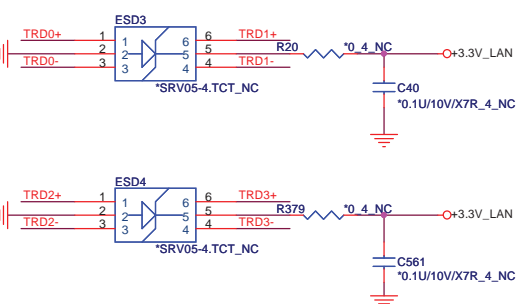
Atheros AR8151 AR8152



Netlist delete
Pin13 &19



Change to CM1293A-04SO

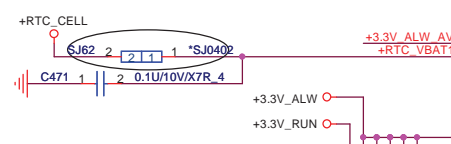
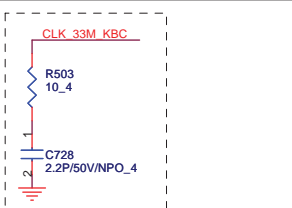


Wait for Connector list to update

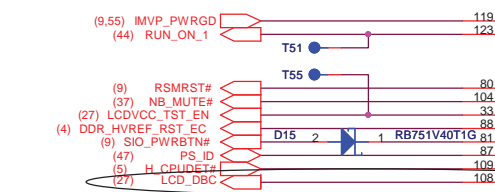
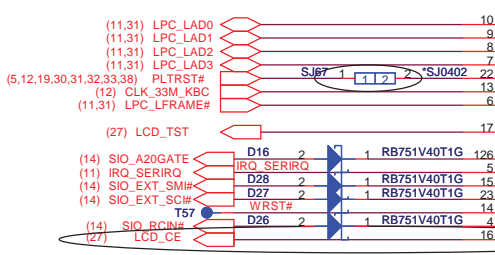
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PROJECT : SS8

LAN (AR8151B)

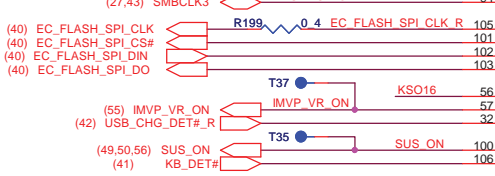
Size Document Number Rev
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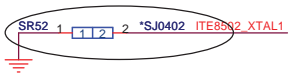
SERIRO
SC(V1.0)P38:
8.2-k pull-up to +V3.3S
CRB uses a 10-k pull-up to +V3.3S.



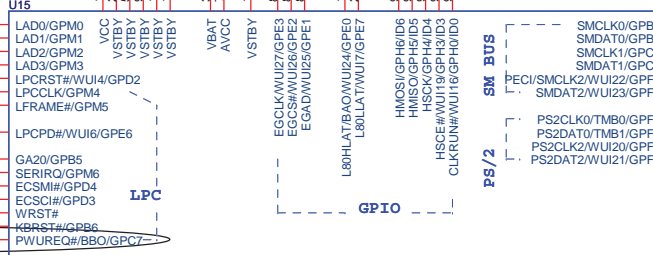
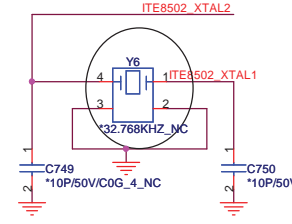
Thermal



For Crystal-Free



32KHz Clock.



IT8518E/CX

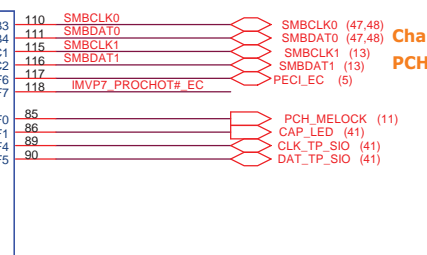
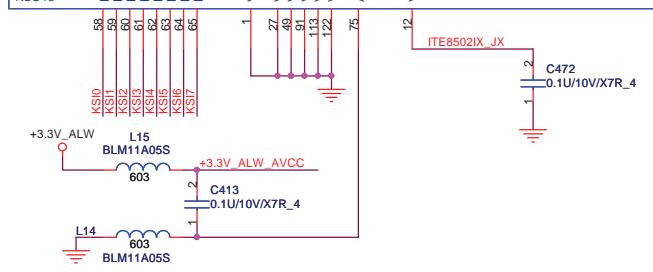
UART port

EXTERNAL SERIAL FLASH

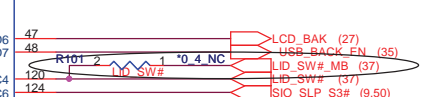
SPI ENABLE

KBMX

CLOCK



PWM



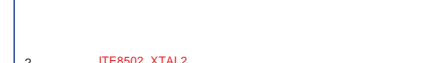
WAKE UP



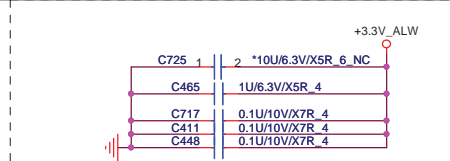
A/D D/A



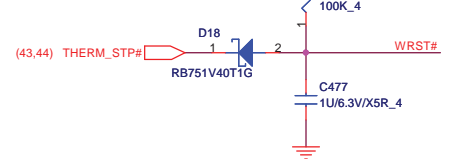
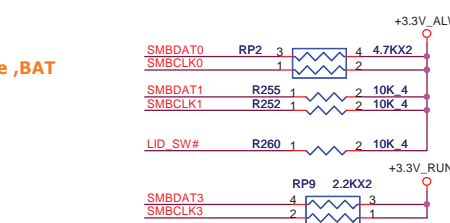
CLOCK



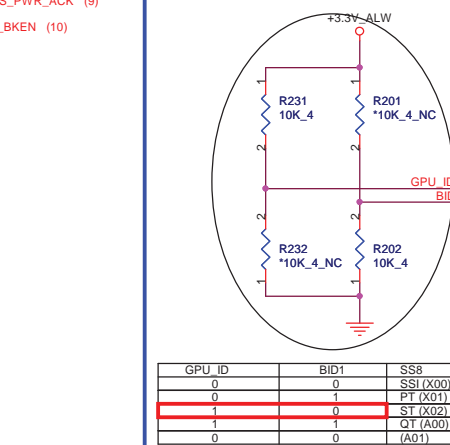
CLOCK



Place these caps close to ITE8518.



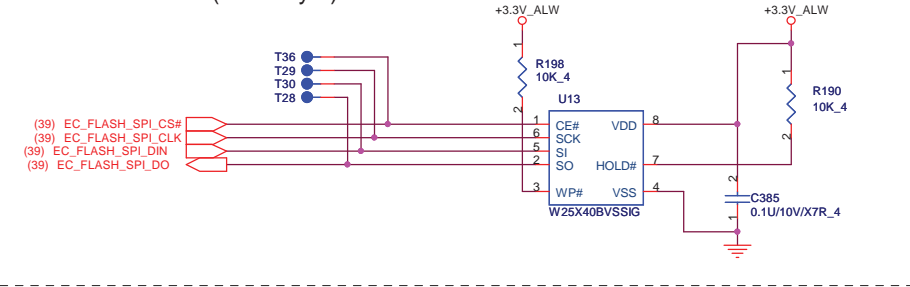
Board ID Straps



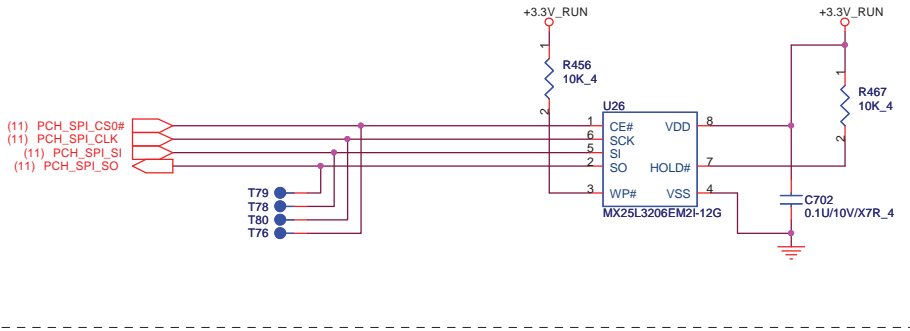
Quanta Computer Inc.
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SIO (ITE8518E)

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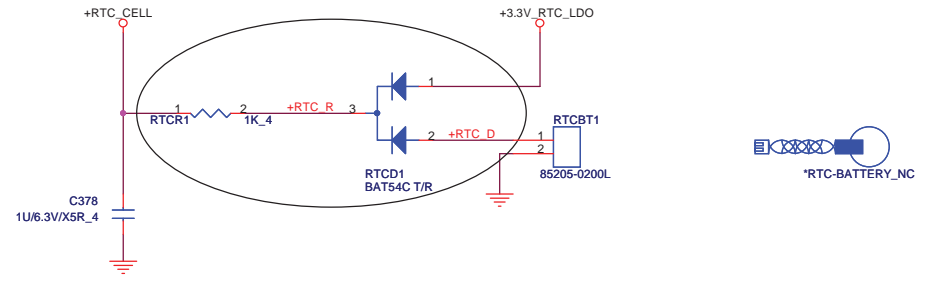
For EC 4Mbit (512K Byte)

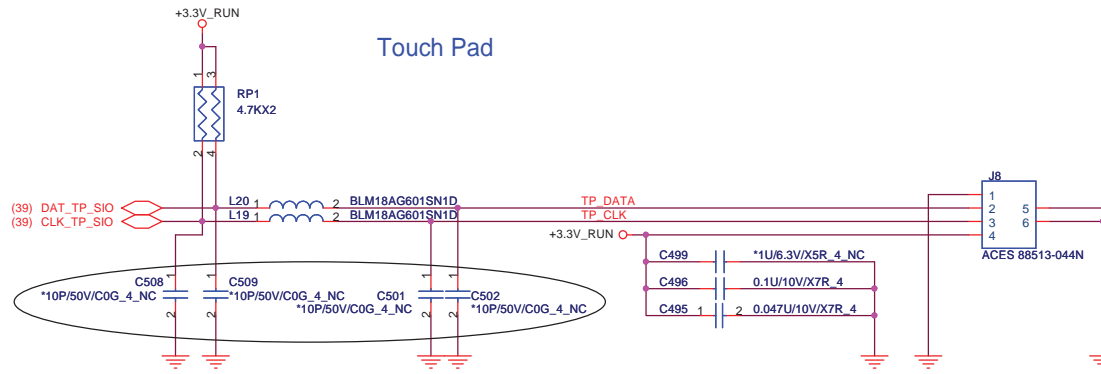


For PCH 32Mbit (4M Byte)

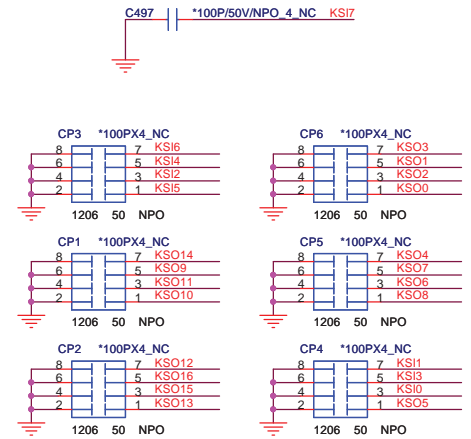
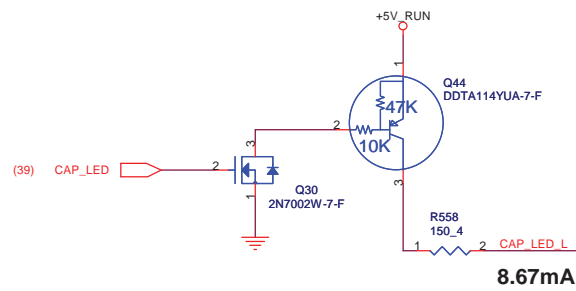


RTC BATTERY



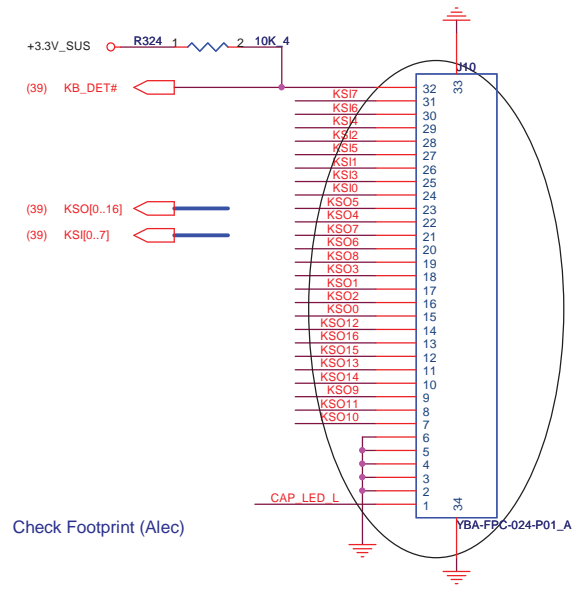


$V_{i(on_max)} = -1.4V$
 $V_{i(off_min)} = -0.3$



100P CAPS CLOSE TO JKB1

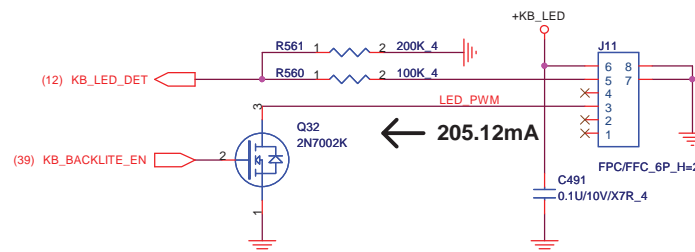
KEYBOARD CONNECTOR



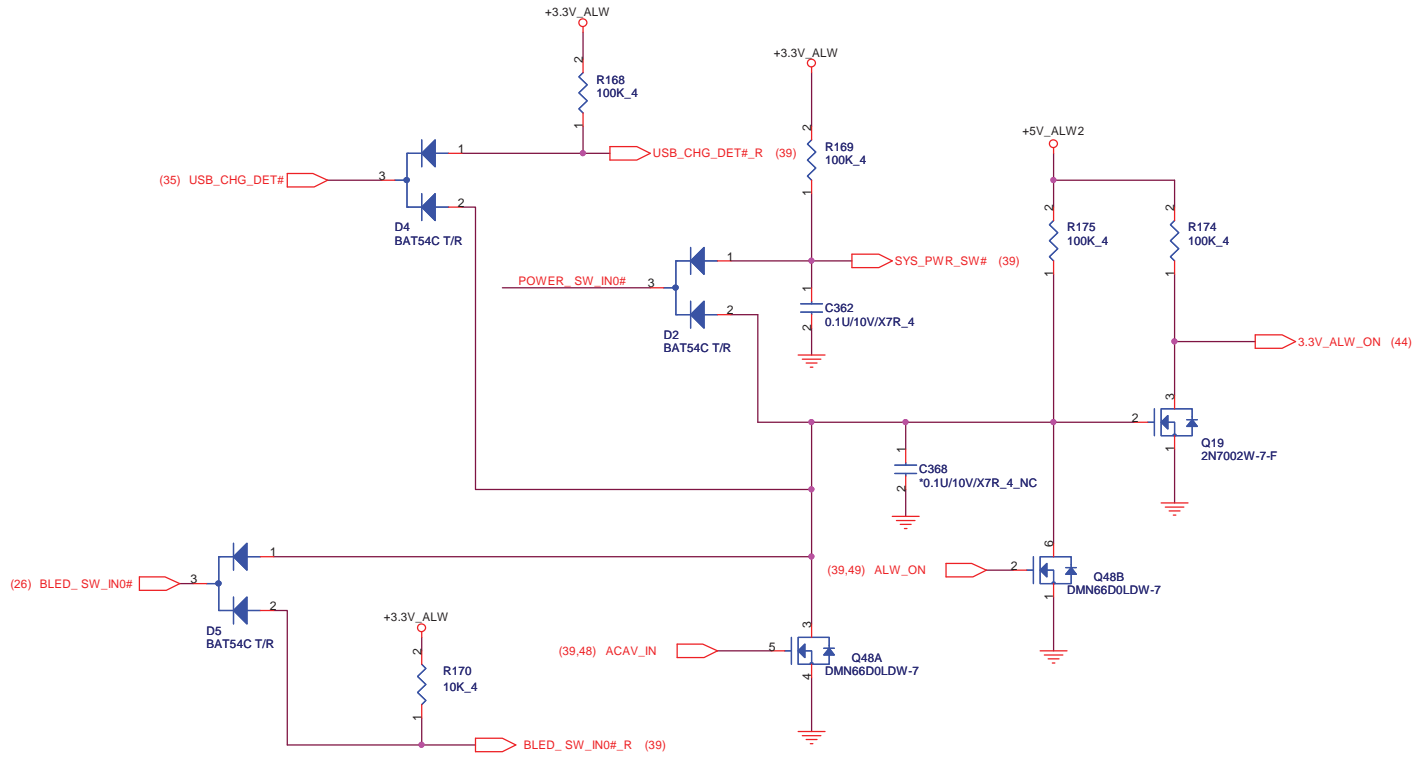
Conn Copy From SS7

+KB_LED power trace width >10 mil

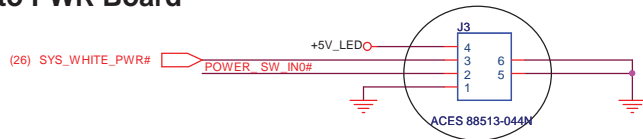
Key board illumination



3VALW ON POWER LOGIC



Conn to PWR Board



Status White LED

Solid White= System On, Normal Activity
 Solid White= Charging (system on);
 Solid White= Charging (system off or hibernate and battery charge <98%);
 OFF= Charging (system off or hibernate and battery charge > 98%);
 "Breathing White " = System in Standby (S3);
 Off = System Off (or in Hibernate);

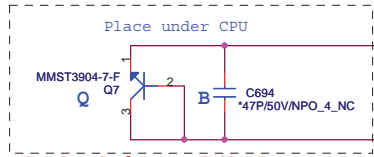
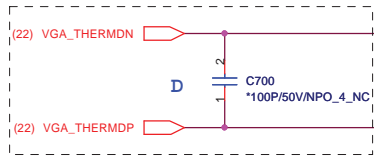
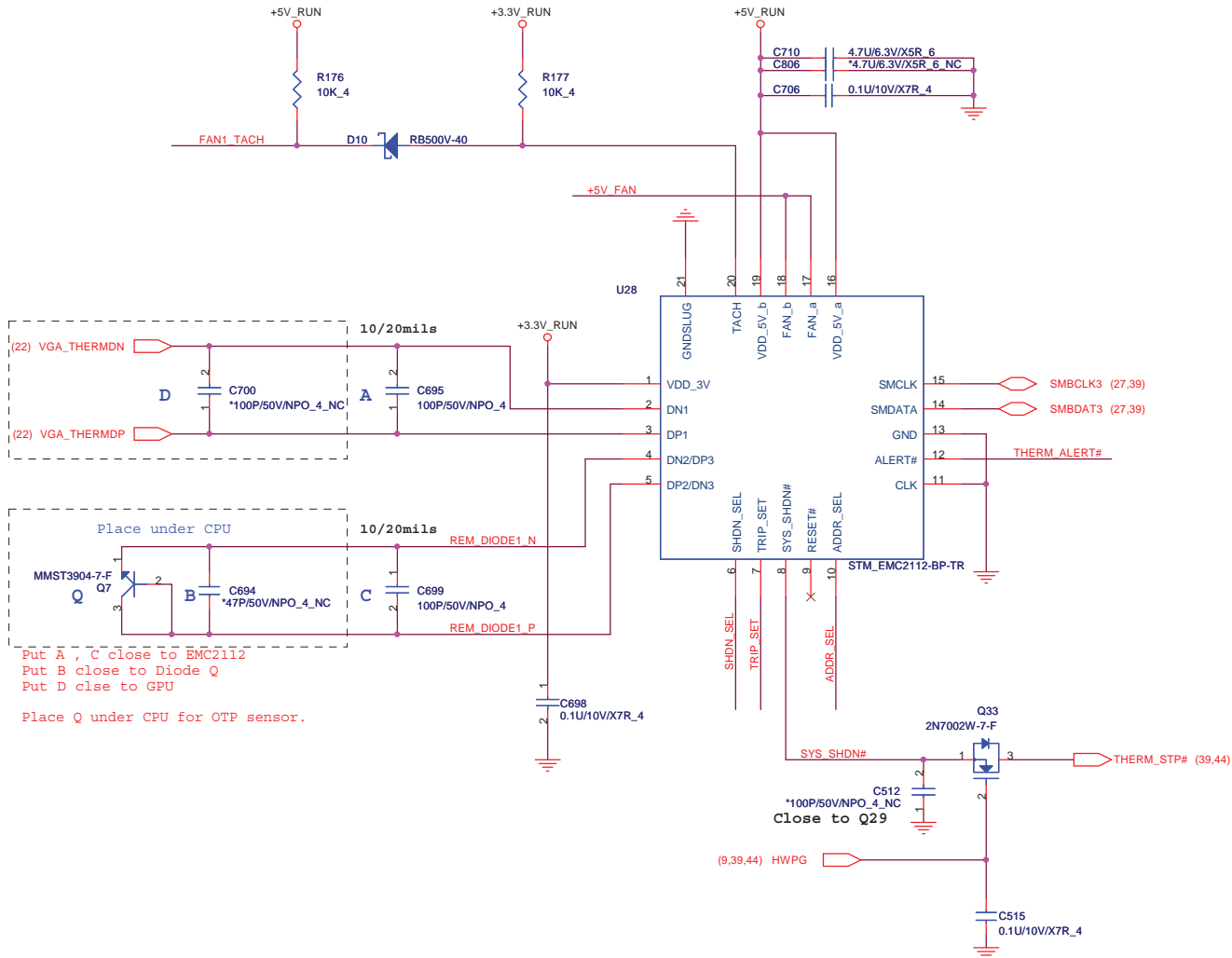
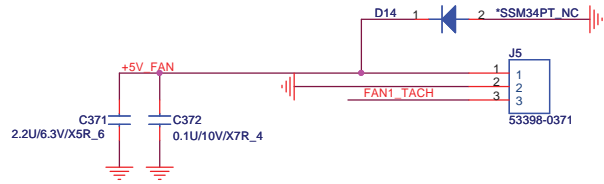


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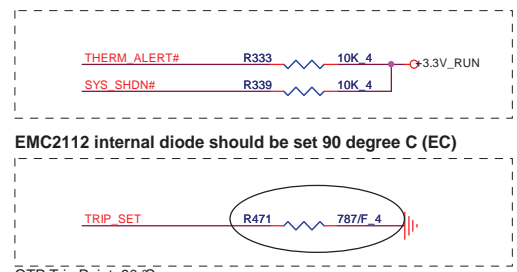
PROJECT : SS8

Size	Document Number	Rev
	PWR SW/LED	3A
Date:	Monday, January 03, 2011	Sheet 42 of 57

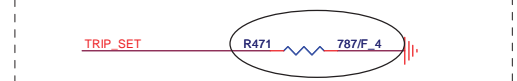
FAN CONTROL



Put A, C close to EMC2112
 Put B close to Diode Q
 Put D close to GPU
 Place Q under CPU for OTP sensor.



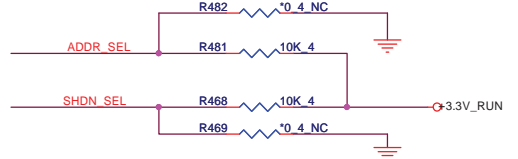
EMC2112 internal diode should be set 90 degree C (EC)

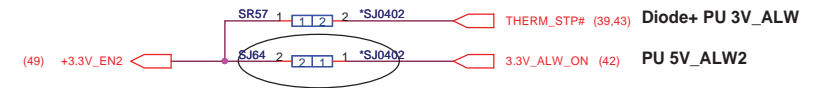
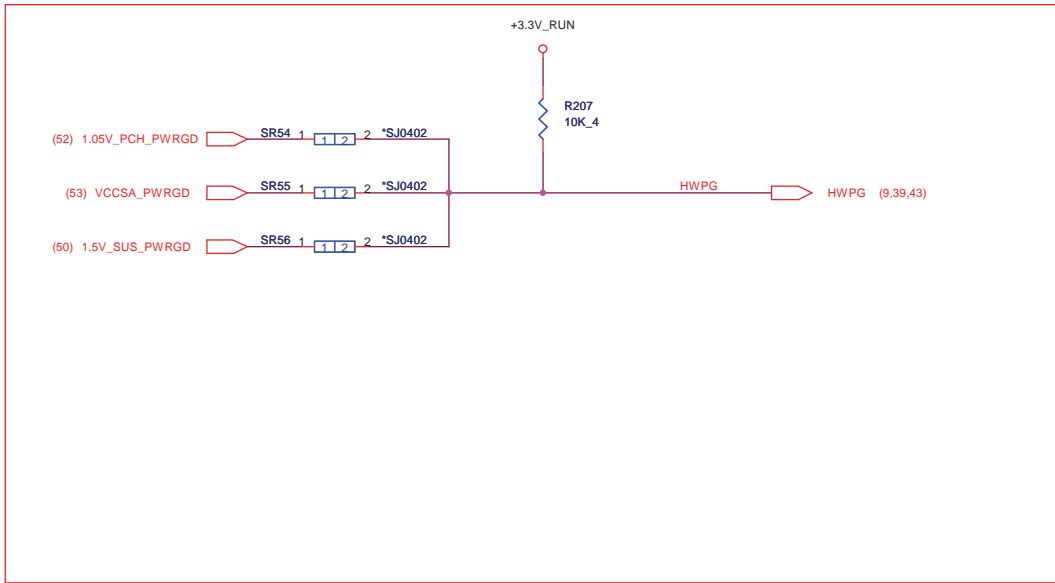


OTP Trip Point: 90 °C
 OTP Hysteresis: 85 °C (Vincent)

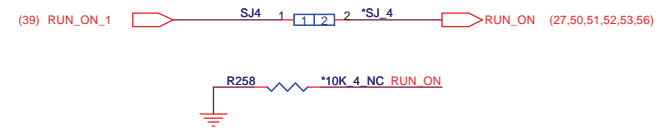
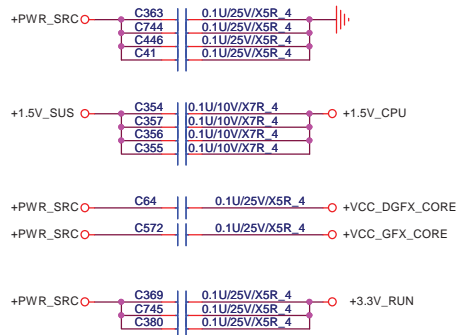
Need to check with BIOS
ADDR_SEL
 HIGH: 0101 110xb
 OPN: 0111 101xb
 GND: 0101 111xb

SHDN_SEL
 HIGH: External Diode 2 Mode
 OPN: AMD CPU/Diode Mode
 GND: Intel Transistor Mode





Stitch Cap



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		3A
System Reset Circuit		
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CPU XDP

PCH XDP

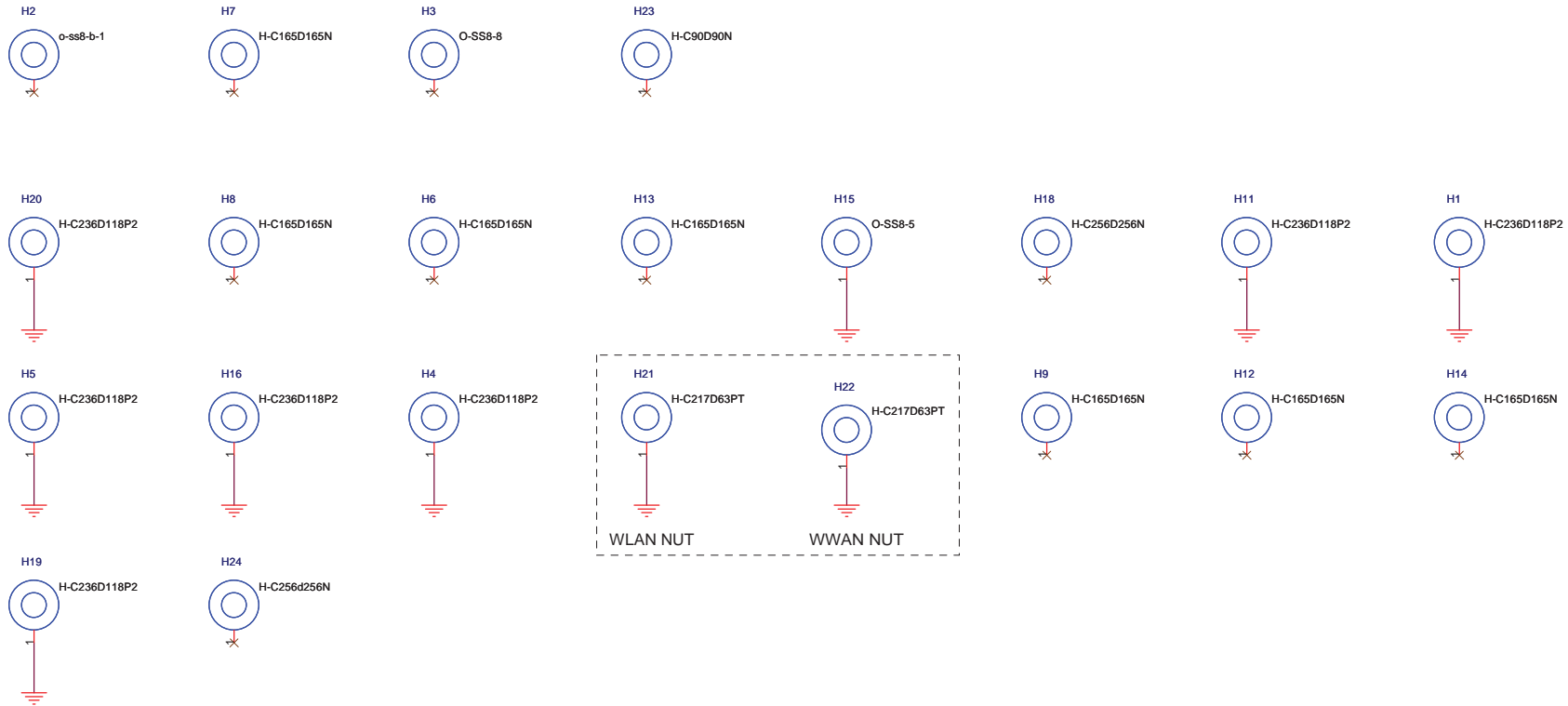
Del 0420

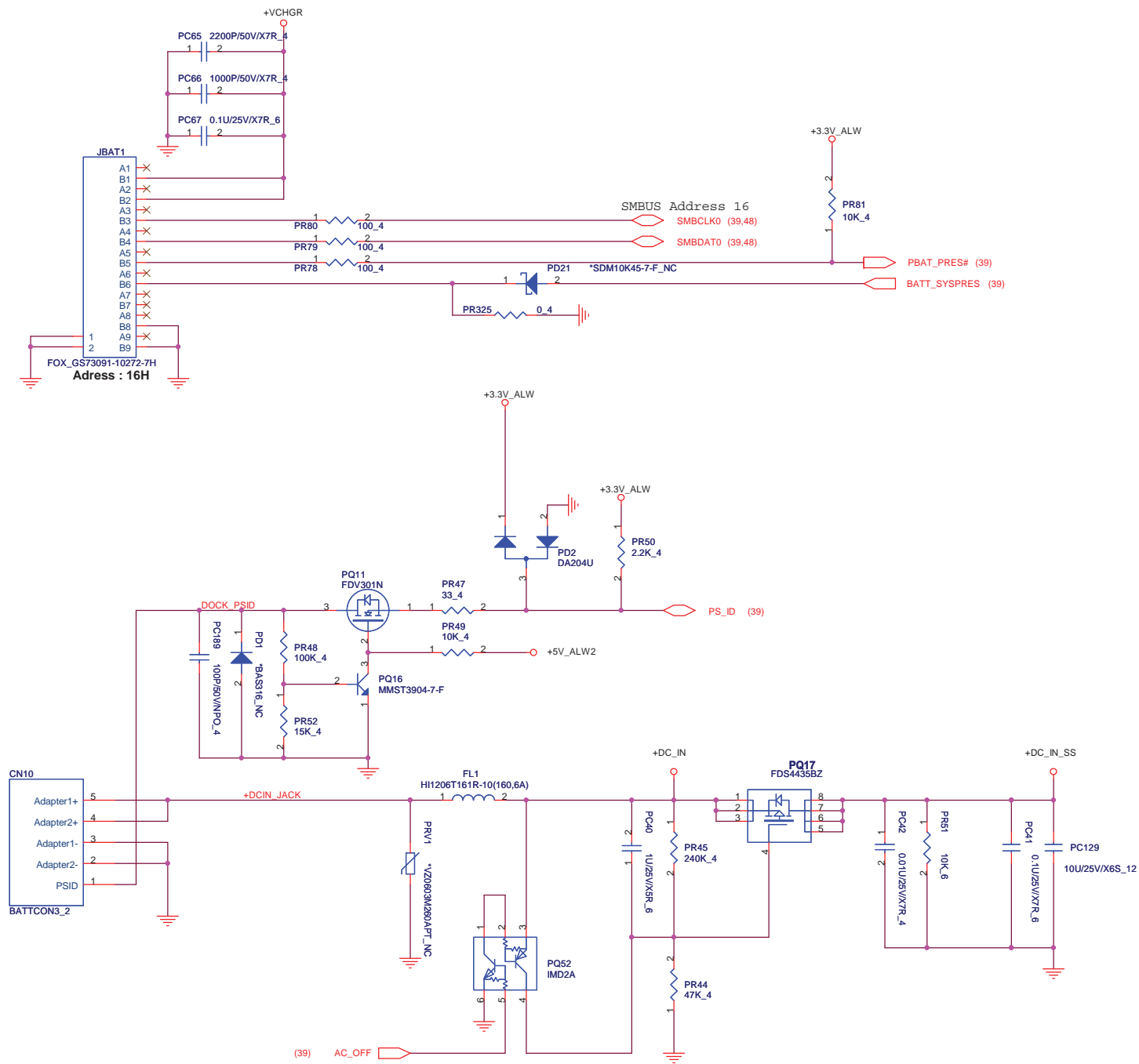


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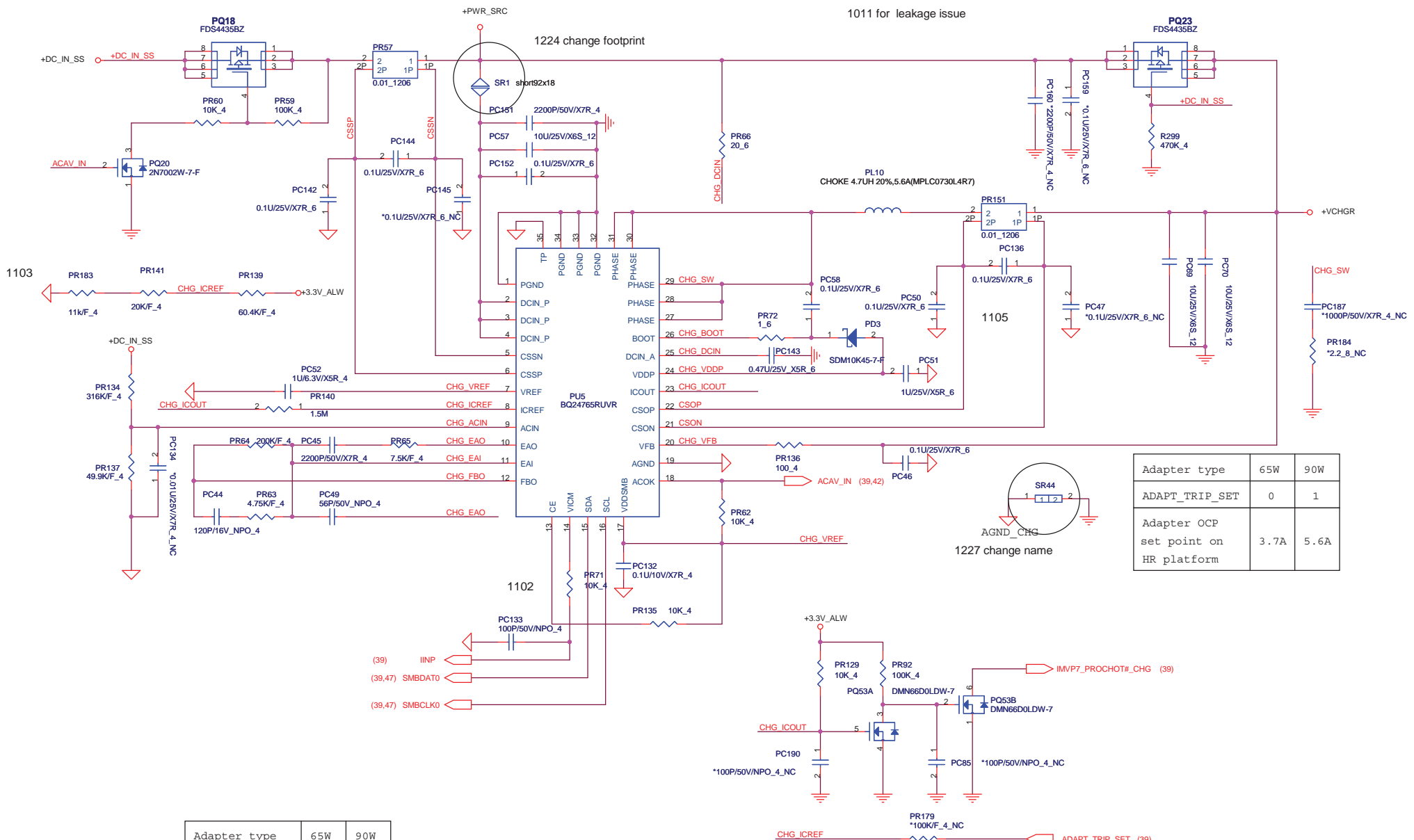
PROJECT : SS8

Size	Document Number	Rev
	BLANK	3A
Date:	Monday, January 03, 2011	Sheet 45 of 57





Charger (BQ24765RUVR)



Adapter type	65W	90W
ADAPT_TRIP_SET	0	1
Adapter OCP set point on HR platform	3.7A	5.6A

Adapter type	65W	90W
ADAPT_TRIP_SET	0	1
Adapter OCP set point on HR platform	3.7A	5.6A

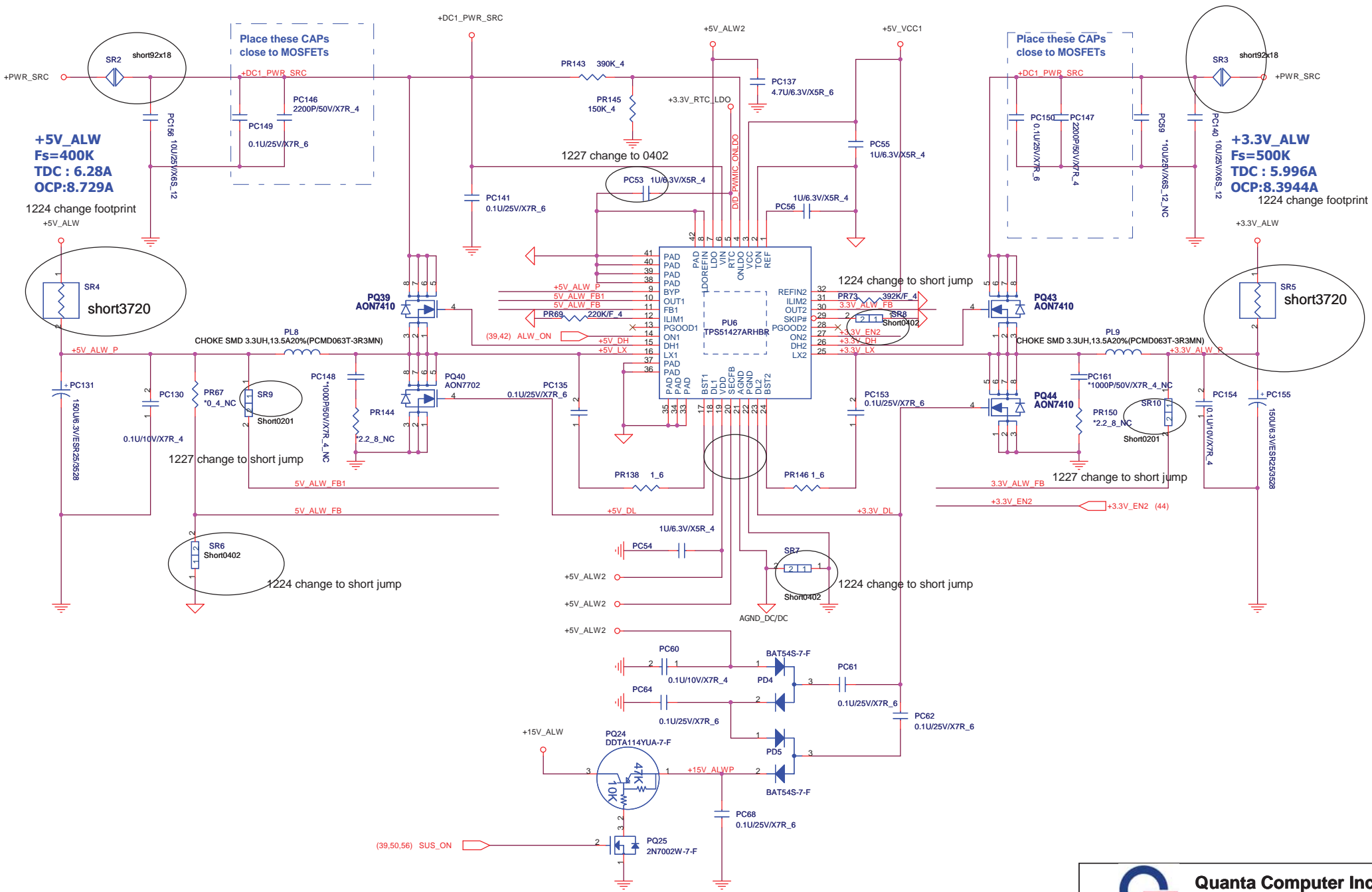
	Only 90 W	65W-90 W
PR179	NA	100K
PR141	20k	10k
PR183	11k	10k


Need GPIO pin with SW team confirm

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Size	Document Number	Rev
	Charger (BQ24765RUVR)	3A
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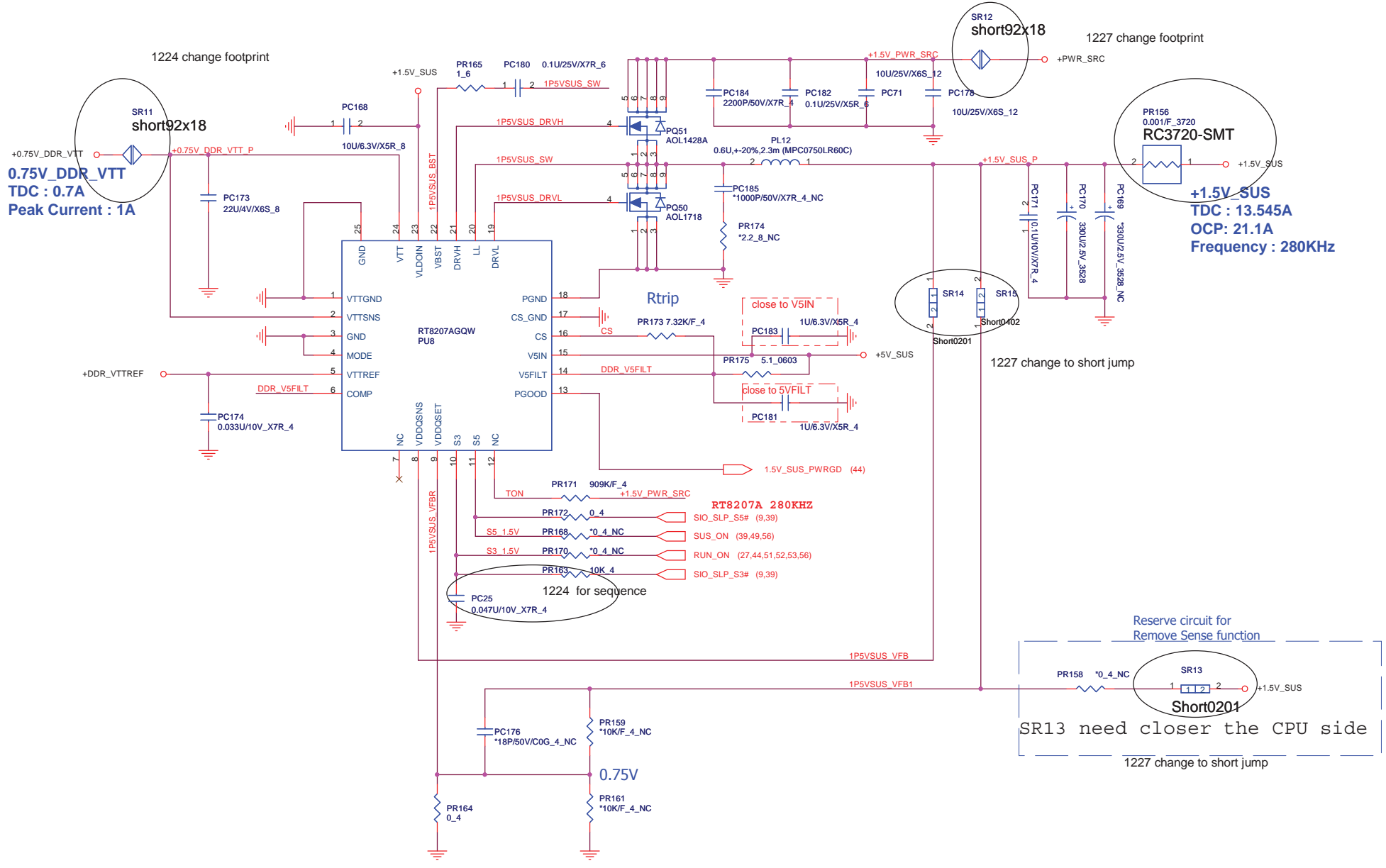
+3.3V_ALW / +5V_SUS / +15V_ALW (TPS51427ARHBR)

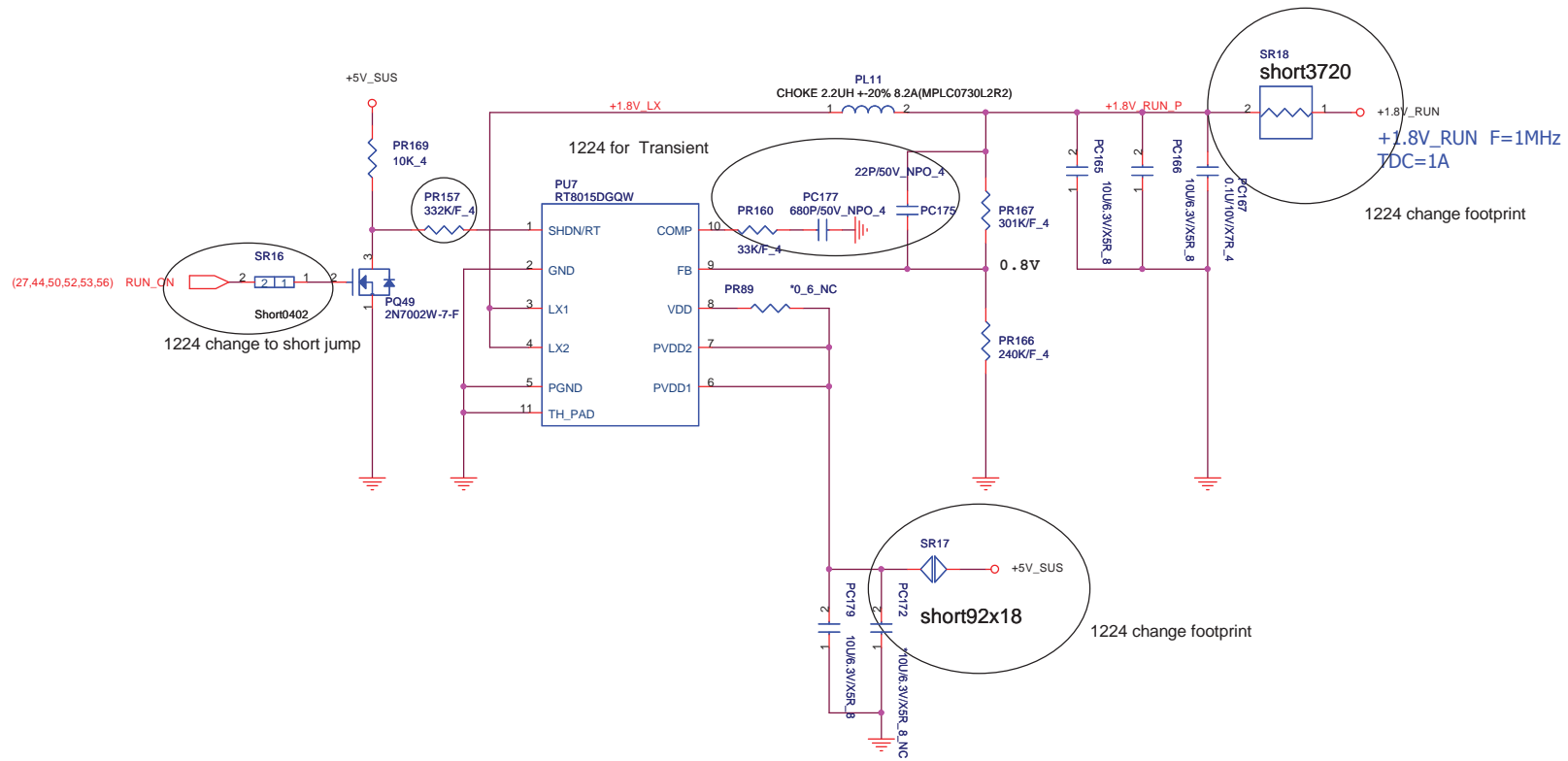



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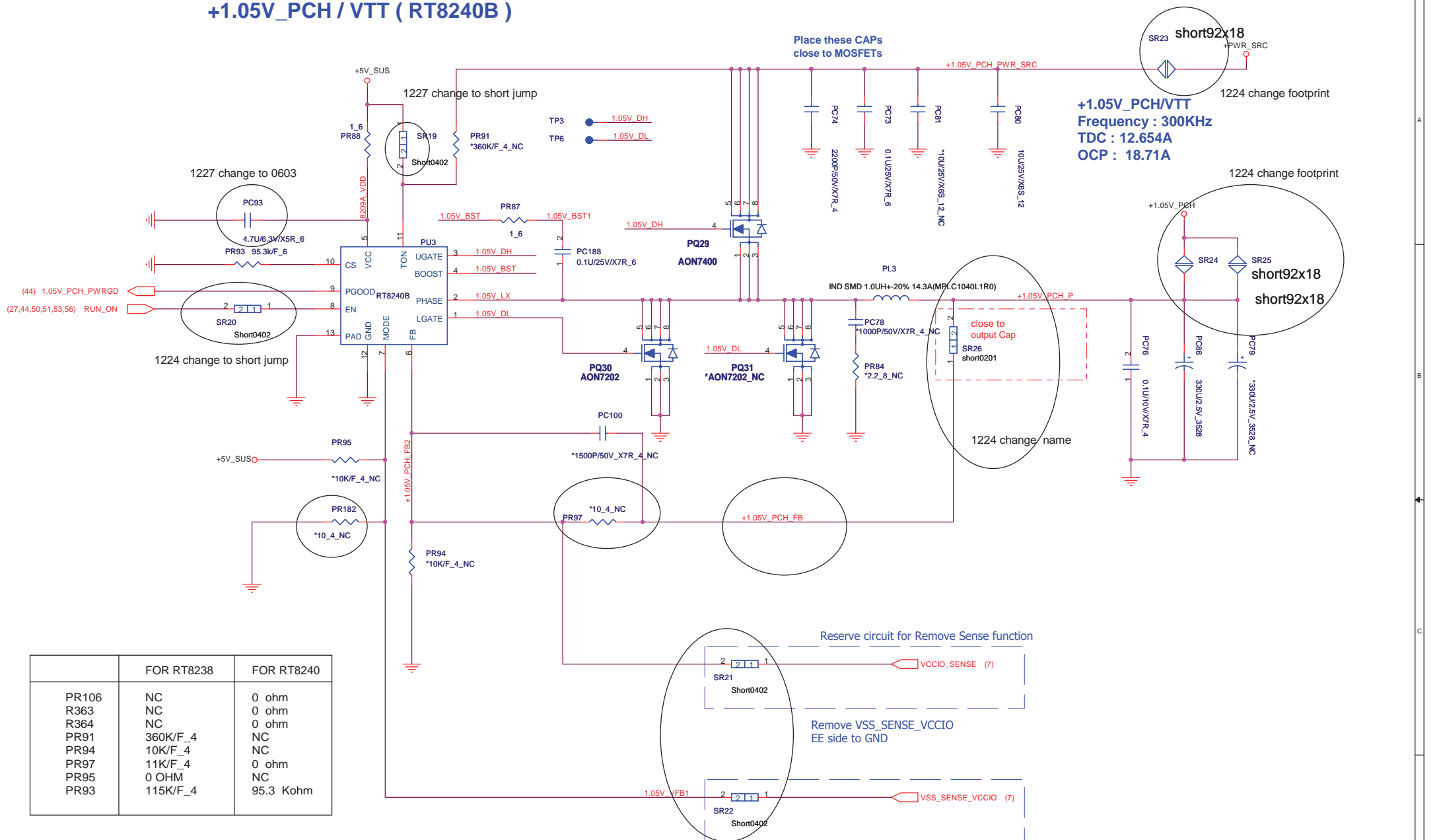
Size	Document Number	Rev
	3.3V_ALW / 5V_ALW (TPS51427ARHBR)	3A
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+1.5V_SUS (RT8207AGQW)





+1.05V_PCH / VTT (RT8240B)



+1.05V_PCH/VTT
Frequency : 300KHz
TDC : 12.654A
OCP : 18.71A

Place these CAPS
close to MOSFETs

1224 change name


Reserve circuit for Remove Sense function

Remove VSS_SENSE_VCCIO
EE side to GND

Remove VSS_SENSE_VCCIO
EE side to GND

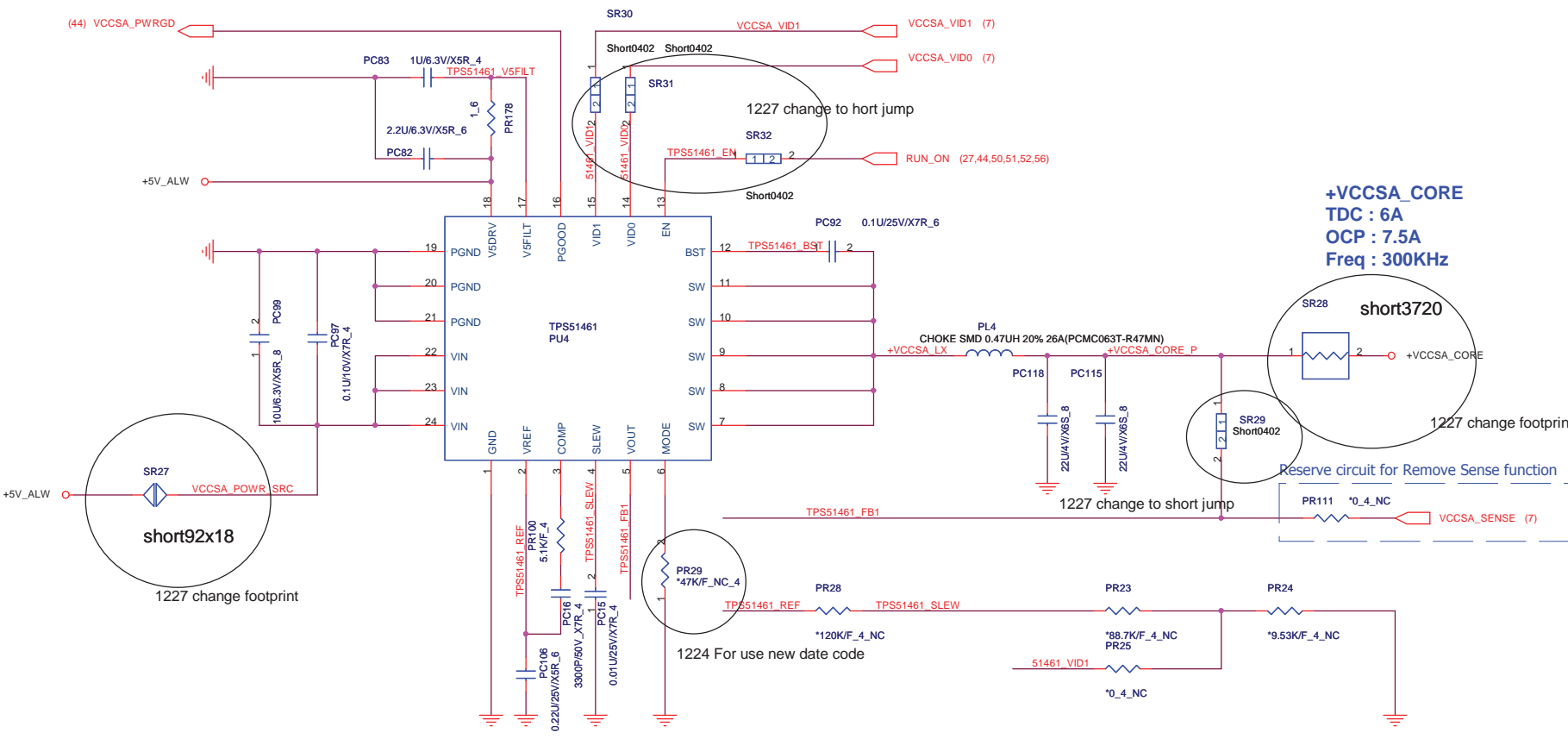
	FOR RT8238	FOR RT8240
PR106	NC	0 ohm
R363	NC	0 ohm
R364	NC	0 ohm
PR91	360K/F_4	NC
PR94	10K/F_4	NC
PR97	11K/F_4	0 ohm
PR95	0 OHM	NC
PR93	115K/F_4	95.3 Kohm

+1.05V_PCH
 Control IC: RT8240
 H/S MOSFET: AO4496 (AOS), Qg=6.1nC, Rds(on)=26mohm, PD:3.1W
 L/S MOSFET: AO4468 (AOS), Qg=12nC, Rds(on)=22mohm, PD:3.1W
 Inductor: 1.5UH+20% 9A (10D40F-1R5M)(TTA), DCR=10.5mohm
 Output Cap: 1*390U, 2.5V(20%, 105C, 6.3*5.8), ESR=10mohm



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Size	Document Number	Rev
	+1.05V_PCH / VTT (RT8240B)	3A
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+VCCSA_CORE
TDC : 6A
OCF : 7.5A
Freq : 300KHz

1227 change to hort jump

1227 change footprint

1227 change to short jump

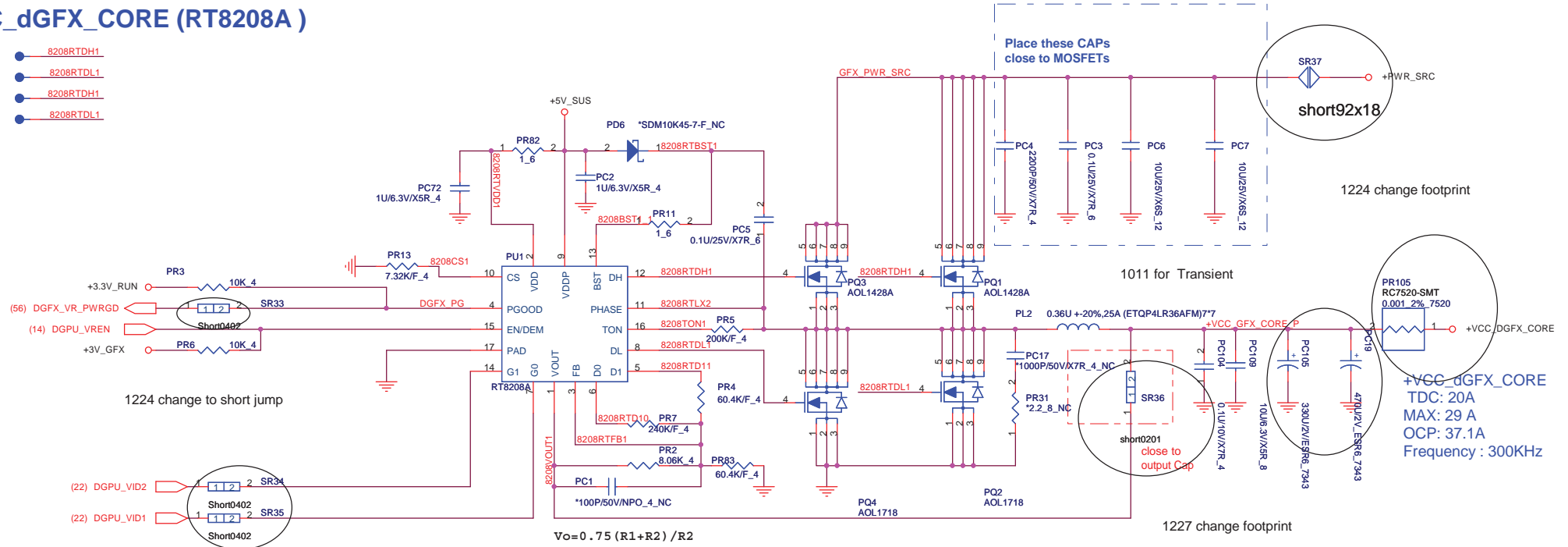
1224 For use new date code

Reserve circuit for Remove Sense function

+VCCSA	VCCSA_VID1	
0.8V	High	
0.9V	Low	Apply now

+VCC_dGFX_CORE (RT8208A)

- TP4 ● 8208RTDH1
- TP8 ● 8208RTDL1
- TP7 ● 8208RTDH1
- TP5 ● 8208RTDL1



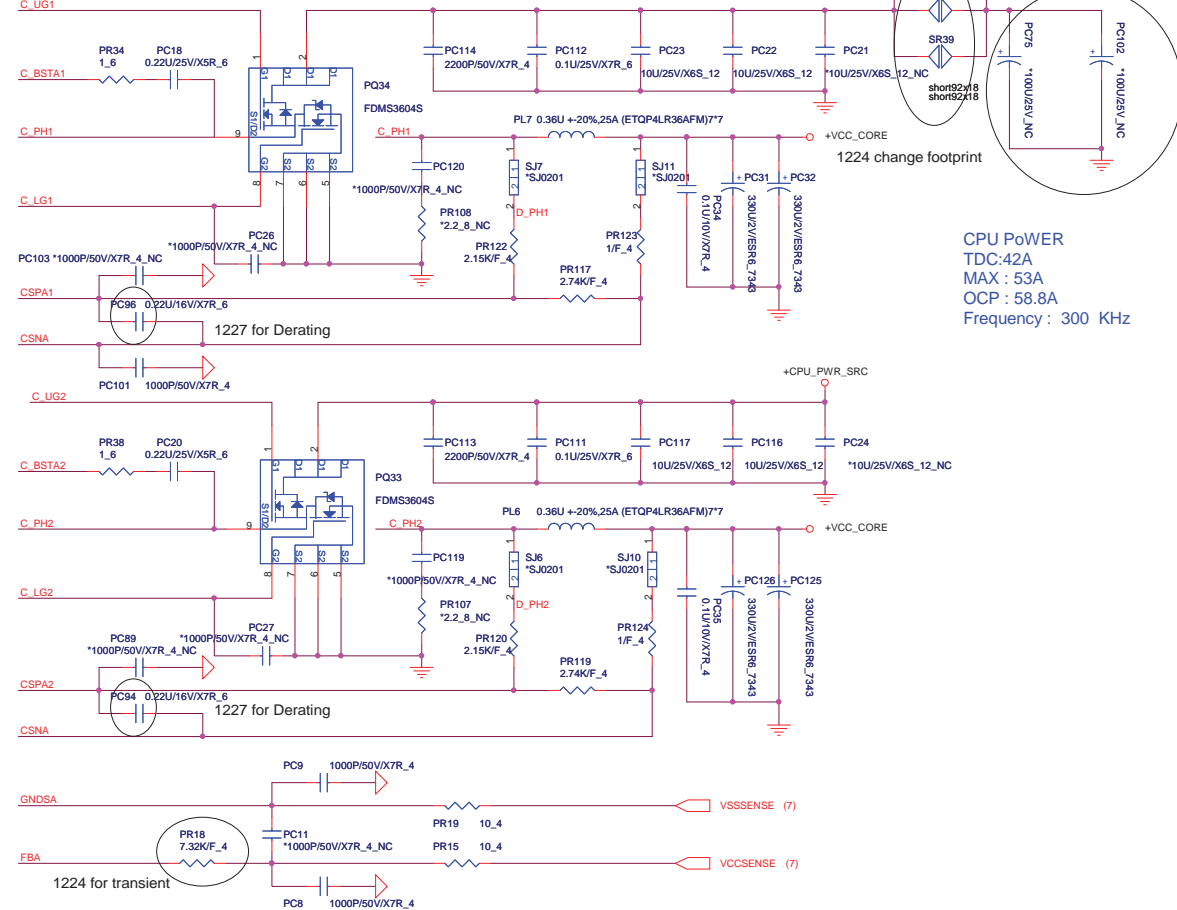
$$V_o = 0.75 (R1 + R2) / R2$$

+VCC_GFX_CORE
 Control IC: RT8208A
 H/S MOSFET: FDMS8692 (Fairchild), Qg=11nC, Rds(on)=14mohm, PD:2.5W
 L/S MOSFET: FDMS7670 (Fairchild), Qg=24nC, Rds(on)=5mohm, PD:2.5W
 Inductor: 0.36UH +-20% 45A (MPO104F-R36H1) (Delta), DCR=0.89mohm
 Output Cap: 2*390U, 2.5V (20%, 105C, 6.3*5.8), ESR=10mohm

DGPU_VID1	DGPU_VID2	+VCC_GFX_CORE
LOW	LOW	0.85V
HIGH	LOW	NA (0.875V)
LOW	HIGH	0.95V
HIGH	HIGH	0.975V

TON1	PR211 = 200K
FREQ	297K

CPU Power



CPU Power
TDC: 42A
MAX : 53A
OCP : 58.8A
Frequency : 300 KHz

12/24 Remove PC77

1224 change footprint

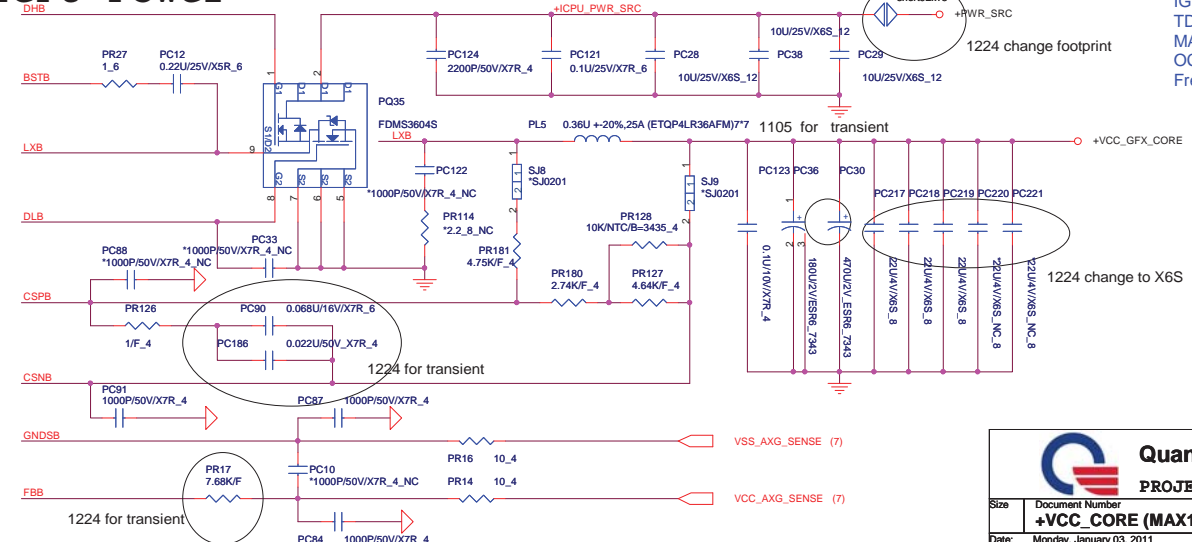
1227 for Derating

1227 for Derating

1227 for Derating

1224 for transient

IGPU Power



IGPU Power
TDC : 21.5A
MAX : 33A
OCP : 39A
Frequency : 330 KHz

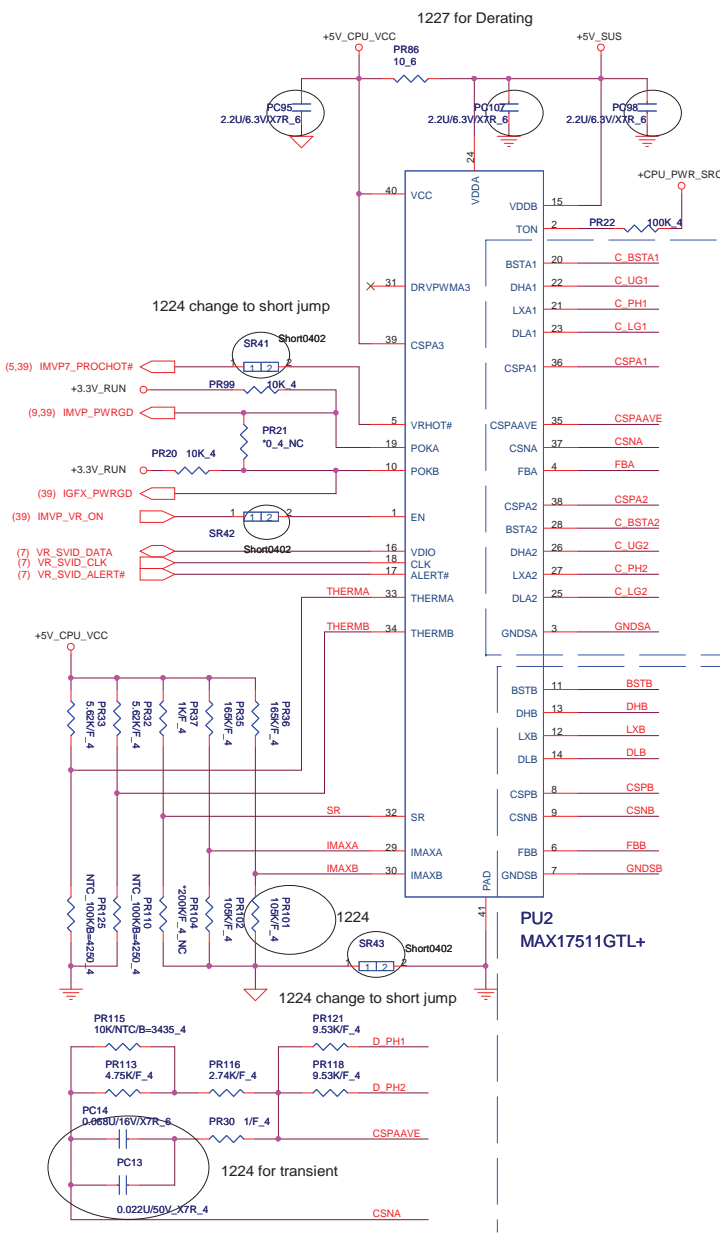
1224 change footprint


1105 for transient

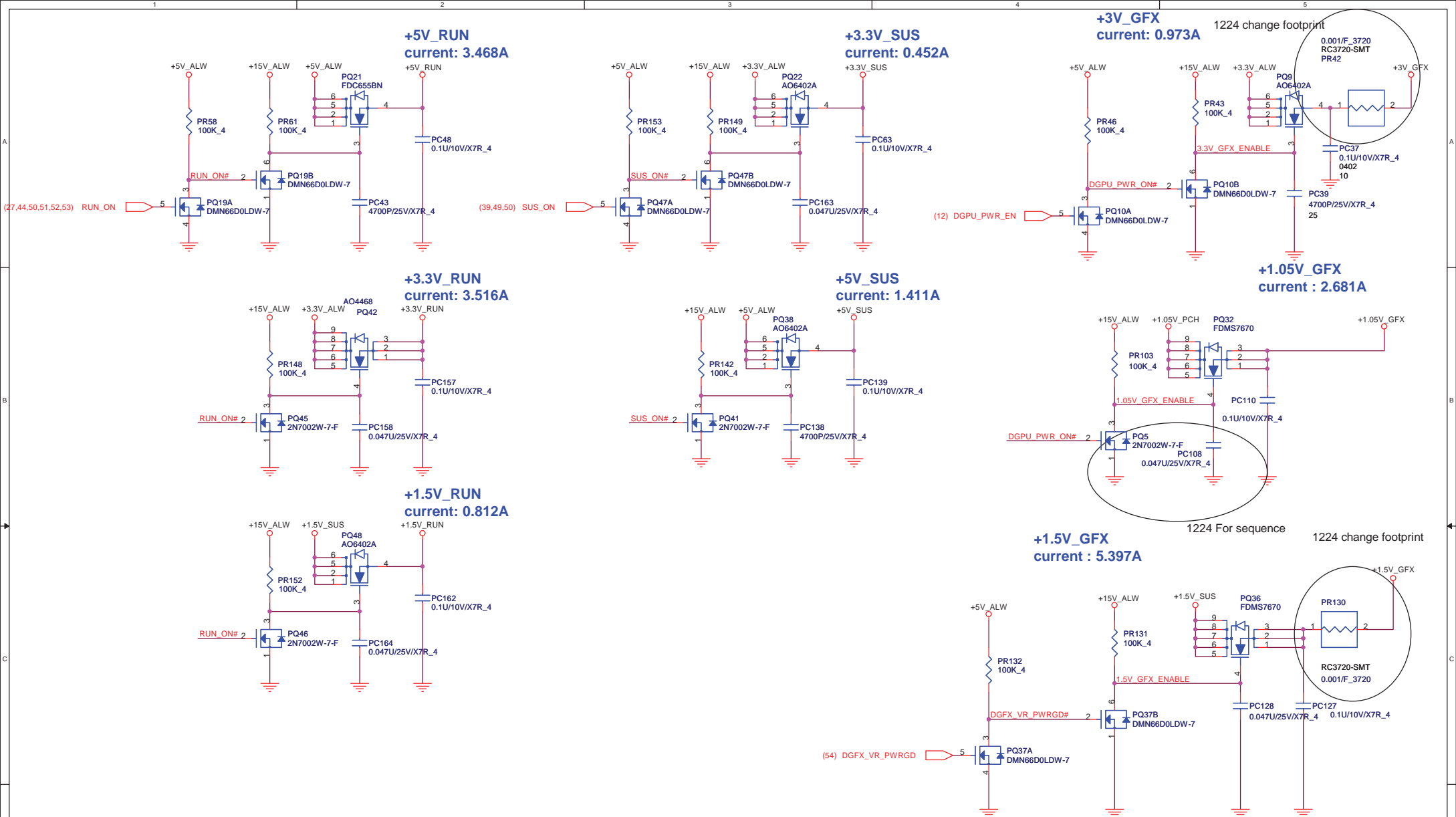
1224 change to X6S

1224 for transient

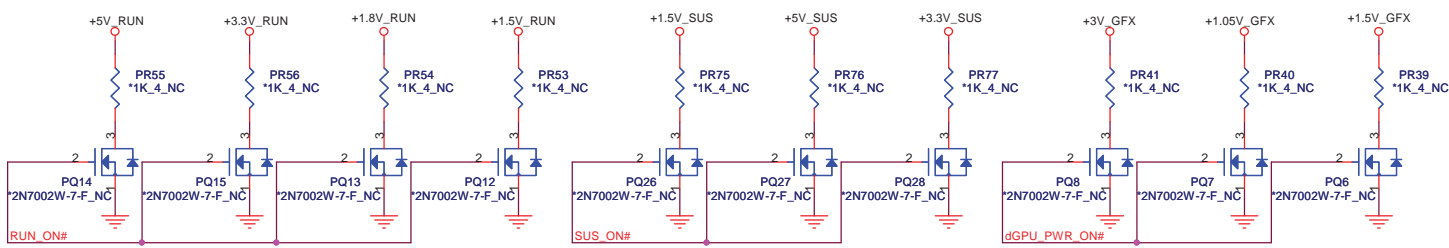
1224 for transient




Quanta Computer Inc.
 PROJECT : SS8
 +VCC_CORE (MAX17511)
 Date: Monday, January 03, 2011 Sheet 55 of 57

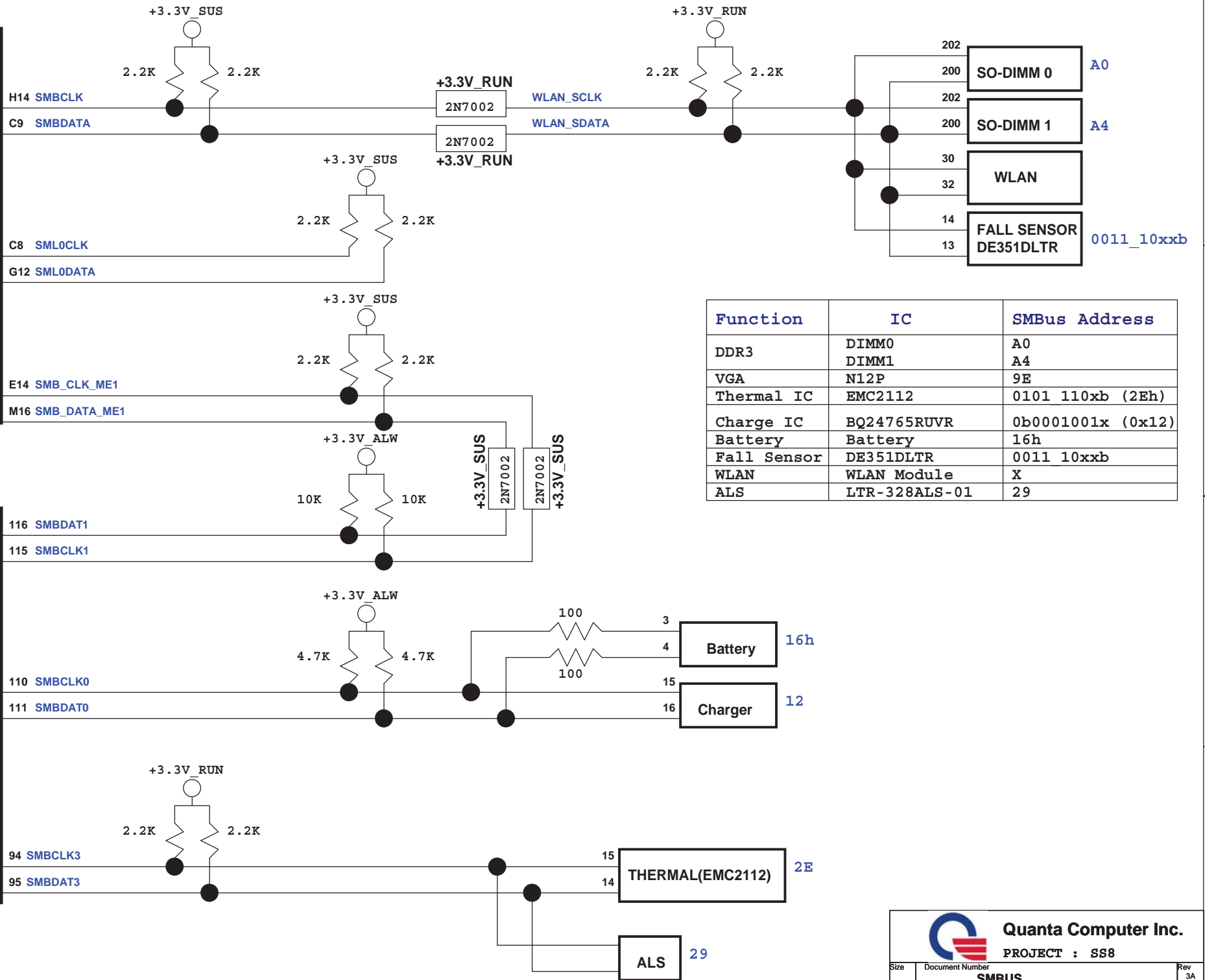
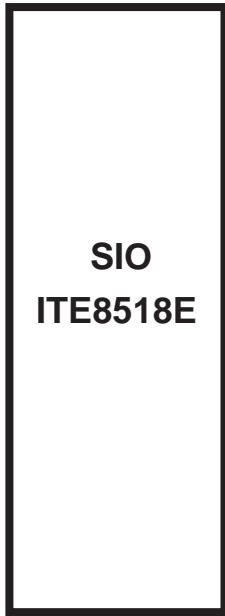
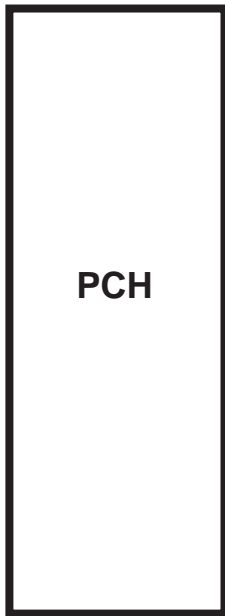


Reserve discharge path



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PROJECT : SS8

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	Load Switch	3A
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Function	IC	SMBus Address
DDR3	DIMM0 DIMM1	A0 A4
VGA	N12P	9E
Thermal IC	EMC2112	0101 110xb (2Eh)
Charge IC	BQ24765RUVR	0b0001001x (0x12)
Battery	Battery	16h
Fall Sensor	DE351DLTR	0011 10xxb
WLAN	WLAN Module	X
ALS	LTR-328ALS-01	29