High-performance Switching Regulators

Flexible Step-down Switching Regulator

BD9778F/HFP, BD9002HFP, BD9781HFP

● Description

The flexible step-down switching regulator is a switching regulator designed with a high voltage built-in POWER MOS FET, providing a free setting function of operating frequency with external resistor. This switching regulator features a wide input voltage range (5 to 35 V or 12 to 46 V) and operating temperature range (-40 to +125˚C). Furthermore, the external synchronization input pin (BD9781HFP) is equipped, enabling synchronous operation with external clock.

● Features

1) Designed with fewer external components
2) Wide input voltage range: 5 to 35 V (BD9778F/HFP and BD9781HFP), 12 to 46 V (BD9002HFP)
3) Built-in P-ch POWER MOS FET
4) Output voltage setting enabled with external resistor: 1 to VIN
5) Reference voltage accuracy: ±2%
6) Wide operating temperature range: -40 to +125˚C
7) Low dropout: 100% ON Duty cycle
8) Stand-by mode supply current: 0 μA (Typ.) (BD9002HFP has no standby function)
9) Oscillation frequency variable with external resistor: 50 to 300 kHz (BD9002HFP), 50 to 500 kHz (BD9778F/HFP and BD9781HFP)
10) External synchronization enabled (only on the BD9781HFP)
11) Soft start function (Soft start time adjustable with external capacitor on the BD9002HFP. On other Series, soft start time fixed to 5 ms (Typ.)
12) Built-in overcurrent protection circuit
13) Built-in thermal shutdown protection circuit
14) High power HRP7 package mounted (BD9778HFP, BD9002HFP, and BD9781HFP) Compact SOP8 package mounted (BD9778F)

● Use

All fields of industrial equipment, such as TV, printer, DVD, projector, pinball machine, PC, car stereo, car navigation, communication like ETC, AV, and OA.

● Lineup

Item	BD9778F/HFP	BD9002HFP	BD9781HFP
Output current	2A	2.5A	4A
Input range	5 ~ 35V	12 ~ 46V	5 ~ 35V
Oscillation frequency range	50 ~ 500kHz	50 ~ 300kHz	50 ~ 500kHz
External synchronization	Not provided	Not provided	Provided
Standby function	Provided	Not provided	Provided
Operating temperature	−40 ~ +125˚C	−40 ~ +125˚C	−40 ~ +125˚C
Package	SOP8 / HRP7	HRP7	HRP7

● Absolute Maximum Ratings (Ta = 25°C)

Parameter		Symbol	Limits	Unit
Power supply voltage	BD9778F/HFP,BD9781HFP	V_{IN}	36	V
	BD9002HFP		50	
Output switch pin voltage		V_{SW}	V_{IN}	V
Output switch current	BD9778F/HFP	I_{SW}	2 *1	A
	BD9002HFP		2.5 *1	
	BD9781HFP		4 *1	
EN/SYNC, EN pin voltage		$V_{EN/SYNC}$,V_{EN}	V_{IN}	V
SS, RT, FB, INV pin voltage		V_{SS},V_{RT},V_{FB},V_{INV}	7	
Power dissipation	HRP7	Pd	5.5 *2	W
	SOP8		0.69 *3	
Operating temperature range		Topr	−40 ~ +125	°C
Storage temperature range		Tstg	−55 ~ +150	°C
Maximum junction temperature		Tjmax	150	°C

*1 Should not exceed Pd-value.
*2 Should be derated by 44 mW/°C at Ta=25°C or more, when mounted on 2-layer PCB of 70 × 70 × 1.6 mm³.
(PCB incorporates thermal via. Copper foil area on the front side of PCB: 10.5 × 10.5 mm². Copper foil area on the reverse side of PCB: 70 × 70 mm²)
*3 Should be derated by 5.52 mW/°C at Ta=25°C or more, when mounted on 2-layer PCB of 70 × 70 × 1.6 mm³.

● Recommended operating range

Parameter	BD9778F/HFP	BD9002HFP	BD9781HFP	Unit
Operating power supply voltage	5 ~ 35	12 ~ 46	5 ~ 35	V
Output switch current	~ 2	~ 2.5	~ 4	A
Output voltage (ON Duty)	6 ~ 100	6 ~ 100	6 ~ 100	%
Oscillation frequency	50 ~ 500	50 ~ 300	50 ~ 500	kHz
Oscillation frequency set resistance	40 ~ 800	100 ~ 800	39 ~ 800	kΩ

● Electrical characteristics

◎BD9778F/HFP (Unless otherwise specified, Ta = -40 to +125°C, V_{IN} =13.2 V, V_{EN} = 5 V)

Parameter	Symbol	Limits			Unit	Condition
		Min.	Typ.	Max.		
Circuit current	I_Q	−	3	4.2	mA	I_O=0A
[SW block]						
POWER MOS FET ON resistance	R_{ON}	−	0.53	0.9	Ω	I_{SW}=50mA
Operating output current of overcurrent protection	I_{OLIMIT}	2	4	−	A	* Design assurance
Output leak current	I_{OLEAK}	−	0	30	μA	V_{IN}=35V,V_{EN}=0V
[Error Amp block]						
Reference voltage	V_{REF}	0.96	1.00	1.04	V	V_{FB}=V_{INV}
Reference voltage input regulation	ΔVREF	−	0.5	−	%	V_{IN}=5 ~ 35V
Input bias current	I_B	−1	−	−	μA	V_{INV}=1.1V
Maximum FB voltage	V_{FBH}	2.4	2.5	−	V	V_{INV}=0.5V
Minimum FB voltage	V_{FBL}	−	0.05	0.10	V	V_{INV}=1.5V
FB sink current	I_{FBSINK}	−5.0	−3.0	−0.5	mA	V_{FB}=1.5V,V_{INV}=1.5V
FB source current	$I_{FBSOURCE}$	70	120	170	μA	V_{FB}=1.5V,V_{INV}=0.5V
Soft start time	T_{SS}	−	5	−	mS	* Design assurance
[Oscillator block]						
Oscillation frequency	Fosc	82	102	122	kHz	R_T=390kΩ
Frequency input regulation	ΔFosc	−	1	−	%	V_{IN}=5 ~ 35V
[Enable block]						
Threshold voltage	V_{EN}	0.8	1.7	2.6	V	
Input current	I_{EN}	−	13	50	μA	V_{EN}=5V

* Not designed for radiation resistance.

◎BD9002HFP (Unless otherwise specified, Ta=−40 ~ +125°C,V_{IN}=13.2V)

Parameter	Symbol	Limits			Unit	Condition
		Min.	Typ.	Max.		
Circuit current	I_Q	−	3	8	mA	I_O=0A
[SW block]						
POWER MOS FET ON resistance	R_{ON}	−	0.6	1.2	Ω	I_{SW}=50mA
Operating output current of overcurrent protection	I_{OLIMIT}	2.5	4	−	A	* Design assurance
[Error Amp block]						
Reference voltage	V_{REF}	0.96	1.00	1.04	V	V_{FB}=V_{INV}
Reference voltage input regulation	ΔVREF	−	0.5	−	%	V_{IN}=12 ~ 46V
Input bias current	I_B	−1	−	−	μA	V_{INV}=0.9V
Maximum FB voltage	V_{FBH}	2.4	2.5	−	V	V_{INV}=0.5V
Minimum FB voltage	V_{FBL}	−	0.05	0.10	V	V_{INV}=1.5V
FB sink current	I_{FBSINK}	−5.0	−3.0	−0.5	mA	V_{FB}=1.5V,V_{INV}=1.5V
FB source current	$I_{FBSOURCE}$	70	120	170	μA	V_{FB}=1.5V,V_{INV}=0.5V
[Oscillator block]						
Oscillation frequency	F_{OSC}	82	102	122	kHz	R_T=360kΩ
Frequency input regulation	ΔFOSC	−	2	−	%	V_{IN}=12 ~ 46V
[UVLO detection block]						
Threshold voltage	V_{UVLO}	9.0	9.5	10.0	V	Output ON
Hysteresis width	V_{HYS}	0.2	0.5	0.8	V	Output OFF
[Soft start block]						
Charge current	I_{SS}	−4.0	−2.5	−1.0	μA	V_{SS}=1.0V
Threshold voltage	V_{SS}	−	1.0	−	V	V_{INV} = 1.0 V, SS voltage
Standby voltage	V_{SSSTB}	−	10	100	mV	SS voltage
Output OFF threshold voltage	V_{THOFF}	0.2	0.31	−	V	SS voltage

* Not designed for radiation resistance.

◎BD9781HFP (Unless otherwise specified, Ta=−40 ~ +125°C,V_{IN}=13.2V,$V_{EN/SYNC}$=5V)

Parameter	Symbol	Limits			Unit	Condition
		Min.	Typ.	Max.		
Circuit current	I_Q	−	3	8	mA	I_O=0A
[SW block]						
POWER MOS FET ON resistance	R_{ON}	−	0.5	0.9	Ω	I_{SW}=50mA
Operating output current of overcurrent protection	I_{OLIMIT}	4	6	−	A	* Design assurance
Output leak current	I_{OLEAK}	−	0	30	μA	V_{IN}=35V,$V_{EN/SYNC}$=0V
[Error Amp block]						
Reference voltage	V_{REF}	0.97	1.00	1.03	V	V_{FB}=V_{INV}
Reference voltage input regulation	ΔVREF	−	0.5	−	%	V_{IN}=5 ~ 35V
Input bias current	I_B	−1	−	−	μA	V_{INV}=1.1V
Maximum FB voltage	V_{FBH}	2.4	2.5	−	V	V_{INV}=0.5V
Minimum FB voltage	V_{FBL}	−	0.05	0.10	V	V_{INV}=1.5V
FB sink current	I_{FBSINK}	−5.0	−3.0	−0.5	mA	V_{FB}=1.5V,V_{INV}=1.5V
FB source current	$I_{FBSOURCE}$	70	120	170	μA	V_{FB}=1.5V,V_{INV}=0.5V
Soft start time	T_{SS}	−	5	−	mS	* Design assurance
[Oscillator block]						
Oscillation frequency	F_{OSC}	82	102	122	kHz	R_T=390kΩ
Frequency input regulation	ΔFOSC	−	1	−	%	V_{IN}=5 ~ 35V
[Enable/Synchronizing input block]						
Threshold voltage	$V_{EN/SYNC}$	0.8	1.7	2.6	V	
Input current	$I_{EN/SYNC}$	−	35	90	μA	$V_{EN/SYNC}$=5V
External synchronizing frequency	F_{SYNC}	−	150	−	kHz	$F_{EN/SYNC}$=150kHz

* Not designed for radiation resistance.

● Reference data

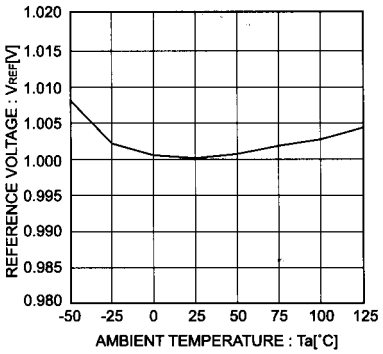


Fig.1 Output reference voltage vs. Ambient temperature (All series)

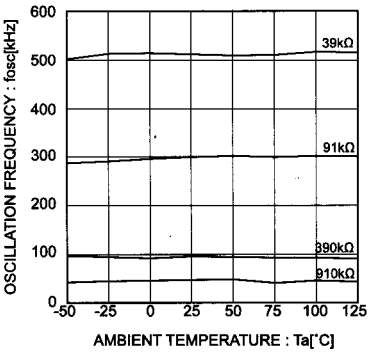


Fig.2 Frequency vs. Ambient temperature (All series)

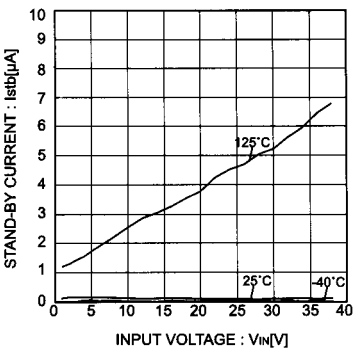


Fig.3 Stand-by current (BD9781HFP)

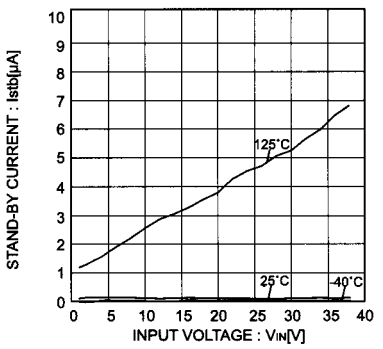


Fig.4 Stand-by current (BD9778F/HFP)

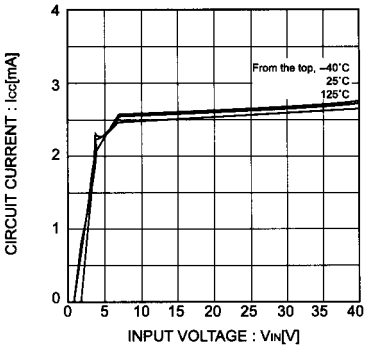


Fig.5 Circuit current (BD9781HFP)

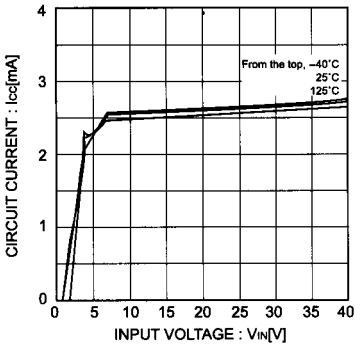


Fig.6 Circuit current (BD9778F/HFP)

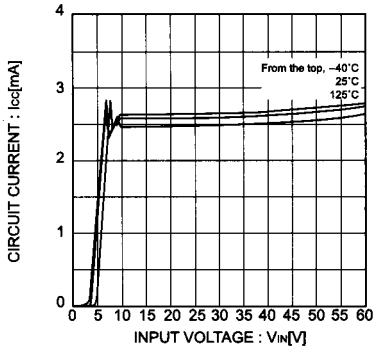


Fig.7 Circuit current (BD9002HFP)

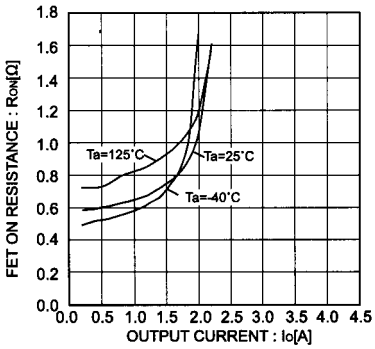


Fig.8 ON resistance VIN = 5V (BD9781HFP)

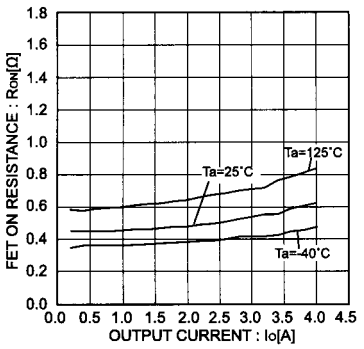


Fig.9 ON resistance VIN=7V (BD9781HFP)

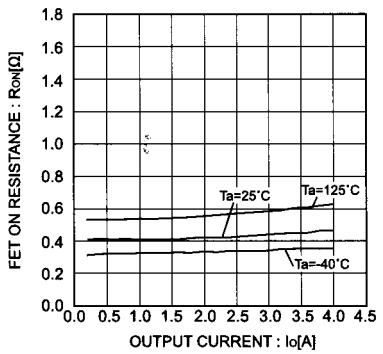


Fig.10 ON resistance VIN=13.2V (BD9781HFP)

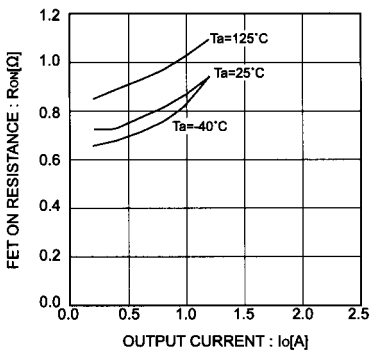


Fig.11 ON resistance VIN=5V (BD9778F/HFP)

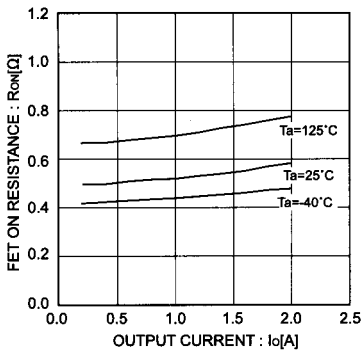


Fig.12 ON resistance VIN=7V (BD9778F/HFP)

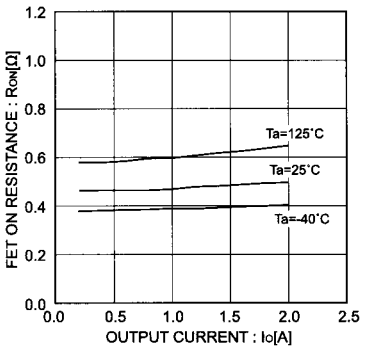


Fig.13 ON resistance VIN=13.2V (BD9778F/HFP)

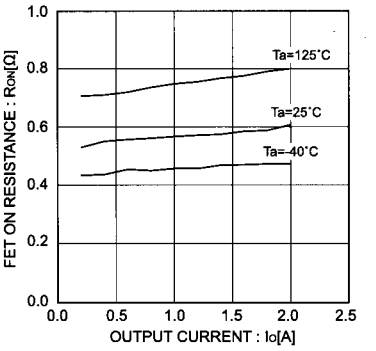


Fig.14 ON resistance VIN=12V (BD9002HFP)

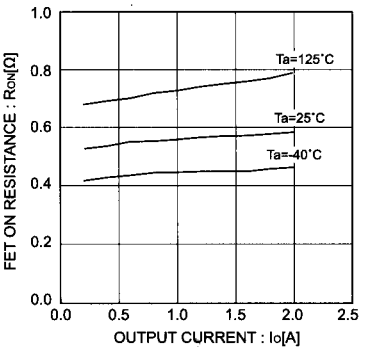


Fig.15 ON resistance VIN=13.2V (BD9002HFP)
(Dropout voltage can be calculated by the expression, RON × IO)

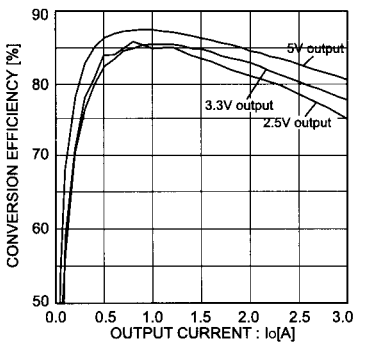


Fig.16 Io vs. Efficiency (VIN=12V,f=200kHz)
(BD9781HFP)

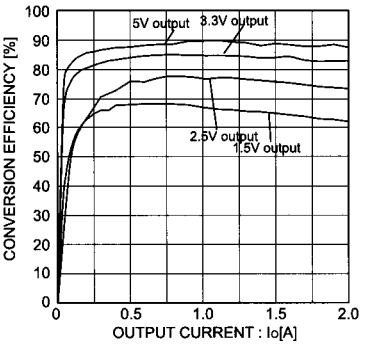


Fig.17 Io vs. Efficiency (VIN=12V,f=100kHz)
(BD9778F/HFP)

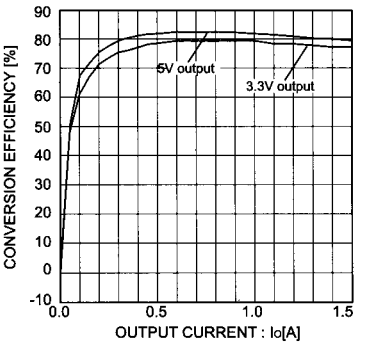


Fig.18 Io vs. Efficiency (VIN=42V,f=200kHz)
(BD9002HFP)

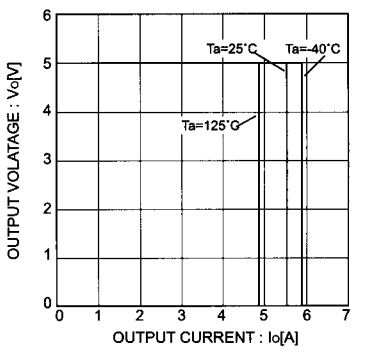


Fig.19 Over current protection (BD9781HFP)

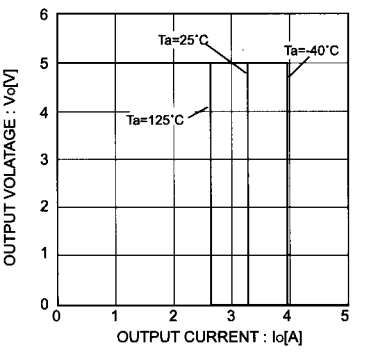


Fig.20 Over current protection (BD9778F/HFP)

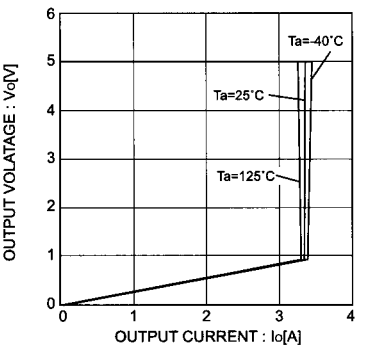


Fig.21 Over current protection (BD9002HFP)

● Block diagram / Application circuit / Pin assignment

(BD9778F)

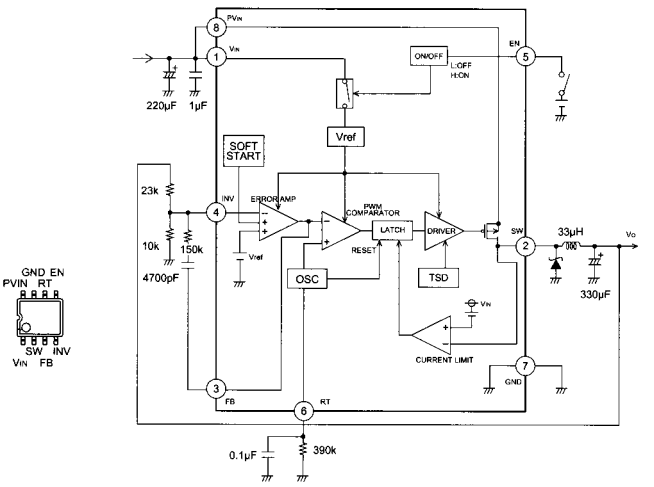


Fig.22

No.	Pin name	Function
1	VIN	Power supply input
2	SW	Output
3	FB	Error Amp output
4	INV	Output voltage feedback
5	EN	Enable
6	RT	Frequency setting resistor connection
7	GND	Ground
8	PVIN	Power system power supply input

(BD9778HFP)

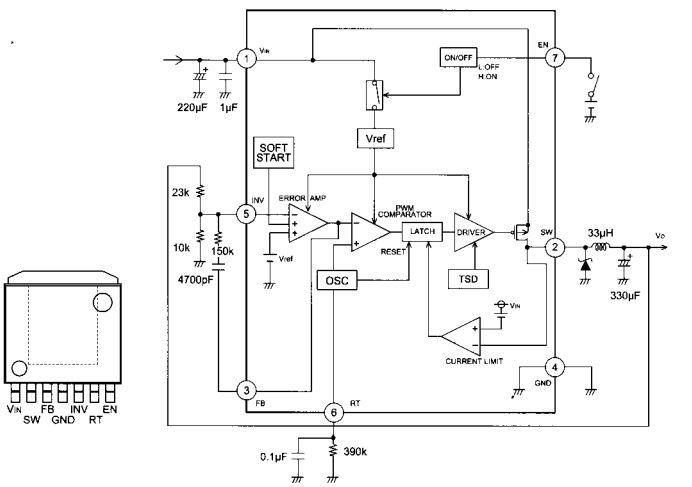


Fig.23

No.	Pin name	Function
1	VIN	Power supply input
2	SW	Output
3	FB	Error Amp output
4	GND	Ground
5	INV	Output voltage feedback
6	RT	Frequency setting resistor connection
7	EN	Enable
FIN	–	Ground

(BD9002HFP)

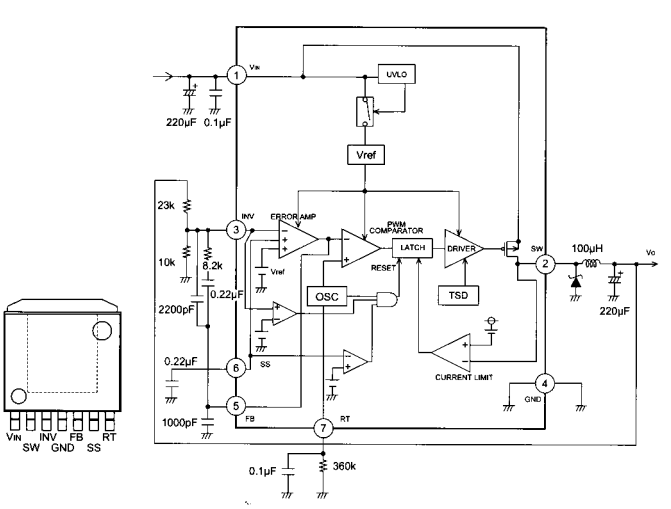


Fig.24

No.	Pin name	Function
1	VIN	Power supply input
2	SW	Output
3	INV	Output voltage feedback
4	GND	Ground
5	FB	Error Amp output
6	SS	Soft start
7	RT	Frequency setting resistor connection
FIN	–	Ground

(BD9781HFP)

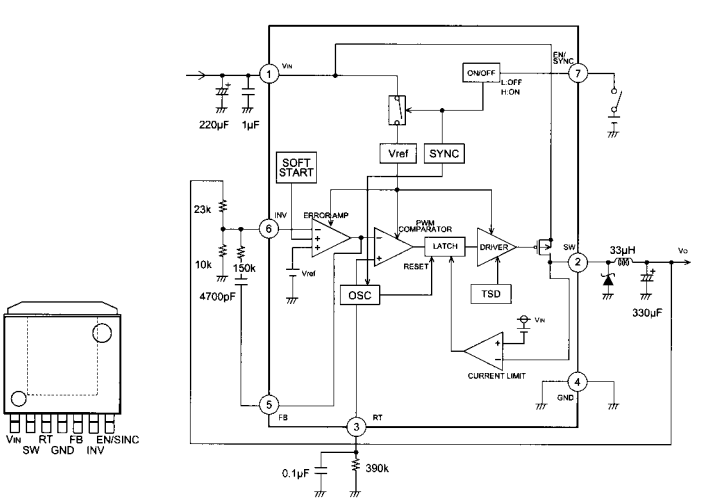


Fig.25

No.	Pin name	Function
1	VIN	Power supply input
2	SW	Output
3	RT	Frequency setting resistor connection
4	GND	Ground
5	FB	Error Amp output
6	INV	Output voltage feedback
7	EN/SYNC	Enable/Synchronizing pulse input
FIN	–	Ground

● Description of operations

- ERROR AMP
  The ERROR AMP block is an error amplifier used to input the reference voltage (1 V typ.) and the "INV" pin voltage. The output "FB" pin controls the switching duty and also output voltage Vo. These "INV" and "FB" pins are externally mounted to facilitate phase compensation. Inserting a capacitor and resistor between these pins enables adjustment of phase margin. (Refer to recommended examples on page 11.)

- SOFT START
  The SOFT START block provides a function to prevent the overshoot of the output voltage Vo through gradually increasing the normal rotation input of the error amplifier when power supply turns ON to gradually increase the switching Duty. The soft start time is set to 5 msec (Typ.). On the BD9002HFP, however, this soft start time can be adjusted with a capacitor connected to the "SS" pin. For details of the soft start time setting, refer to information in Description of external components on page 10.

- ON/OFF(BD9778F/HFP,BD9781HFP)
  Setting the "EN" pin to 0.8 V or less makes it possible to shut down the circuit. Standby current is set to 0 μA (Typ.). Furthermore, on the BD9781HFP, applying a pulse having a frequency higher than set oscillation frequency to the "EN/SYNC" pin allows for external synchronization (up to +50% of the set frequency).

- PWM COMPARATOR
  The PWM COMPARATOR block is a comparator to make comparison between the "FB" pin and internal triangular wave and output a switching pulse.
  The switching pulse duty varies with the "FB" value and can be set in the range of 0 to 100%.

- OSC(Oscillator)
  The OSC block is a circuit to generate a triangular wave to be input in the PWM comparator. Connecting a resistor to the "RT" pin enables setting of oscillation frequency.

- TSD(Thermal Shut Down)
  In order to prevent thermal destruction/thermal runaway of this IC, the TSD block will turn OFF the output when the chip temperature reaches approximately 150˚C or more. When the chip temperature falls to a specified level, the output will be reset. However, since the TSD is absolutely designed to protect the IC itself, the thermal design should be provided with the thermal shutdown detection temperature of approximately less than 150˚C.

- CURRENT LIMIT
  While the output POWER P-ch MOS FET is ON, if the voltage between drain and source (ON resistance × load current) exceeds the reference voltage internally set with the IC, this block will turn OFF the output to latch. The overcurrent protection detection values have been set as shown below, respectively.
  BD9781HFP . . . 8A(Typ.)
  BD9002HFP,BD9778F/HFP . . . 4A(Typ.)

  Furthermore, since this overcurrent protection is automatically reset, after the output is turned OFF and latched, the latch will be reset with the RESET signal output by each oscillation frequency. In the case of BD9002HFP, however, if the output voltage drops below 20% of the set voltage, the output will be completely turned OFF and latched. In order to restart the circuit, the V_{IN} should be reset.

  However, this protection circuit is only effective to prevent destruction due to a sudden accident but does not support for the continuous operation of the protection circuit (e.g. if a load, which significantly exceeds the output current capacitance, is normally connected). Furthermore, since the overcurrent protection detection value has characteristic negative to temperatures, give consideration to the thermal design.

● Timing chart
(BD9781HFP)

• While in basic operation mode

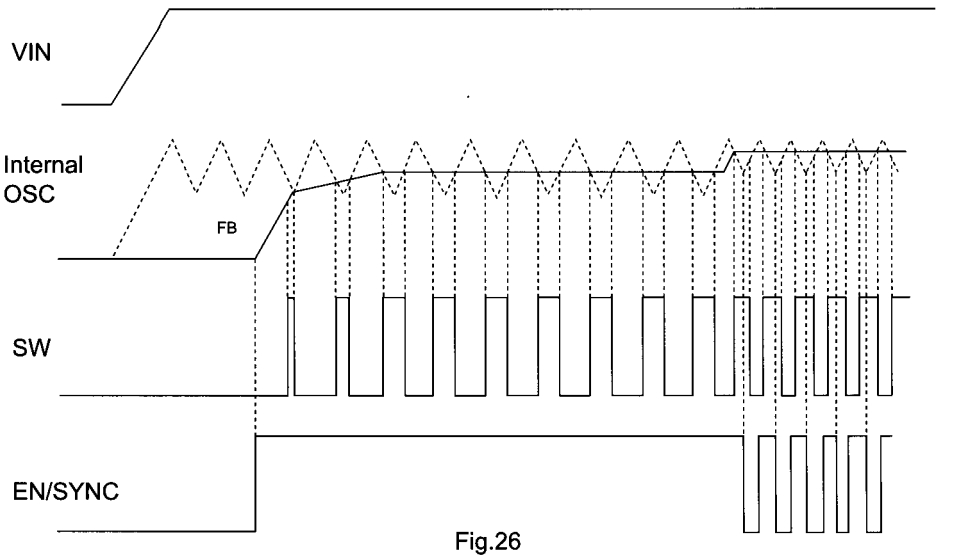


Fig.26

• While in overcurrent protection mode

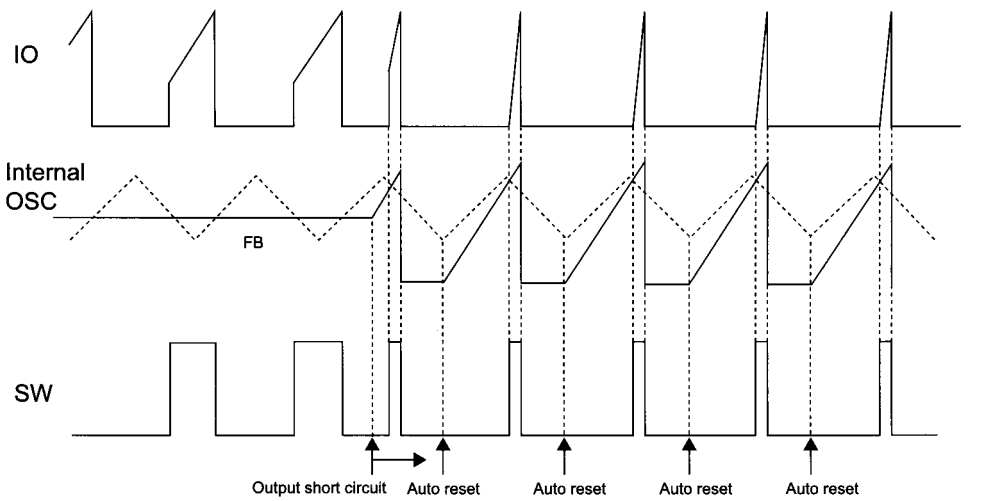


Fig.27

● External synchronizing function (BD9781HFP)

In order to activate the external synchronizing function, connect the frequency setting resistor to the RT pin and then input a synchronizing signal to the EN/SYNC pin.
As the synchronizing signal, input a pulse wave higher than a frequency determined with the setting resistor (RT).
On the BD9781HFP, design the frequency difference to be within 50%.
Furthermore, make setting of the pulse wave duty in the range of 10% to 90%.

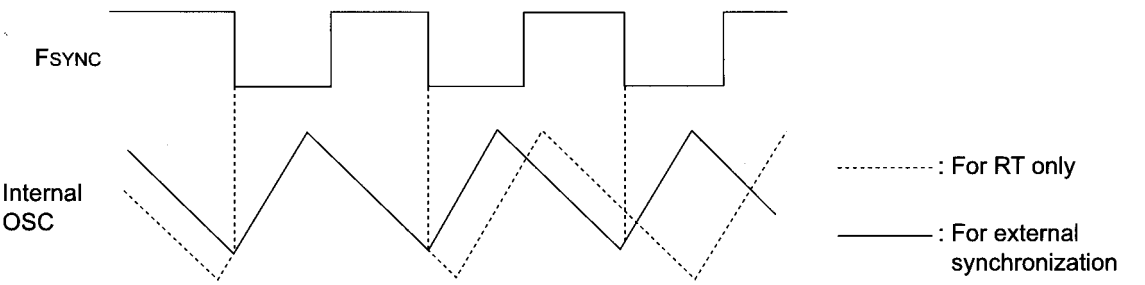


Fig.28

● Description of external components

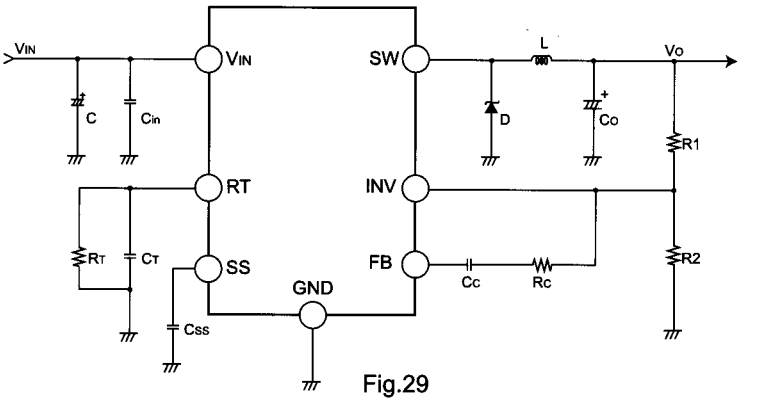


Fig.29

Design procedure	Calculation example
Vo = Output voltage, Vin (Max.) = Maximum input voltage Io (Max.) = Maximum load current, f = Oscillation frequency 1. Setting or output voltage Output voltage can be obtained by the formula shown below. $Vo=1 \times (1+R1/R2)$ Use the formula to select the R1 and R2. Furthermore, set the R2 to 30 kΩ or less. Select the current passing through the R1 and R2 small enough for the output current.	When Vo = 5 V and R2 = 10 kΩ, $5=1 \times (1+R1/10k\Omega)$ R1=40kΩ
2. Selection of coil (L) The value of the coil can be obtained by the formula shown below. $L=(V_{IN}-Vo) \times Vo / (V_{IN} \times f \times \Delta Io)$ ΔIo: Output ripple current f = Operating frequency Normally, ΔIo should be approximately 10 to 20% of Io. If this coil is not set to the optimum value, normal (continuous) oscillation may not be achieved. Furthermore, set the value of the coil with an adequate margin so that the peak current passing through the coil will not exceed the rated current of the coil.	When V_{IN} = 13.2 V, Vo = 5 V, Io = 2 A, and f = 100 kHz, $L=(13.2-5) \times 5/13.2 \times 1/100k \times 1/(2 \times 0.15)$ $=103.5\mu H \fallingdotseq 100\mu$ L=100μH
3. Selection of output capacitor (Co) The output capacitor can be determined according to the output ripple voltage ΔVo (p-p) required. Obtain the required ESR value by the formula shown below and then select the capacitance. $\Delta IL=(V_{IN}-Vo) \times Vo/(L \times f \times V_{IN})$ $\Delta Vpp=\Delta IL \times ESR+(\Delta IL \times Vo)/(2 \times Co \times f \times V_{IN})$ Make setting of the rating of the capacitor with an adequate margin to the output voltage. Also, make setting of the maximum allowable ripple current with an adequate margin to ΔIL. Furthermore, the output rise time should be shorter than the sift start time. Select the output capacitor having a value smaller than that obtained by the formula shown below. $C_{Max}=\dfrac{3.5m \times (I_{Limit}-Io(Max))}{Vo}$ ILimit:2A(BD9778F/HFP), 2.5(BD9002HFP), 4A(BD9781HFP) If this capacitance is not optimum, faulty startup or else may result.	V_{IN}=13.2V, Vo=5V, L=100μH, f=100kHz $\Delta IL=(13.2-5) \times 5/(100 \times 10^{-6} \times 100 \times 10^{3} \times 13.2)$ $\fallingdotseq 0.31$ ΔIL=0.31A When I_{Limit}: 2 A, Io (Max) = 1 A, and Vo = 5V, $C_{Max}=3.5m \times (2-1)/5$ $=700\mu$ C_{Max}=700μF

Design procedure	Calculation example
4. Selection of diode Make setting of the rating of the diode with an adequate margin to the maximum load current. Also, make setting of the rated inverse voltage with an adequate margin to the maximum input voltage. Selecting a diode having a low forward voltage and short reverse recovery time will provide high efficiency.	When V_{IN} = 36 V and Io = (max.) 2 A, Select a diode of rated current of 2 A or more and rated withstand voltage of 36 V or more.
5. Selection of input capacitor Two capacitors, ceramic capacitor CIN and bypass capacitor C, should be inserted between the V_{IN} and GND. Be sure to insert a ceramic capacitor of 1 to 10 µF for the CIN. The capacitor C should have a low ESR and significantly large ripple current. The ripple current I_{RMS} can be obtained by the formula shown below. $I_{RMS}=Io \times \sqrt{VO \times (Vin-Vo)/ Vin^2}$ Select capacitors that can accept this ripple current. If the capacitance of CIN and C is not optimum, this IC may malfunction.	When V_{IN} = 13.2 V, Vo = 5 V, and Io = 1 A, $I_{RMS}=1 \times \sqrt{5 \times (13.2-5)/(13.2)^2}$ =0.235 I_{RMS}=0.235A
6. Setting of soft start time (BD9002HFP) The soft start time Tss can be set with the capacitor Css inserted between the SS and GND. $Tss=\frac{Vss(1V\ typ.) \times Css}{Iss(2.5\mu A\ Typ.)}$ If this capacitance is not optimum, overshoot may result. Make the capacitance setting in the range of 0.1 to 2.2 µF.	When Css = 0.1 µF, $Tss=\frac{1 \times 0.1 \times 10^{-6}}{2.5 \times 10^{-6}}$ =0.04 Tss=0.04s
7. Setting of oscillation frequency Referring Fig. 31 and Fig. 32 on the following page, select RT for the oscillation frequency to be used. Furthermore, in order to eliminate noises, be sure to connect ceramic capacitors of 0.1 to 1.0 µF in parallel.	
8. Setting of phase compensation (Rc and Cc) The phase margin can be set through inserting a capacitor or a capacitor and resistor between the INV pin and the FB pin. Each set value varies with the output coil, capacitance, I/O voltage, load, or else. Therefore, set the phase compensation to the optimum value according to these conditions. (For details, refer to Application circuit on page 11.) If this setting is not optimum, output oscillation or else may result.	

* The set values listed above are all reference values. On the actual mounting of the IC, the characteristics may vary with the routing of wirings and the types of parts in use. In this connection, it is recommended to thoroughly verify these values on the actual system prior to use.

● Directions for pattern layout of PCB

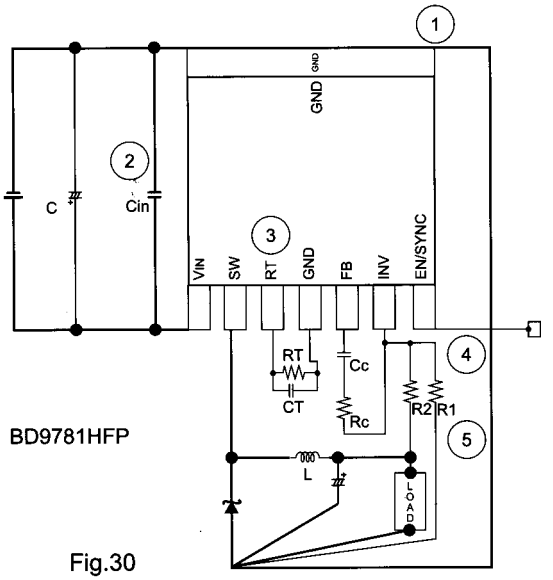


Fig.30

①Arrange the wirings shown by heavy lines as short as possible in a broad pattern.
②Locate the input ceramic capacitor Cin as close to the VIN-GND pin as possible.
③Locate the RT and CT as close to the GND pin as possible.
④Locate the R1 and R2 as close to the INV pin as possible, and provide the shortest wiring from the R1 and R2 to the INV pin.
⑤Locate the R1 and R2 as far away from the L as possible.

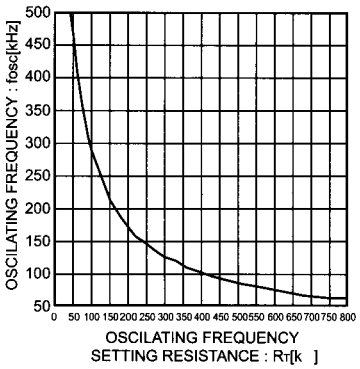


Fig.31 RT vs fOSC
(BD9781HFP/BD9778F/HFP)

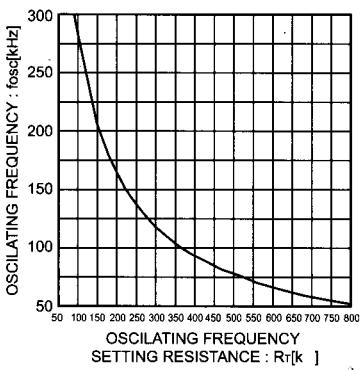


Fig.32 RT vs fOSC (BD9002HFP)

● Phase compensation setting procedure

1. About application stability conditions

The following section shows the stability conditions of negative feedback system.

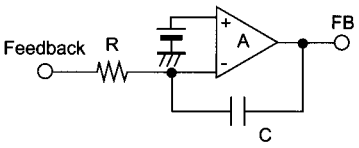
Furthermore, since the DC/DC converter application is sampled according to the switching frequency, GBW (frequency at 0-dB gain) of the overall system should be set to 1/10 or less of the switching frequency. The following section summarizes the targeted characteristics of this application.

- At a 1 (0-dB) gain, the phase delay is 150° or less (i.e., the phase margin is 30° or more).
- The GBW for this occasion is 1/10 or less of the switching frequency.

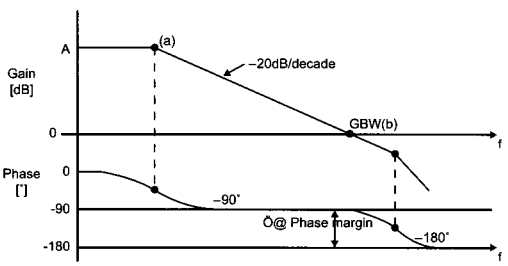
In other words, the responsiveness is determined with restrictions on the GBW. Consequently, in order to upgrade the responsiveness, higher switching frequency should be provided.

The knack for ensuring the stability through the phase compensation is to cancel a secondary phase delay (-180°) resulting from LC resonance with a secondary phase lead (i.e., through inserting two phase leads).
Furthermore, the GBW (i.e., frequency at 0-dB gain) is determined according to phase compensation capacitance to be provided for the error amplifier. Consequently, in order to reduce the GBW, increase the capacitor capacitance.

(1) Typical integrator (Low pass filter)



(2) Open loop characteristics of integrator



Point (a) $fa = \frac{1}{2\pi RCA}$ [Hz]

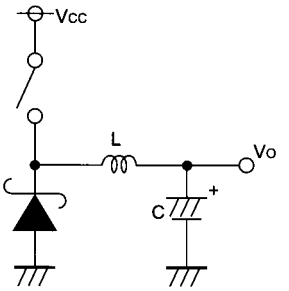
Point (b) $fb = GBW = \frac{1}{2\pi RC}$ [Hz]

Since the error amplifier is provided with (1) or (2) phase compensation, the low pass filter is applied. In the case of the DC/DC converter application, the R becomes a parallel resistance of the feedback resistance.

2. For output capacitors having high ESR, such as electrolyte capacitor

For output capacitors having high ESR (i.e., several Ω), the phase compensation setting procedure becomes comparatively simple. Since the DC/DC converter application has surely a LC resonant circuit attached to the output, a -180° phase-delay occurs in that area. If ESR component is present there, however, a +90° phase-lead occurs to shift the phase delay to -90°. Since the phase delay is desired to set within 150°, this is a very effective method but has a demerit to increase the ripple component of the output voltage.

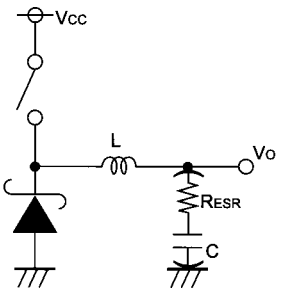
(1) LC resonant circuit



$$fr = \frac{1}{2\pi\sqrt{LC}} \text{ [Hz]}$$

At this resonance point, a -180° phase-delay occurs.

(2) With ESR provided



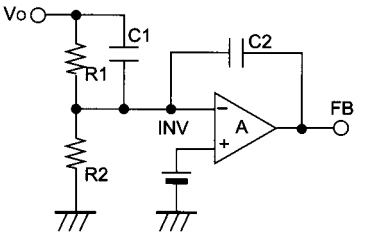
$$fr = \frac{1}{2\pi\sqrt{LC}} \text{ [Hz]: Resonance point}$$

$$f_{ESR} = \frac{1}{2\pi\ R_{ESR}C} \text{ [Hz]: Phase lead}$$

A -90° phase-delay occurs.

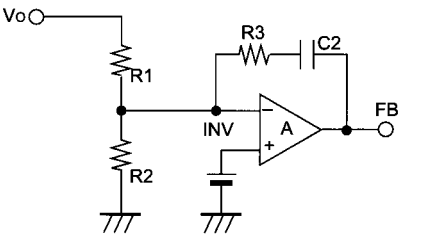
According to changes in phase characteristics due to the ESR, only one phase lead should be inserted. For this phase lead, select either of the methods shows below.

(3) Insert feedback resistance in the C.



$$\text{Phase lead: } fz = \frac{1}{2\pi\ C1R1} \text{ [Hz]}$$

(4) Insert the R3 in integrator.



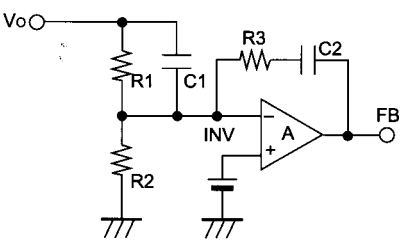
$$\text{Phase lead: } fz = \frac{1}{2\pi\ C2R3} \text{ [Hz]}$$

For the purpose of canceling the LC resonance, the frequency to insert the phase lead should be set close to the LC resonant frequency.
The settings above have simply obtained and no precise calculations or the like have not been made. Consequently, the settings may be adjusted on the actual system. Furthermore, since these characteristics vary with the layout of PCB, loading conditions and others, thorough confirmation should be made on the actual system for the design of mass production.

3. For output capacitors having low ESR, such as ceramic capacitor or OS-CON

Unlike section 2 above, in order to use capacitors having low ESR (i.e., several tens of mΩ), two phase-leads should be inserted so that a -180° phase-delay due to LC resonance will be compensated. The following section shows a typical phase compensation procedure.

(1) Phase compensation with secondary phase lead



$$\text{Phase lead: } f_{Z1} = \frac{1}{2\pi\ R1C1} \text{ [Hz]}$$

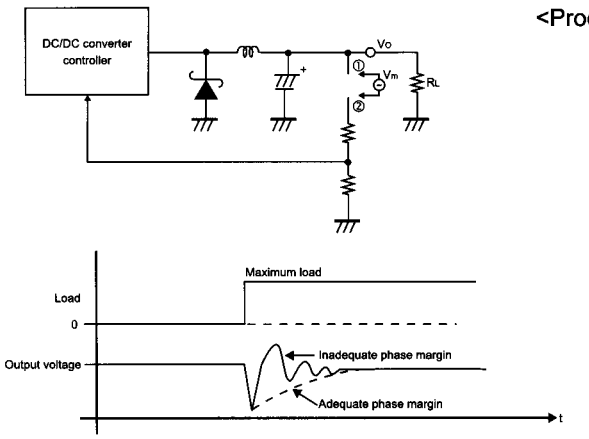
$$\text{Phase lead: } f_{Z2} = \frac{1}{2\pi\ R3C2} \text{ [Hz]}$$

$$\text{LC resonant frequency: } fr = \frac{1}{2\pi\sqrt{LC}} \text{ [Hz]}$$

For the settings of phase lead frequency, insert both of the phase leads close to the LC resonant frequency. According to empirical rule, setting the phase lead frequency f_{Z2} with R3 and C2 lower than the LC resonant frequency fr, and the phase lead frequency f_{Z1} with the R1 and C1 higher than the LC resonant frequency fr will provide stable application conditions.

<Reference> Measurement of open loop of DC/DC converter

In order to make measurement of the open loop of DC/DC converter, use the gain phase analyzer or FRA to measure the frequency characteristics.



<Procedure>

1. Check to be sure output causes no oscillation at the maximum load in closed loop.
2. Isolate (1) and (2) and insert Vm (with amplitude of approximately 100 mVpp).
3. Measure (probe) the oscillation of (1) to that of (2).

Furthermore, the phase margin can be also measured with the load responsiveness.
Measure variations in the output voltage when instantaneously changing the load from no load to the maximum load. Even though ringing phenomenon was caused, if, due to low phase margin, no ringing takes place, it can be said that phase margin is provided. However, no specific phase margin can be probed.

● About heat loss

For thermal design, be sure to operate the IC within the following conditions.
(Since the temperatures described hereunder are all guarantee temperatures, be sure to take the margin into account.)

1. The ambient temperature Ta is to be 125°C or less.
2. The chip junction temperature Tj is to be 150°C or less.

The chip junction temperature Tj can be considered in the following two patterns.

①To obtain Tj from the IC surface temperature Tc in the actual use state,
$Tj = Tc + \theta j\text{-}c \times W$

<Reference value> θj-c : HRP7 7°C/W
SOP8 32.5°C/W

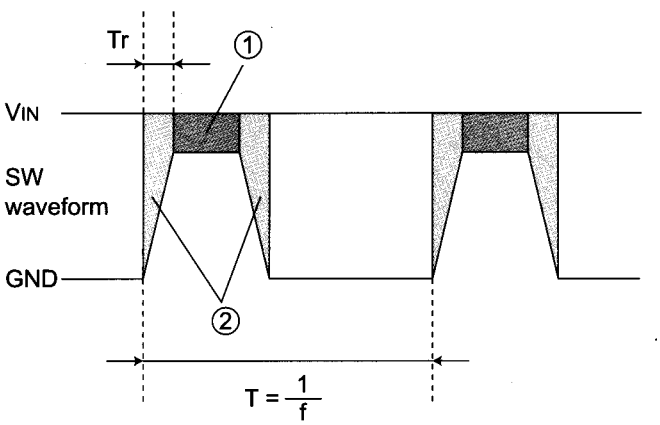
②To obtain Tj from the ambient temperature Ta
$Tj = Ta + \theta j\text{-}a \times W$

<Reference value> θj-a : HRP7 89.3°C/W Single piece of IC
54.3°C/W 2-layer PCB (Copper foil area on the front side of PCB: 15 × 15 mm²)
22.7°C/W 2-layer PCB (Copper foil area on the front side of PCB: 70 × 70 mm²)
PCB size: 70 × 70 × 1.6 mm³ (PCB incorporates thermal via.)
Copper foil area on the front side of PCB: 10.5 × 10.5 mm²
SOP8 222.2°C/W Single piece of IC
181.8°C/W 1-layer PCB
PCB size: 70 × 70 × 1.6 mm³

The heat loss W of the IC can be obtained by the formula shown below.

$$W = Ron \times Io^2 \times \frac{Vo}{VIN} + VIN \times Icc + Tr \times VIN \times Io \times f$$

Ron: ON resistance of IC (refer to pages 4 and 5.) Io: Load current
Vo: Output current VIN: Input current Icc: Circuit current (Refer to pages 2 and 3)
Tr: Switching rise/fall time (Approximately 40 nsec)
F: Oscillation frequency



① $Ron \times Io^2$

② $2 \times \frac{1}{2} \times Tr \times \frac{1}{T} \times VIN \times Io$

$= Tr \times VIN \times Io \times f$

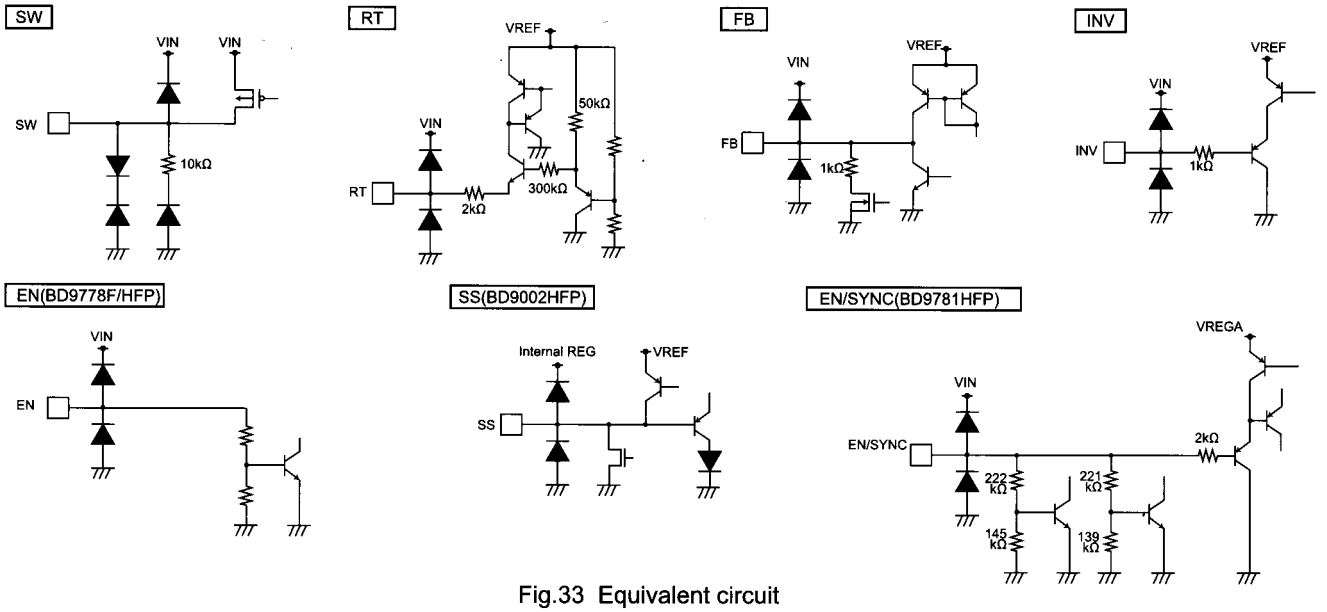


Fig.33 Equivalent circuit

● Cautions on use

1. Absolute maximum ratings
   Exceeding the absolute maximum ratings, such as applied voltage, operating temperature range, etc., can break down the IC. Should the IC break down, it will be impossible to identify breaking mode such as short circuit mode or an open mode. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including use of fuses, etc.
2. GND potential
   Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state.
3. Thermal design
   With consideration given to power dissipation (Pd) in the actual use state, provide the thermal design with an adequate margin.
4. Short circuit between pins and erroneous mounting
   In order to mount ICs on a set printed circuit board, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between pins or between the pin and the power supply or the GND pin, the ICs can break down.
5. Operation in strong electromagnetic field
   Please note that using ICs in the strong electromagnetic field can malfunction them.
6. Inspection with set printed circuit board
   On the inspection with the set printed circuit board, if a capacitor is connected to a low-impedance pin, the IC can suffer stress. Therefore, be sure to discharge from the set printed circuit board by each process. For protection against static electricity, establish a ground for the assembly process and pay thorough attention to the transportation and the storage of the set printed circuit board. Furthermore, in order to connect the jig for the inspection process, be sure to turn OFF the power supply and then mount the set printed circuit board to the jig. After the completion of the inspection, be sure to turn OFF the power supply and then dismount the set printed circuit board from the jig.
7. This IC is a monolithic IC, which has P+ isolation and P layer between elements to isolate the elements. P-N junction is formed with this P layer and the N layer of each element, thus composing a variety of parasitic elements.
   For example, as shown in Fig. 35, if the resistor and the transistor is connected with the pin respectively,
   - When GND>Pin A or GND>Pin B, P-N junction will operate as a parasitic diode.
   - When GND>Pin B, P-N junction will operate as a parasitic transistor.

   In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the IC. Therefore, pay thorough attention not to handle the input pins such as to apply to the input pins a voltage lower than the GND (P layer) so that any parasitic element will operate.

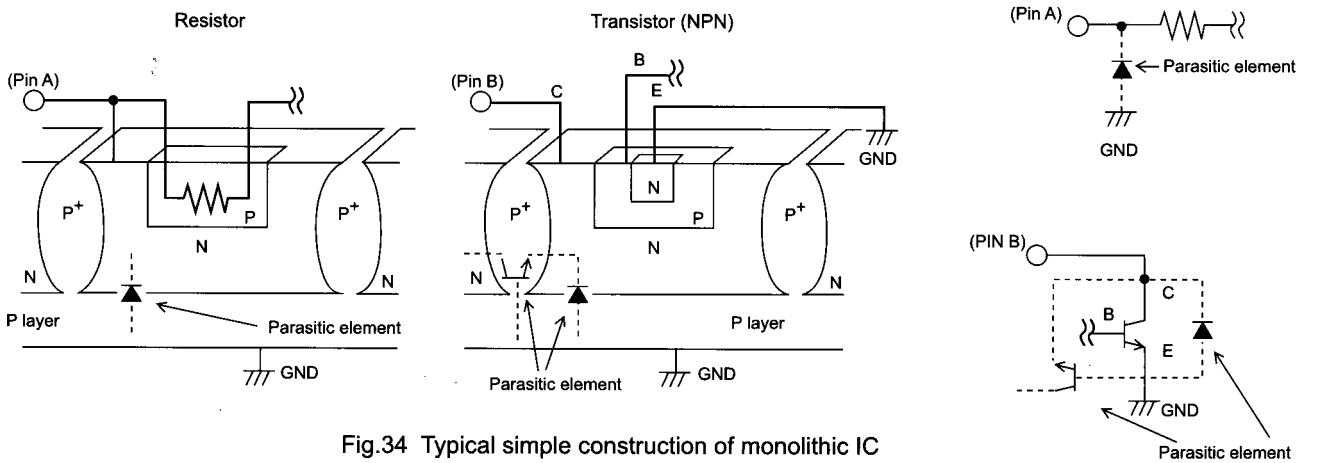


Fig.34 Typical simple construction of monolithic IC

8. Ground board pattern
If small-signal GND and large-current GND are provided, It will be recommended to separate the large-current GND pattern from the small-signal GND pattern and establish a single ground at the reference point of the set PCB so that resistance to the wiring pattern and voltage fluctuations due to a large current will cause no fluctuations in voltages of the small-signal GND. Pay attention not to cause fluctuations in the GND wiring pattern of external parts as well.

9. Temperature protection (thermal shut down) circuit
This IC has a built-in temperature protection circuit to prevent the thermal destruction of the IC. As described above, be sure to use this IC within the power dissipation range. Should a condition exceeding the power dissipation range continues, the chip temperature Tj will rise to activate the temperature protection circuit, thus turning OFF the output power element. Then, when the tip temperature Tj falls, the circuit will be automatically reset.
Furthermore, since the temperature protection circuit is activated under the condition exceeding the absolute maximum ratings, NEVER attempt to use the temperature protection circuit for set design or else.

10. On the application shown below, if there is a mode in which VIN and each pin potential are inverted, for example, if the VIN is short-circuited to the Ground with external diode charged, internal circuits may be damaged. To avoid that, it is recommended to insert a backflow prevention diode in series with the VIN or a bypass diode between each pin and VIN.

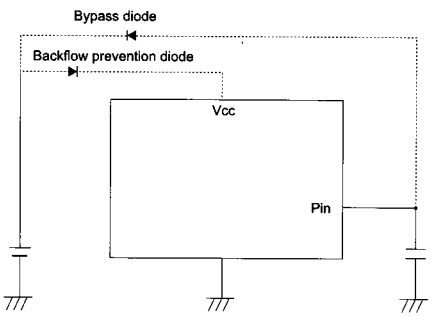
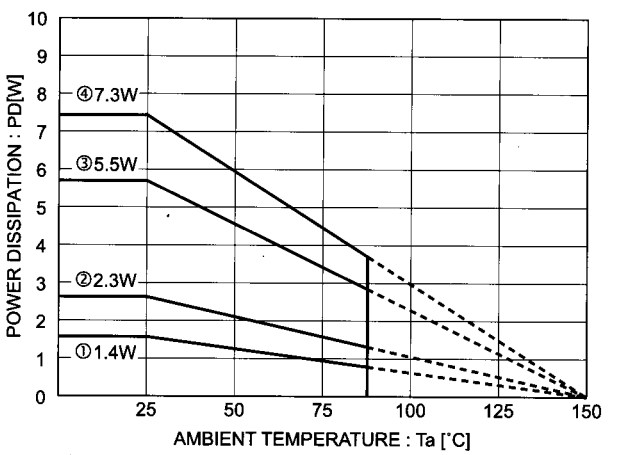


Fig.35

● Thermal derating characteristics

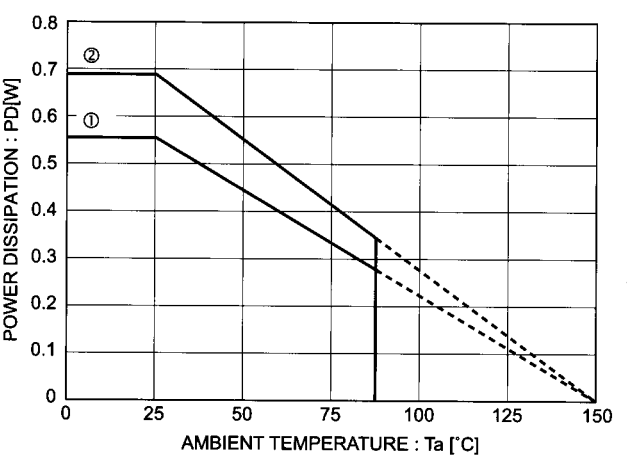
HRP7



① Single piece of IC
PCB size: 70 × 70 × 1.6 mm³ (PCB incorporates thermal via.)
Copper foil area on the front side of PCB: 10.5 × 10.5 mm²
② 2-layer PCB (Copper foil area on the reverse side of PCB: 15 × 15 mm²)
③ 2-layer PCB (Copper foil area on the reverse side of PCB: 70 × 70 mm²)
④ 4-layer PCB (Copper foil area on the reverse side of PCB: 70 × 70 mm²)

Fig.36

SOP8



① Single piece of IC
② When mounted on ROHM standard PCB
(Glass epoxy PCB of 70 mm × 70 mm × 1.6 mm)

Fig.37

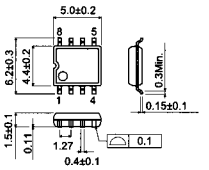
● Selection of order type

B	D	9	7	7	8	H	F	P	–	T	R

ROHM model name	Product No.	Package type	Taping type
	9778 = 36V/2A 9781 = 36V/4A 9002 = 50V/2.5A	F = SOP8 HFP = HRP7	E2 = Reel-type embossed carrier tape (SOP8) TR = Reel-type embossed carrier tape (HRP7)

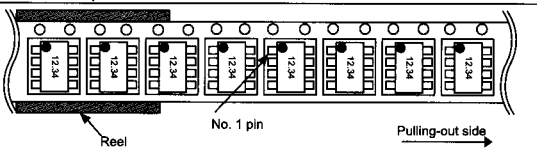
SOP8

<Outline dimensions>



<Package specifications>

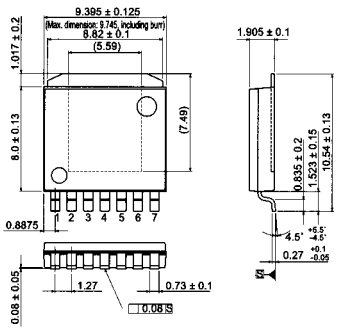
Package style	Embossed carrier tape
Q'ty per package	2500 pieces
Packaging direction	E2 (When holding a reel by left hand and pulling out the tape by right hand, No. 1 pin appears in the upper left of the reel.)



* Please place an order for this IC in multiplies of the quantity per package.

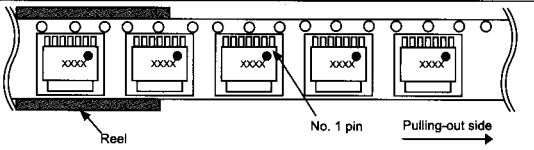
HRP7

<Outline dimensions>



<Package specifications>

Package style	Embossed carrier tape
Q'ty per package	2000 pieces
Packaging direction	TR (When holding a reel by left hand and pulling out the tape by right hand, No. 1 pin appears in the upper right of the reel.)



* Please place an order for this IC in multiplies of the quantity per package.

Excellence in Electronics

ROHM CO., LTD.
21, Saiin Mizosaki-cho, Ukyo-ku, Kyoto
615-8585, Japan
TEL: (075)311-2121 FAX: (075)315-0172
URL http: // www. rohm. com

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Atlanta U.S.A. / ROHM ELECTRONICS ATLANTA SALES OFFICE (DIVISION OF ROHM ELE. U.S.A.,LLC)
TEL: +1(770)754-5972 FAX: +1(770)754-0691
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TEL: +49(2154)9210 FAX: +49(2154)921400
United Kingdom / ROHM ELECTRONICS GMBH (UK)
TEL: +44(0)1908-306700 FAX: +44(0)1908-235788
France / ROHM ELECTRONICS GMBH (FRANCE)
TEL: +33(0)1 56 97 30 60 FAX: +33(0)1 56 97 30 80
Hong Kong China / ROHM ELECTRONICS (H.K.) CO., LTD.
TEL: +852(2)7406262 FAX: +852(2)375-8971
Shanghai China / ROHM ELECTRONICS (SHANGHAI) CO., LTD.
TEL: +86(21)6279-2727 FAX: +86(21)6247-2066
Dalian China / ROHM ELECTRONICS TRADING (DALIAN) CO., LTD.
TEL:+86(411)8230-8549 FAX:+86(411)8230-8537
Beijing China / BEIJING REPRESENTATIVE OFFICE
TEL: +86(10)8525-2483 FAX: +86(10)8525-2489
Taiwan / ROHM ELECTRONICS TAIWAN CO., LTD.
TEL: +886(2)2500-6956 FAX: +886(2)2503-2869
Korea / ROHM ELECTRONICS KOREA CORPORATION
TEL: +82(2)8182-700 FAX: +82(2)8182-715
Singapore / ROHM ELECTRONICS ASIA PTE. LTD. (RES / REI)
TEL: +65-6332-2322 FAX: +65-6332-5662
Malaysia / ROHM ELECTRONICS (MALAYSIA) SDN. BHD.
TEL: +60(3)7958-8355 FAX: +60(3)7958-8377
Philippines / ROHM ELECTRONICS (PHILIPPINES) SALES CORPORATION
TEL: +63(2)807-6872 FAX: +63(2)809-1422
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TEL: +66(2)254-4890 FAX: +66(2)256-6334

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