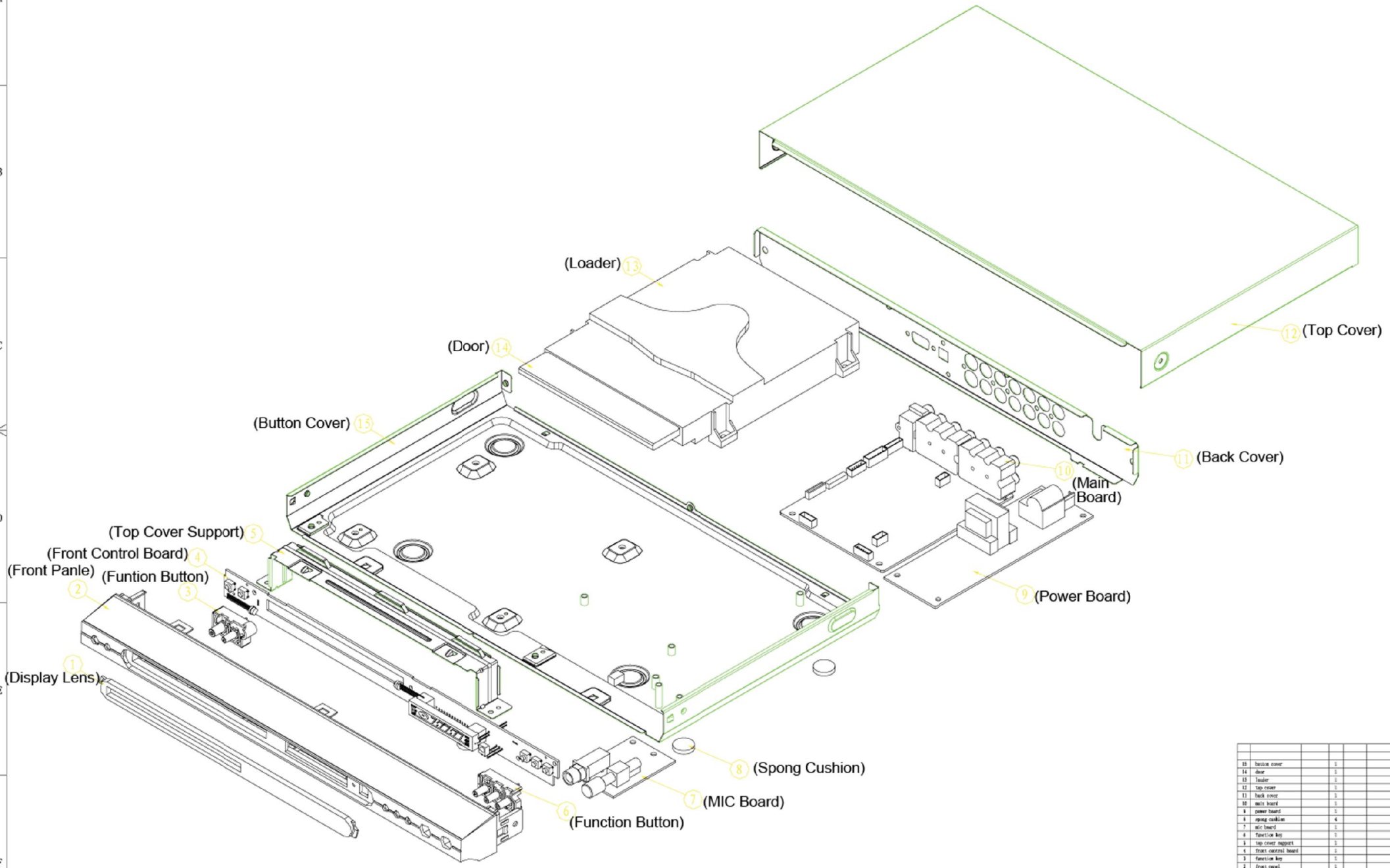
Elenberg DVDP-2417/DVDP-2420



NO.	PARTS NAME	PARTS NO.	Q'TY	MATERIAL	REMARK
15	button cover		1		
14	door		1		
13	loader		1		
12	top cover		1		
11	back cover		1		
10	main board		1		
9	power board		1		
8	spong cushion		4		
7	mic board		1		
6	function key		5		
5	top cover support		1		
4	front control board		1		
3	function key		5		
2	front panel		1		
1	display lens		1		

DIMENSION	TOLERANCE	MODEL	DVP-818	malata WANLIDA GROUP CO.,LTD.
		REV	0001	
		UNIT	mm	DSGN / 设计 DATE 2006.12.02
		SCALE	1:1	CHK DATE
ANGLE				APPR DATE

SERVICE MANUAL

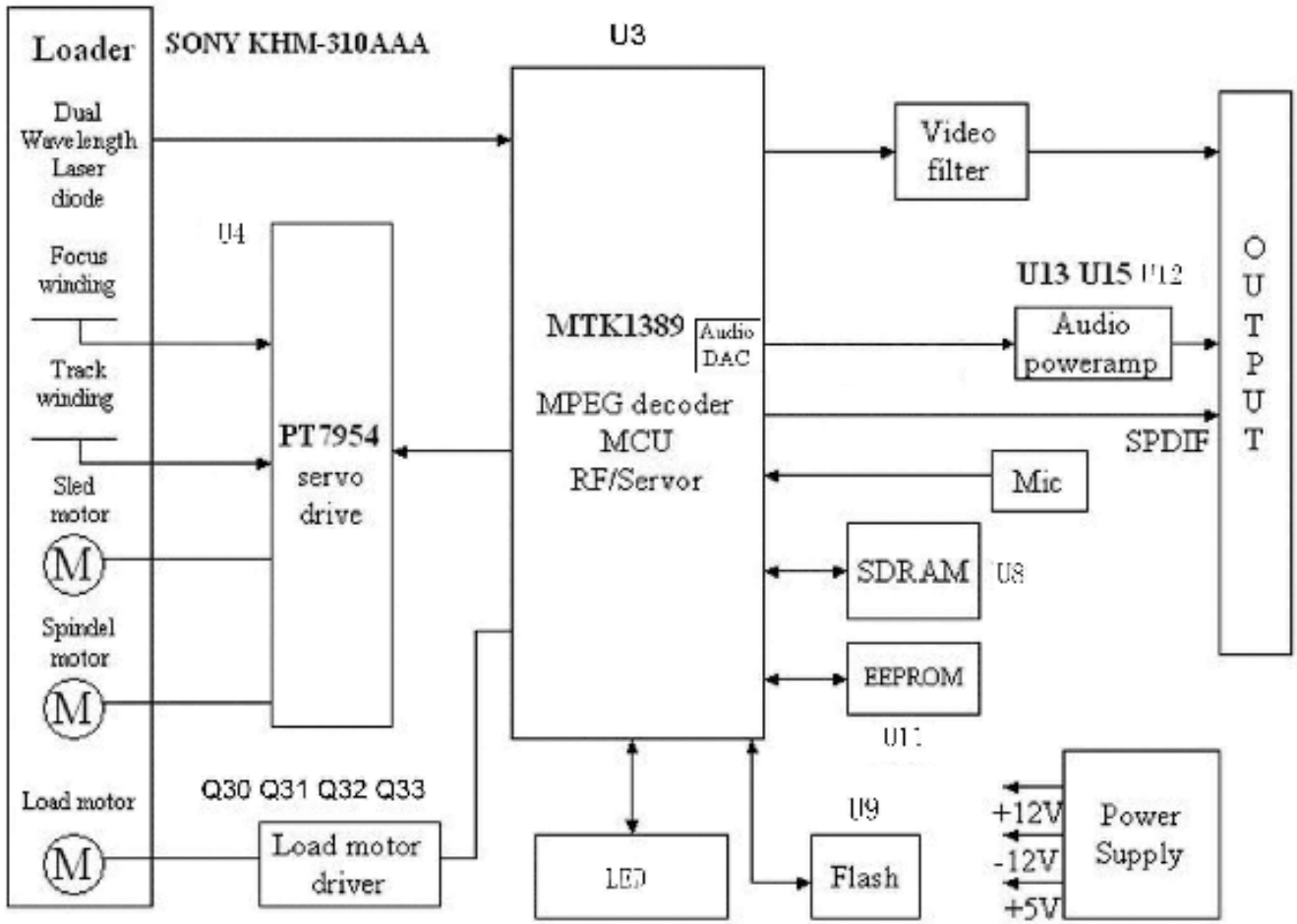
MODEL:DVDP-2420E/2417E

CONTENT

Part 1 Brief Introduction

Thank you for buying ELENBERG DVD Product. As a high-resolution DVD player, The DVD offers the high quality of DVD playback from a sleek, portable chassis. It plays almost all kinds of discs such as DVD-video, video CD, CD-R, CD-RW, MP3,WMA,PICTURE-CD JPEG, audio CD, and Super Video CD and MP4 discs compatible with the horizontal resolution more than 500 lines. It features an optical Dolby Digital output for ready connection with receivers equipped with Dolby decoders，The DAC audio converter and virtual surround sound capability deliver great sound whether you're listening through six speakers or two, while video features like A-B repeat and multiple-viewing-angle are displayed on the high-quality TV screen. The DVD SERIES comes with a wireless remote control, USER`S MANUAL.

Speciations		
Brand	E L E N B E R G	
DVD Type	DVDP-2417E/2420E	
General		
Exterior Color	Silver&black	
Number of Discs		
Playable Audio Formats	CD, CD-R, CD-RW, MP3	
Playable Video Formats	DVD, SVCD, JPEG,MP4	
Video Outputs	Composite,S-VEDIO,VGA,SCART	
Laser wavelength	780/650 nm	
Video system	AUTO/NTSC/PAL	
Frequency Response	20Hz-20KHz ± 2.5dB	
Audio signal-to noise rate	≥85 dB	
Audio distortion + noise	≤-70dB（1KHz）	
Dynamic range	≥80Db（1KHz）	
Channel separation	≥70Db（1KHz）	
Audio Out	Analog audio out	Out Level: 2V $\pm^{0.2}_{1.0}$, Load: 10kΩ
	Digital audio out:	Out Level: 0.5V_{P-P}, Load: 75Ω
Video Out	Out level: 1V_{P-P}±0.2 load:75Ω Unbalanced negative	
Power Supply	AC 100-240V 50/60 Hz	
Power Consumation	≤14W	
Dimension	370mm×245mm×44mm	
Weight	About 2kg	


Loader
SONY KHM-310AAA
U3
Dual Wavelength Laser diode
Focus winding
Track winding
Sled motor
Spindel motor
Load motor
U4
PT7954 servo drive
Q30 Q31 Q32 Q33
Load motor driver
MTK1389
Audio DAC
MPEG decoder
MCU
RF/Servor
LED
Video filter
U13 U15 U12
Audio poweramp
SPDIF
Mic
SDRAM
U8
EEPROM
U11
U9
Flash
+12V
-12V
+5V
Power Supply
OUTPUT

PART 2 KEY Ics And Assemblies

On Main Board			On power board		
Serial No	**Position**	**Type**	**Serial no**	**position**	**type**
1	U1	AMS1117	1	U804	2A0565/FSDH321
2	U2	CX1117-3.3	2	U802	PC817/EL817
3	U5		3	U803	KA431
4	U3	MTK1389DE/E			
5	U4	PT7954	On Panel board		
6	U7				
7	U6		**Serial no**	**position**	**position**
8	U8	K4S6416432H			
9	U9	MX 29LV160BT	1	U1	PT1628
10	U11	24C16			
11	U10				
12	U13 U15 U12	NJM4558			

ICS ON MAIN BOARD

REG1117:800mA and 1A Low Dropout Positive Regulator1.8V, 2.5V, 2.85V, 3.3V, 5V, and Adjustable

FEATURES

- FIXED AND ADJUSTABLE VERSIONS
- 2.85V MODEL FOR SCSI-2 ACTIVE TERMINATION
- OUTPUT CURRENT:
  REG1117: 800mA max
  REG1117A: 1A max
- OUTPUT TOLERANCE: ±1% max
- DROPOUT VOLTAGE:
  REG1117: 1.2V max at I_O = 800mA
  REG1117A: 1.3V max at I_O = 1A
- INTERNAL CURRENT LIMIT
- THERMAL OVERLOAD PROTECTION
- SOT-223 AND DDPAK SURFACE MOUNT PACKAGES

APPLICATIONS

- SCSI-2 ACTIVE TERMINATION
- HAND-HELD DATA COLLECTION DEVICES
- HIGH EFFICIENCY LINEAR REGULATORS
- BATTERY POWERED INSTRUMENTATION
- BATTERY MANAGEMENT CIRCUITS FOR NOTEBOOK AND PALMTOP PCs
- CORE VOLTAGE SUPPLY:
  FPGA, PLD, DSP, CPU

DESCRIPTION

The REG1117 is a family of easy-to-use three-terminal voltage regulators. The family includes a variety of fixed- and adjustable-voltage versions, two currents (800mA and 1A) and two package types (SOT-223 and DDPAK). See the chart below for available options.

Output voltage of the adjustable versions is set with two external resistors. The REG1117's low dropout voltage allows its use with as little as 1V input-output voltage differential.

Laser trimming assures excellent output voltage accuracy without adjustment. An NPN output stage allows output stage drive to contribute to the load current for maximum efficiency.

	800mA		1A	
VOLTAGE	SOT-223	DDPAK	SOT-223	DDPAK
1.8V			✔	✔
2.5V			✔	✔
2.85V	✔			
3.3V	✔	✔		
5V	✔			✔
Adj.	✔		✔	✔

SPECIFICATIONS

At T_J = +25°C, unless otherwise noted.

PARAMETER		CONDITIONS	REG1117, REG1117A MIN	TYP	MAX	UNITS
OUTPUT VOLTAGE						
REG1117-2.85		I_O = 10mA, V_{IN} = 4.85V	2.820	2.85	2.880	V
	Note 1	I_O = 0 to 800mA, V_{IN} = 4.05 to 10V	2.790	2.85	2.910	V
REG1117-3.3		I_O = 10mA, V_{IN} = 5.3V	3.270	3.30	3.330	V
	Note 1	I_O = 0 to 800mA, V_{IN} = 4.8 to 10V	3.240	3.30	3.360	V
REG1117-5		I_O = 10mA, V_{IN} = 7V	4.950	5.00	5.050	V
	Note 1	I_O = 0 to 800mA, V_{IN} = 6.5 to 10V	4.900	5.00	5.100	V
REG1117A-1.8		I_O = 10mA, V_{IN} = 3.8V	1.782	1.8	1.818	V
	Note 1	I_O = 0 to 1A, V_{IN} = 3.8V to 10V	1.764	1.8	1.836	V
REG1117A-2.5		I_O = 10mA, V_{IN} = 4.5V	2.475	2.5	2.525	V
	Note 1	I_O = 0 to 1A, V_{IN} = 4.5V to 10V	2.450	2.5	2.550	V
REG1117A-5		I_O = 10mA, V_{IN} = 7V	4.950	5.0	5.050	V
	Note 1	I_O = 0 to 1A, V_{IN} = 7V to 10V	4.900	5.0	5.100	V
REFERENCE VOLTAGE						
REG1117 (Adjustable)		I_O = 10mA, $V_{IN} - V_O$ = 2V	1.238	1.250	1.262	V
	Note 1	I_O = 10 to 800mA, $V_{IN} - V_O$ = 1.4 to 10V	1.225	1.250	1.280	V
REG1117A (Adjustable)		I_O = 10mA, $V_{IN} - V_O$ = 2V	1.238	1.250	1.262	V
	Note 1	I_O = 10mA to 1A, $V_{IN} - V_O$ = 1.4 to 10V	1.225	1.250	1.280	V
LINE REGULATION						
REG1117-2.85	Note 1	I_O = 0, V_{IN} = 4.25 to 10V		1	7	mV
REG1117-3.3	Note 1	I_O = 0, V_{IN} = 4.8 to 10V		2	7	mV
REG1117-5	Note 1	I_O = 0, V_{IN} = 6.5 to 15V		3	10	mV
REG1117 (Adjustable)	Note 1	I_O = 10mA, $V_{IN} - V_O$ = 1.5 to 13.75V		0.1	0.4	%
REG1117A (Adjustable)	Note 1	I_O = 10mA, $V_{IN} - V_O$ = 1.5 to 13.75V		0.1	0.4	%
REG1117A-1.8	Note 1	I_O = 0, V_{IN} = 3.8V to 10V		1	7	mV
REG1117A-2.5	Note 1	I_O = 0, V_{IN} = 4.5V to 10V		1	7	mV
REG1117A-5.0	Note 1	I_O = 0, V_{IN} = 7V to 15V		3	10	mV
LOAD REGULATION						
REG1117-2.85	Note 1	I_O = 0 to 800mA, V_{IN} = 4.25V		2	10	mV
REG1117-3.3	Note 1	I_O = 0 to 800mA, V_{IN} = 4.8V		3	12	mV
REG1117-5	Note 1	I_O = 0 to 800mA, V_{IN} = 6.5V		3	15	mV
REG1117 (Adjustable)	Note 1, 2	I_O = 10 to 800mA, $V_{IN} - V_O$ = 3V		0.1	0.4	%
REG1117A (Adjustable)	Note 1, 2	I_O = 10mA to 1A, $V_{IN} - V_O$ = 3V		0.1	0.4	%
REG1117A-1.8		I_O = 0 to 1A, V_{IN} = 3.8V		2	10	mV
REG1117A-2.5		I_O = 0 to 1A, V_{IN} = 4.5V		2	10	mV
REG1117A-5		I_O = 0 to 1A, V_{IN} = 7.0V		3	15	mV
DROPOUT VOLTAGE	Note 3					
All Models	Note 1	I_O = 100mA		1.00	1.10	V
	Note 1	I_O = 500mA		1.05	1.15	V
REG1117 Models	Note 1	I_O = 800mA		1.10	1.20	V
REG1117A		I_O = 1A		1.2	1.30	V
	Note 1	I_O = 1A		1.2	1.55	V
CURRENT LIMIT						
REG1117 Models		$V_{IN} - V_O$ = 5V	800	950	1200	mA
REG1117A		$V_{IN} - V_O$ = 5V	1000	1250	1600	mA
MINIMUM LOAD CURRENT						
Adjustable Models	Note 1, 2	$V_{IN} - V_O$ = 13.75V		1.7	5	mA
QUIESCENT CURRENT						
Fixed-Voltage Models	Note 1	$V_{IN} - V_O$ = 5V		4	10	mA
Adjust Pin Current	Note 1, 2	I_O = 10mA, $V_{IN} - V_O$ = 1.4 to 10V		50	120	µA
vs Load Current, REG1117	Note 1	I_O = 10mA to 800mA, $V_{IN} - V_O$ = 1.4 to 10V		0.5	5	µA
vs Load Current, REG1117A	Note 1	I_O = 10mA to 1A, $V_{IN} - V_O$ = 1.4 to 10V		0.5	5	µA
THERMAL REGULATION						
All Models	Note 4	30ms Pulse		0.01	0.1	%/W
RIPPLE REJECTION						
All Models		f = 120Hz, $V_{IN} - V_{OUT}$ = 3V+1V_{PP} Ripple		62		dB
TEMPERATURE DRIFT						
Fixed-Voltage Models		T_J = 0°C to +125°C		0.5		%
Adjustable Models		T_J = 0°C to +125°C		2		%

SPECIFICATIONS (cont.)

At T_J = +25°C, unless otherwise noted.

PARAMETER	CONDITIONS	REG1117, REG1117A			UNITS
		MIN	TYP	MAX	
LONG-TERM STABILITY					
All Models	T_A = +125°C, 1000Hr		0.3		%
OUTPUT NOISE					
rms Noise, All Models	f = 10Hz to 10kHz		0.003		%
THERMAL RESISTANCE					
Operating Junction Temperature Range		0		+125	°C
Storage Range		–65		+150	°C
Thermal Resistance, θ_{JC}	(Junction-to-Case at Tab)				
3-Lead SOT-223 Surface-Mount			15		°C/W
3-Lead DDPAK Surface-Mount	f > 50Hz		2		°C/W
	dc		3		°C/W
Thermal Resistance, θ_{JA}	(Junction-to-Case at Tab)				
3-Lead DDPAK Surface-Mount	No Heat Sink		65		°C/W

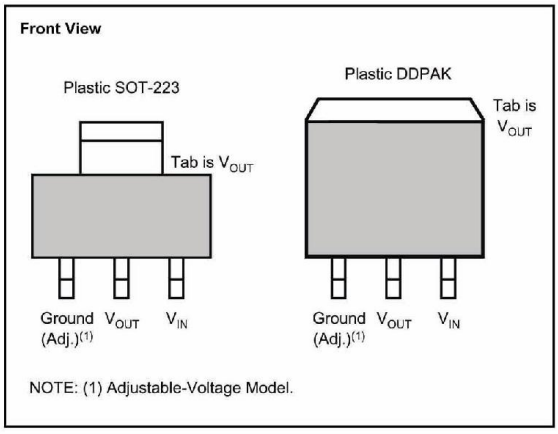
NOTES: (1) Specification applies over the full operating Junction temperature range, 0°C to 125°C. (2) REG1117 and REG1117A adjustable versions require a minimum load current for ±3% regulation. (3) Dropout voltage is the Input voltage minus output voltage that produces a 1% decrease in output voltage. (4) Percentage change in unloaded output voltage before vs after a 30ms power pulse of I_O = 800mA (REG1117 models), I_O = 1A (REG1117A), $V_{IN} - V_O$ = 1.4V (Reading taken 10ms after pulse).

ABSOLUTE MAXIMUM RATINGS(1)

Power Dissipation	Internally Limited
Input Voltage	15V
Operating Junction Temperature Range	0°C to +125°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature (soldering, 10s)(2)	+300°C

NOTE: (1) Stresses above these ratings may cause permanent damage. (2) See "Soldering Methods."

CONNECTION DIAGRAM



NOTE: (1) Adjustable-Voltage Model.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

MT1389: is a DVD player system-on-chip (SOC) which incorporates advanced features like MPEG-4 video decoder, high definition TV encoder, and state-of-art de-interlace processing. The MT1389 enables consumer electronics manufacturers to build high quality, cost-effective DVD players, portable DVD players or any other home entertainment audio/video devices. Based on Media Tek's world-leading DVD player SOC architecture, the MT1389 is the 3rd generation of the DVD player SOC. It integrates the MediaTek 2nd generation front-end analog RF amplifier and the Servo/MPEG AV decoder. To enrich the feature of DVD player, the MT1389 equips a MPEG-4 video decoder supporting the MPEG-4/DivX2 advanced simple profile (ASP). It makes the MT1389-based DVD player be capable of playback MPEG-4 contents which become more and more popular now. The progressive scan of the MT1389 utilized a proprietary advanced motion-adaptive algorithm to achieve best movie/video playback. It can easily detect 3:2/2:2 pull down source and restore the correct original pictures. It also supports a patent-pending edge-preserving algorithm to remove the saw-tooth effect.

5-5 Pin Definitions

Abbreviations:

- SR: Slew Rate
- PU: Pull Up
- PD: Pull Down
- SMT: Schmitt Trigger
- 4mA~16mA: Output buffer driving strength.

Pin	Main	Alt.	Type	Description
RF Interface (26)				
191	RFGND18		Ground	Analog ground
192	RFVDD18		Power	Analog power 1.8V
212	OSP		Analog output	RF Offset cancellation capacitor connecting
213	OSN		Analog output	RF Offset cancellation capacitor connecting
214	RFGC		Analog output	RF AGC loop capacitor connecting for DVD-ROM
215	IREF		Analog Input	Current reference input. It generates reference current for RF path. Connect an external 15K resistor to this pin and AVSS
216	AVDD3		Power	Analog power 3.3V
1	AGND		Ground	Analog ground
2	DVDA		Analog Input	AC coupled input path A
3	DVDB		Analog Input	AC coupled input path B
4	DVDC		Analog Input	AC coupled input path C
5	DVDD		Analog Input	AC coupled input path D
6	DVDRFIP		Analog Input	AC coupled DVD RF signal input RFIP
7	DVDRFIN		Analog Input	AC coupled DVD RF signal input RFIN
8	MA		Analog Input	DC coupled main-beam RF signal input A
9	MB		Analog Input	DC coupled main-beam RF signal input B
10	MC		Analog Input	DC coupled main-beam RF signal input C
11	MD		Analog Input	DC coupled main-beam RF signal input D
12	SA		Analog Input	DC coupled sub-beam RF signal input A
13	SB		Analog Input	DC coupled sub-beam RF signal input B

Pin	Main	Alt.	Type	Description
14	SC		Analog Input	DC coupled sub-beam RF signal input C
15	SD		Analog Input	DC coupled sub-beam RF signal input D
16	CDFON		Analog Input	CD focusing error negative input
17	CDFOP		Analog Input	CD focusing error positive input
18	TNI		Analog Input	3 beam satellite PD signal negative input
19	TPI		Analog Input	3 beam satellite PD signal positive input
ALPC (4)				
20	MDI1		Analog Input	Laser power monitor input
21	MDI2		Analog Input	Laser power monitor input
22	LDO2		Analog Output	Laser driver output
23	LDO1		Analog Output	Laser driver output
Reference Voltage (3)				
28	V2REFO		Analog output	Reference voltage 2.8V
29	V20		Analog output	Reference voltage 2.0V
30	VREFO		Analog output	Reference voltage 1.4V
Analog Monitor Output (7)				
24	SVDD3		Power	Analog power 3.3V
25	CSO	RFOP	Analog output	1) Central servo 2) Positive main beam summing output
26	RFLVL	RFON	Analog output	1) RFRP low pass, or 2) Negative main beam summing output
27	SGND		Ground	Analog ground
31	FEO		Analog output	Focus error monitor output
32	TEO		Analog output	Tracking error monitor output
33	TEZISLV		Analog output	TE slicing Level
Analog Servo Interface (8)				
204	ADCVDD3		Power	Analog 3.3V power for ADC
205	ADCVSS		Ground	Analog ground for ADC

Pin	Main	Alt.	Type	Description
206	RFVDD3		Power	Analog power
207	RFRPDC		Analog output	RF ripple detect output
208	RFRPAC		Analog Input	RF ripple detect input (through AC-coupling)
209	HRFZC		Analog Input	High frequency RF ripple zero crossing
210	CRTPLP		Analog output	Defect level filter capacitor connecting
211	RFGND		Ground	Analog Power
RF Data PLL Interface (9)				
195	JITFO		Analog output	Output terminal of RF jitter meter
196	JITFN		Analog Input	Input terminal of RF jitter meter
197	PLLVSS		Ground	Ground pin for data PLL and related analog circuitry
198	IDACEXLP		Analog output	Data PLL DAC Low-pass filter
199	PLLVDD3		Power	Power pin for data PLL and related analog circuitry
200	LPFON		Analog Output	Negative output of loop filter amplifier
201	LPFIP		Analog Input	Positive input terminal of loop filter amplifier
202	LPFIN		Analog Input	Negative input terminal of loop filter amplifier
203	LPFOP		Analog Output	Positive output of loop filter amplifier
Motor and Actuator Driver Interface (10)				
34	OP_OUT		Analog output	Op amp output
35	OP_INN		Analog input	Op amp negative input
36	OP_INP		Analog input	Op amp positive input
37	DMO		Analog Output	Disk motor control output. PWM output
38	FMO		Analog Output	Feed motor control. PWM output
39	TROPENPWM		Analog Output	Tray PWM output/Tray open output
40	PWMOUT1	ADIN0	Analog Output	3) 1st General PWM output 4) AD input 0
41	TRO		Analog Output	Tracking servo output. PDM output of tracking servo compensator

Pin	Main	Alt.	Type	Description
42	FOO		Analog Output	Focus servo output. PDM output of focus servo compensator
43	FG (Digital pin)	ADIN1 GPIO	LVTTL 3.3V Input, Schmitt Input, pull up, with analog input path for ADIN1	1) Motor Hall sensor input 2) AD input 1 3) GPIO
General Power/Ground (11)				
48,84, 132, 146	DVDD18		Power	1.8V power pin for internal digital circuitry
74, 120	DVSS		Ground	1.8V Ground pin for internal digital circuitry
60,87, 108,137	DVDD3		Power	3.3V power pin for internal digital circuitry
149	DVSS		Ground	3.3V Ground pin for internal digital circuitry
Micro Controller and Flash Interface (48)				
54	HIGHA0		InOut 4~16mA, SR PU	Microcontroller address 8
66	HIGHA1		InOut 4~16mA, SR PU	Microcontroller address 9
65	HIGHA2		InOut 4~16mA, SR PU	Microcontroller address 10
64	HIGHA3		InOut 4~16mA, SR PU	Microcontroller address 11
63	HIGHA4		InOut 4~16mA, SR PU	Microcontroller address 12

Pin	Main	Alt.	Type	Description
62	HIGHA5		InOut 4~16mA, SR PU	Microcontroller address 13
61	HIGHA6		InOut 4~16mA, SR PU	Microcontroller address 14
59	HIGHA7		InOut 4~16mA, SR PU	Microcontroller address 15
81	AD7		InOut 4~16mA, SR	Microcontroller address/data 7
78	AD6		InOut 4~16mA, SR	Microcontroller address/data 6
77	AD5		InOut 4~16mA, SR	Microcontroller address/data 5
76	AD4		InOut 4~16mA, SR	Microcontroller address/data 4
75	AD3		InOut 4~16mA, SR	Microcontroller address/data 3
73	AD2		InOut 4~16mA, SR	Microcontroller address/data 2
72	AD1		InOut 4~16mA, SR	Microcontroller address/data 1
71	AD0		InOut 4~16mA, SR	Microcontroller address/data 0
83	IOA0		InOut 4~16mA, SR PU	Microcontroller address 0 / IO
69	IOA1		InOut 4~16mA, SR PU	Microcontroller address 1 / IO

Pin	Main	Alt.	Type	Description
47	IOA2		InOut 4~16mA, SR PU	Microcontroller address 2 / IO
49	IOA3		InOut 4~16mA, SR PU	Microcontroller address 3 / IO
50	IOA4		InOut 4~16mA, SR PU	Microcontroller address 4 / IO
51	IOA5		InOut 4~16mA, SR PU	Microcontroller address 5 / IO
52	IOA6		InOut 4~16mA, SR PU	Microcontroller address 6 / IO
53	IOA7		InOut 4~16mA, SR PU	Microcontroller address 7 / IO
58	A16		Output 4~16mA, SR PU	Flash address 16
82	A17		Output 4~16mA, SR PU	Flash address 17
55	IOA18		InOut 4~16mA, SR PD, SMT	Flash address 18 / IO
56	IOA19		InOut 4~16mA, SR PD, SMT	Flash address 19 / IO

Pin	Main	Alt.	Type	Description
67	IOA20	YUV0	InOut 4~16mA, SR PD, SMT	5) Flash address 20 / IO 6) While External Flash size <= 1MB: I)Alternate digital video YUV output 0
79	IOA21	YUV7 GPIO	InOut 4~16mA, SR PD, SMT	7) Flash address 21 / IO 8) While External Flash size <= 2MB: I)Digital video YUV output 7 II) GPIO
80	ALE		InOut 4~16mA, SR PU, SMT	Microcontroller address latch enable
70	IOOE#		InOut 4~16mA, SR SMT	Flash output enable, active low / IO
57	IOWR#		InOut 4~16mA, SR PU, SMT	Flash write enable, active low / IO
68	IOCS#		InOut 4~16mA, SR SMT	Flash chip select, active low / IO
85	UWR#		InOut 4~16mA, SR PU, SMT	Microcontroller write strobe, active low
86	URD#		InOut 4~16mA, SR PU, SMT	Microcontroller read strobe, active low
88	UP1_2		InOut 4mA, SR PU, SMT	Microcontroller port 1-2
89	UP1_3		InOut 4mA, SR PU, SMT	Microcontroller port 1-3

Pin	Main	Alt.	Type	Description
91	UP1_4		InOut 4mA, SR PU, SMT	Microcontroller port 1-4
92	UP1_5		InOut 4mA, SR PU, SMT	Microcontroller port 1-5
93	UP1_6	SCL	InOut 4mA, SR PU, SMT	9) Microcontroller port 1-6 10) I^2C clock pin
94	UP1_7	SDA	InOut 4mA, SR PU, SMT	11) Microcontroller port 1-7 12) I^2C data pin
95	UP3_0	RXD	InOut 4mA, SR PU, SMT	13) Microcontroller port 3-0 14) 8032 RS232 RxD
96	UP3_1	TXD	InOut 4mA, SR PU, SMT	15) Microcontroller port 3-1 16) 8032 RS232 TxD
97	UP3_4	RXD SCL	InOut 4mA, SR PU, SMT	17) Microcontroller port 3-4 18) Hardwired RD232 RxD 19) I^2C clock pin
98	UP3_5	TXD SDA	InOut 4mA, SR PU, SMT	20) Microcontroller port 3-5 21) Hardwired RD232 TxD 22) I^2C data pin
102	IR		Input SMT	IR control signal input
103	INT0#		InOut 4~16mA, SR PU, SMT	Microcontroller external interrupt 0, active low
Audio interface (28)				

Pin	Main	Alt.	Type	Description
153	ALRCK	YUV1 GPO	InOut 4mA, PD, SMT	1) Audio left/right channel clock 2) Trap value in power-on reset: I)1: use external 373 II) 0: use internal 373 3) While internal audio DAC used: I)Digital video YUV output 1 II) GPO
151	ABCK	YUV0 GPIO	InOut 4mA	4) Audio bit clock 5) While internal audio DAC used: I)Digital video YUV output 0 II) GPIO
154	ASDATA0	YUV2 GPO	InOut 4mA PD SMT	8) Audio serial data 0 (Front-Left/Front-Right) 9) Trap value in power-on reset: I)1: manufactory test mode II) 0: normal operation 10) While internal audio DAC used: I)Digital video YUV output 2 II) GPO
155	ASDATA1	YUV4 GPO	InOut 4mA PD SMT	11) Audio serial data 1 (Left-Surround/Right-Surround) 12) Trap value in power-on reset: I)1: manufactory test mode II) 0: normal operation 13) While only 2 channels output: I)Digital video YUV output 4 II) GPO
156	ASDATA2	YUV5 GPO	InOut 4mA PD SMT	14) Audio serial data 2 (Center/LFE) 15) Trap value in power-on reset: I)1: manufactory test mode II) 0: normal operation 16) While only 2 channels output: I)Digital video YUV output 5 II) GPO
157	ASDATA3	YUV6 GPIO	InOut 4mA PD SMT	17) Audio serial data 3 (Center-back/ Center-left-back/Center-right-back, in 6.1 or 7.1 mode) 18) While only 2 channels output: I)Digital video YUV output 6 II) GPIO
158	MC_DATA	INT2# YUV0 GPIO	InOut 2mA	19) Microphone serial input 20) While not support Microphone: I)Microcontroller external interrupt 2 II) Digital video YUV output 0 III) GPIO

Pin	Main	Alt.	Type	Description
159	SPDIF		Output 4~16mA, SR: ON/OFF	S/PDIF output
172	AADVSS		Ground	Ground pin for 2ch audio ADC circuitry
173	AKIN2		Analog	Audio ADC input 2
174	ADVCM		Analog	2ch audio ADC reference voltage
175	AKIN1		Analog	Audio ADC input 1
176	AADVDD		Power	3.3V power pin for 2ch audio ADC circuitry
177	APLLVDD3		Power	3.3V Power pin for audio clock circuitry
178	APLLCAP		Analog InOut	APLL external capacitance connection
179	APLLVSS		Ground	Ground pin for audio clock circuitry
180	ADACVSS2		Ground	Ground pin for audio DAC circuitry
181	ADACVSS1		Ground	Ground pin for audio DAC circuitry
182	ARF	GPIO	Output	21) Audio DAC sub-woofer channel output 22) While internal audio DAC not used: GPIO
183	ARS	GPIO	Output	23) Audio DAC right Surround channel output 24) While internal audio DAC not used: GPIO
184	AR	GPIO	Output	25) Audio DAC right channel output 26) While internal audio DAC not used: a. SDATA1 b. GPIO
185	AVCM		Analog	Audio DAC reference voltage
186	AL	GPIO	Output	27) Audio DAC left channel output 28) While internal audio DAC not used: a. SDATA2 b. GPIO
187	ALS	GPIO	Output	29) Audio DAC left Surround channel output 30) While internal audio DAC not used: c. SDATA0 d. GPIO
188	ALF	GPIO	Output	31) Audio DAC center channel output 32) While internal audio DAC not used: GPIO
189	ADACVDD1		Power	3.3V power pin for audio DAC circuitry
190	ADACVDD2		Power	3.3V power pin for audio DAC circuitry
Video Interface (12)				
160	DACVDDC		Power	3.3V power pin for video DAC circuitry

Pin	Main	Alt.	Type	Description
161	VREF		Analog	Bandgap reference voltage
162	FS		Analog	Full scale adjustment
163	DACVSSC		Ground	Ground pin for video DAC circuitry
164	CVBS		Output 4mA, SR	Analog composite output
165	DACVDDB		Power	3.3V power pin for video DAC circuitry
166	DACVSSB		Ground	Ground pin for video DAC circuitry
167	DACVDDA		Power	3.3V power pin for video DAC circuitry
168	Y/G		Output 4mA, SR	Green, Y, SY, or CVBS
169	DACVSSA		Ground	Ground pin for video DAC circuitry
170	B/CB/PB		Output 4mA, SR	Blue, CB/PB, or SC
171	R/CR/PR		Output 4mA, SR	Red, CR/PR, CVBS, or SY
MISC (12)				
101	PRST#		Input PU, SMT	Power on reset input, active low
193	XTALO		Output	27MHz crystal output
194	XTALI		Input	27MHz crystal input
44	GPIO0	VSYN YUV1	InOut 4mA, SR SMT	33) General purpose IO 0 34) Vertical sync for video input 35) Digital video YUV output 1
45	GPIO1	HSYN INT4# YUV2	InOut 4mA, SR SMT	36) General purpose IO 1 37) Horizontal sync for video input 38) Microcontroller external interrupt 4 39) Digital video YUV output 2

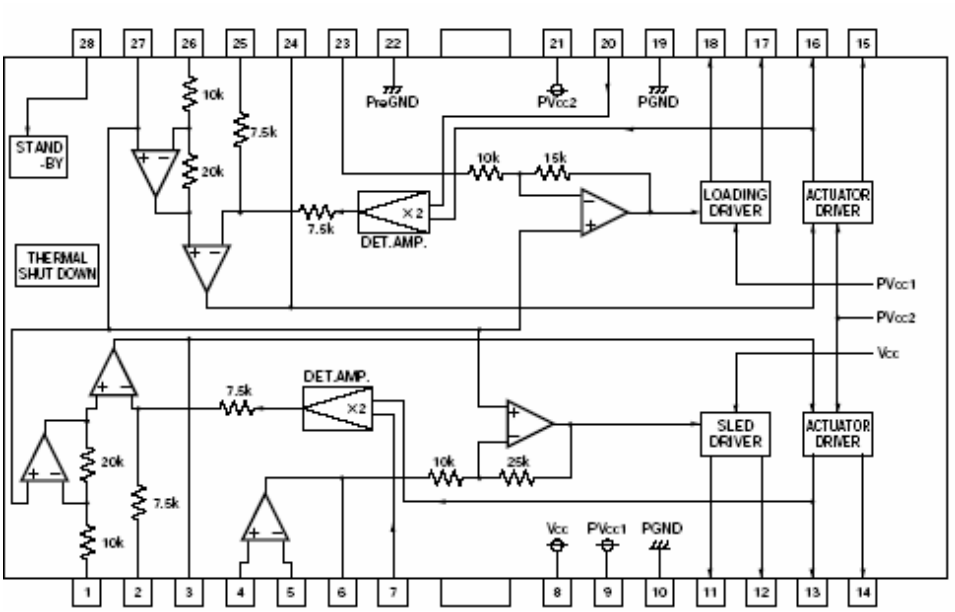
Pin	Main	Alt.	Type	Description
46	GPIO2	SPMCLK	InOut 2mA	40) General purpose IO 2 41) Audio S/PDIF SPMCLK input
147	GPIO3	INT1# SPDATA	InOut 2mA	42) General purpose IO 3 43) Microcontroller external interrupt 1 44) Audio S/PDIF SPDATA input
148	GPIO4	SPLRCK	InOut 2mA	45) General purpose IO 4 46) Audio S/PDIF SPLRCK input
150	GPIO5	INT3# SPBCK	InOut 2mA	47) General purpose IO 5 48) Microcontroller external interrupt 3 49) Audio S/PDIF SPBCK input
90	GPIO6	YUVCLK	InOut 4mA, SR PD, SMT	50) General purpose IO 6 51) Digital video clock output
99	GPIO7	YUV3	InOut 4mA, PD, SMT	52) General purpose IO 7 53) Digital video YUV output 3
Dram Interface (38) (Sorted by position)				
145	RA4		InOut	DRAM address 4
144	RA5		InOut	DRAM address 5
142	RA7		InOut	DRAM address 7
141	RA8		InOut	DRAM address 8
140	RA9		InOut	DRAM address 9
139	RA11		InOut Pull-Down	DRAM address bit 11
138	CKE		Output	DRAM clock enable
136	RCLK		InOut	Dram clock
135	RA3		InOut	DRAM address 3
134	RA2		InOut	DRAM address 2
133	RA1		InOut	DRAM address 1
131	RA0		InOut	DRAM address 0

Pin	Main	Alt.	Type	Description
130	RA10		InOut	DRAM address 10
129	BA1		InOut	DRAM bank address 1
128	BA0		InOut	DRAM bank address 0
127	RCS#		Output	DRAM chip select, active low
126	RAS#		Output	DRAM row address strobe, active low
125	CAS#		Output	DRAM column address strobe, active low
124	RWE#		Output	DRAM Write enable, active low
123	DQM1		InOut	Data mask 1
122	RD8		InOut	DRAM data 8
121	RD9		InOut	DRAM data 9
119	RD10		InOut	DRAM data 10
118	RD11		InOut	DRAM data 11
117	RD12		InOut	DRAM data 12
116	RD13		InOut	DRAM data 13
115	RD14		InOut	DRAM data 14
114	RD15		InOut	DRAM data 15
113	RD0		InOut	DRAM data 0
112	RD1		InOut	DRAM data 1
111	RD2		InOut	DRAM data 2
110	RD3		InOut	DRAM data 3
109	RD4		InOut	DRAM data 4
107	RD5		InOut	DRAM data 5
106	RD6		InOut	DRAM data 6
105	RD7		InOut	DRAM data 7
104	DQM0		InOut	Data mask 0

Note:

1. The Main column is the main function, Alt. means alternative function.
2. The multi-function GPIO pins are set to green characters.
3. The multi-function GPO pins are ser to blue characters.
4. The external TV encoder mode only supports CCIR-656 mode.

PT7954:



Pin No	symbol	Description	Pin NO	Symbol	Description
1	VINFC	FOCUS DRIVE INPUT	15	VOTK+	Tracking drive output (+)
2	CFCerr1	Error-amplifier filter condenser	16	VOTK-	Tracking drive output (−)
3	CFCerr2	Error-amplifier filter condenser	17	VOLD+	Loader drive output(+)
4	VINSL+	Operational amplifier input of sled drive	18	VOLD-	Loading drive output(−)
5	VINSL−	Operational amplifier input of sled drive	19	PGND	Power GND
6	VOSL	Operational amplifier output of sled drive	20	VNFTK	Tracking driver feedback end
7	VNFFC	Focus drive	21	PVcc2	
8	Vcc	Pre Vcc, Sled drive Vcc	22	PreGND	preGND
9	PVcc1	Loading drive output	23	VINLD	Loading drive input
10	PGND	Power GND	24	CTKerr2	Error−amplifier filter condenser
11	VOSL−	Sled drive output	25	CTKerr1	Error−amplifier filter condenser
12	VOSL+	Sled drive output	26	VINTK	Tracking drive input
13	VOFC−	Focus drive output	27	BIAS	Bias input
14	VOFC+	Focus drive output	28	STBY	Standby end

HY57V641620HG(SAMSUNG K4S6416432H)

DESCRIPTION

The Hynix HY57V641620HG is a 67,108,864-bit CMOS Synchronous DRAM, ideally suited for the main memory applications which require large memory density and high bandwidth. HY57V641620HG is organized as 4banks of 1,048,576x16.

HY57V641620HG is offering fully synchronous operation referenced to a positive edge of the clock. All inputs and outputs are synchronized with the rising edge of the clock input. The data paths are internally pipelined to achieve very high bandwidth. All input and output voltage levels are compatible with LVTTL.

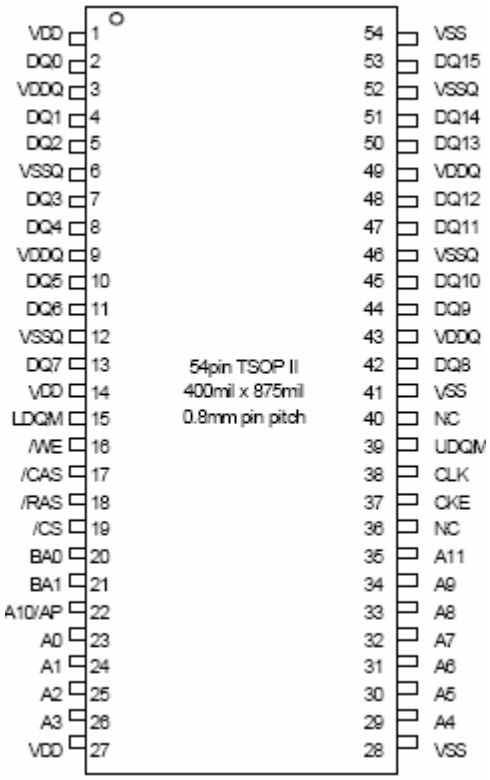
Programmable options include the length of pipeline (Read latency of 2 or 3), the number of consecutive read or write cycles initiated by a single control command (Burst length of 1,2,4,8 or Full page), and the burst count sequence(sequential or interleave). A burst of read or write cycles in progress can be terminated by a burst terminate command or can be interrupted and replaced by a new burst read or write command on any cycle. (This pipelined design is not restricted by a `2N` rule.)

FEATURES

- Single 3.3±0.3V power supply Note)
- Internal four banks operation
- Auto refresh and self refresh
- 4096 refresh cycles / 64ms
- Programmable Burst Length and Burst Type
- Programmable CAS Latency ; 2, 3 Clocks

- 1, 2, 4, 8 or Full page for Sequential Burst
- 1, 2, 4 or 8 for Interleave Burst

- All device pins are compatible with LVTTL interface
- Data mask function by UDQM or LDQM
- JEDEC standard 400mil 54pin TSOP-II with 0.8mmof pin pitch
- All inputs and outputs referenced to positive edge of system clock



PIN DESCRIPTION

PIN	PIN NAME	DESCRIPTION
CLK	Clock	The system clock input. All other inputs are registered to the SDRAM on the rising edge of CLK
CKE	Clock Enable	Controls internal clock signal and when deactivated, the SDRAM will be one of the states among power down, suspend or self refresh
$\overline{CS}$	Chip Select	Enables or disables all inputs except CLK, CKE and DQM
BA0,BA1	Bank Address	Selects bank to be activated during $\overline{RAS}$ activity Selects bank to be read/written during $\overline{CAS}$ activity
A0 ~ A11	Address	Row Address : RA0 ~ RA11, Column Address : CA0 ~ CA7 Auto-precharge flag : A10
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Row Address Strobe, Column Address Strobe, Write Enable	$\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ define the operation Refer function truth table for details
LDQM, UDQM	Data Input/Output Mask	Controls output buffers in read mode and masks input data in write mode
DQ0 ~ DQ15	Data Input/Output	Multiplexed data input / output pin
V_{DD}/V_{SS}	Power Supply/Ground	Power supply for internal circuits and input buffers
V_{DDQ}/V_{SSQ}	Data Output Power/Ground	Power supply for output buffers
NC	No Connection	No connection

DC OPERATING CONDITION (TA=0 to 70°C)

Parameter	Symbol	Min	Typ.	Max	Unit	Note
Power Supply Voltage	VDD, VDDQ	3.0	3.3	3.6	V	1,2
Input High Voltage	VIH	2.0	3.0	VDDQ + 2.0	V	1,3
Input Low Voltage	VIL	VSSQ - 2.0	0	0.8	V	1,4

Note :

1.All voltages are referenced to V_{SS} = 0V

2.V_{IH} (max) is acceptable 5.6V AC pulse width with δ3ns of duration

3.V_{IL} (min) is acceptable -2.0V AC pulse width with δ3ns of duration

AC OPERATING CONDITION (TA=0 to 70°C, VDD=3.3 ± 0.3V[Note2], VSS=0V)

Parameter	Symbol	Value	Unit	Note
AC Input High / Low Level Voltage	VIH / VIL	2.4/0.4	V	
Input Timing Measurement Reference Level Voltage	Vtrip	1.4	V	
Input Rise / Fall Time	tR / tF	1	ns	
Output Timing Measurement Reference Level	Voutref	1.4	V	
Output Load Capacitance for Access Time Measurement	CL	50	pF	1

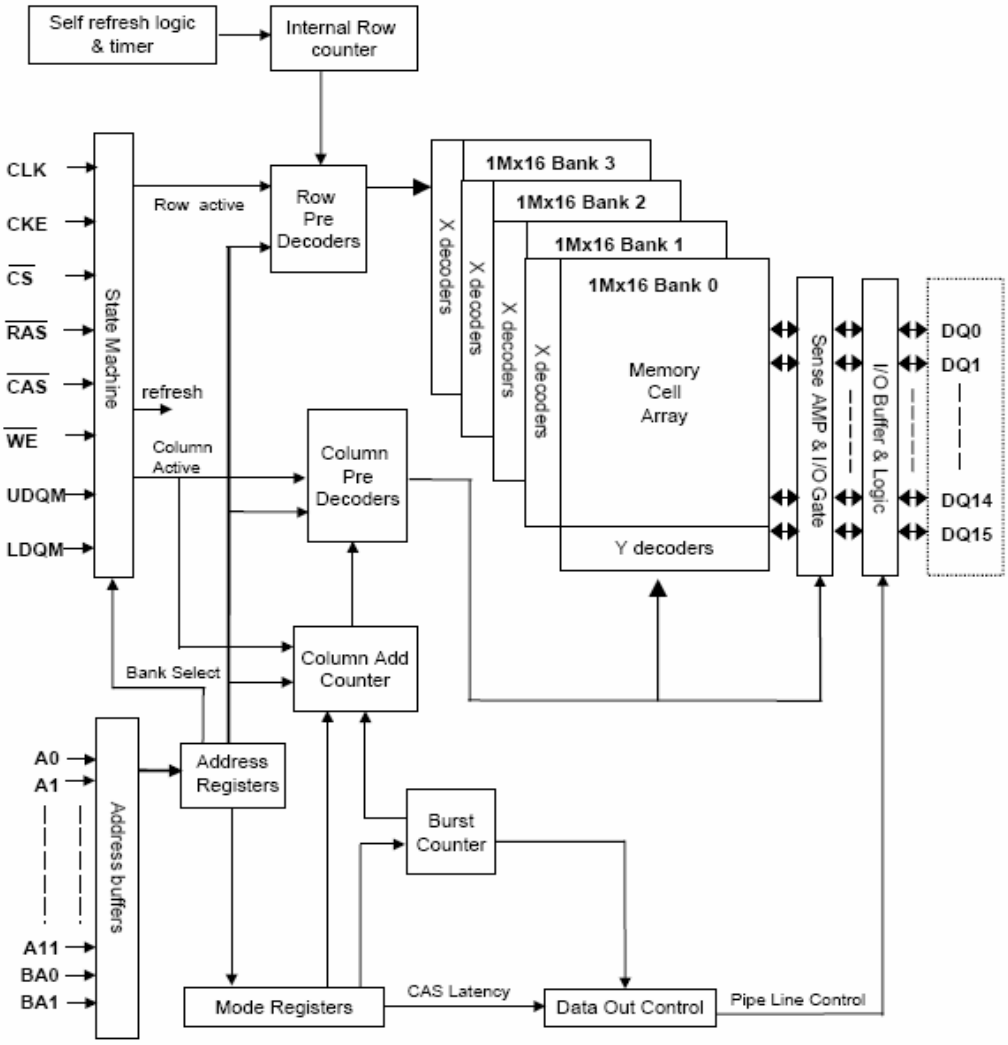
Note :

1. Output load to measure access time is equivalent to two TTL gates and one capacitor (50pF)

For details, refer to AC/DC output circuit

FUNCTIONAL BLOCK DIAGRAM

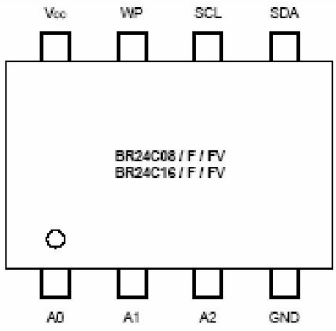
1Mbit x 4banks x 16 I/O Synchronous DRAM



24C16

●Features

- Wide range of operating power supply voltages (2.7V to 5.5V).
- 2-wire serial interface.
- Auto erase and auto completion function when writing data.
- Page write mode function:16byte
- Low current consumption.
  - Operating (at 5V) : 2.0mA (typ.)
  - Standby (at 5V) : 1.0μA (typ.)
- Write protect function.
  - Equipped with WP (write protect) function.
  - Writing disabled when power supply voltage is low.
- Compact DIP8, SOP8, and SSOPB8 packages.
- Highly reliable COMS processing.
- Rewriting possible up to 100,000 times.
- Data can be stored for ten years without corruption.
- Built-in noise filters at SCL and SDA pins.

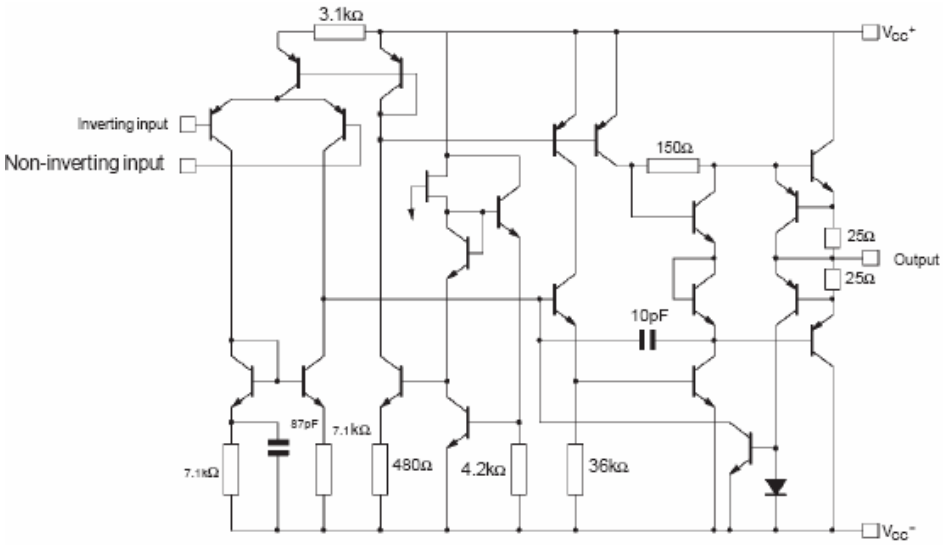


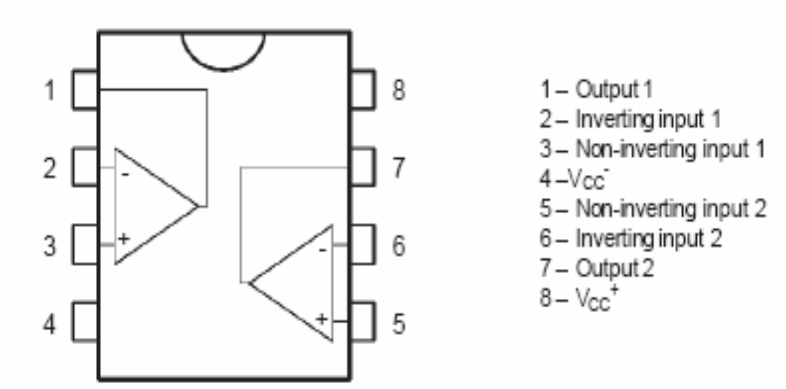
●Operating timing characteristics (unless otherwise noted, Ta = – 40 to + 85°C, Vcc = 2.7V to 5.5V)

Parameter	Symbol	Vcc = 5V ± 10 %			Vcc = 3V ± 10 %			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
SCL frequency	f_{SCL}	—	—	400	—	—	100	kHz
Data clock high time	t_{HIGH}	0.6	—	—	4.0	—	—	μs
Data clock low time	t_{LOW}	1.2	—	—	4.7	—	—	μs
SDA / SCL rise time	t_R	—	—	0.3	—	—	1.0	μs
SDA / SCL fall time	t_F	—	—	0.3	—	—	0.3	μs
Start condition hold time	t_{HD}: STA	0.6	—	—	4.0	—	—	μs
Start condition setup time	t_{SU}: STA	0.6	—	—	4.7	—	—	μs
Input data hold time	t_{HD}: DAT	0	—	—	0	—	—	ns
Input data setup time	t_{SU}: DAT	100	—	—	250	—	—	ns
Output data delay time	t_{PD}	0.1	—	0.9	0.2	—	3.5	μs
Output data hold time	t_{DH}	0.1	—	—	0.2	—	—	μs
Stop condition setup time	t_{SU}: STO	0.6	—	—	4.7	—	—	μs
Bus open time before start of transfer	t_{BUF}	1.2	—	—	4.7	—	—	μs
Internal write cycle time	t_{WR}	—	—	10	—	—	10	ms
Noise erase valid time (SDA / SCL pins)	t_I	—	—	0.05	—	—	0.1	μs

MC4558 wide bandwidth dual bipolar operational amplifiers

- INTERNALLY COMPENSATED
- SHORT–CIRCUIT PROTECTION
- GAIN AND PHASE MATCH BETWEEN AMPLIFIERS
- LOW POWER CONSUMPTION
- GAIN BANDWIDTH PRODUCT (at 100kHz) 5.5MHz





operating characteristics, VDD = 5 V, TA = 25°C, RL = 8 Ω, Gain = –2 V/V, BTL mode

parameter	Test conditions		Min	typ	max	unit
Po out power	THD=1% f=1kHz RL=4 Ω			1.9		W
THD+N Total harmonic distortion plus noise	Po=1W f=20Hz to 15Hz			0.75%		
BOM Maxium output power bandwidth	THD=5%			>15		kHz
Supply ripple rejection ratio	f=1kHz C(BYP)=0.47 μ F	BTL mode		68		dB
SNR				105		dB
Vn noise output voltage	C(BYP)=0.47 μ F f=20Hz to 20kHz	BTL mode		16		μVRMS
		SE mode		30		

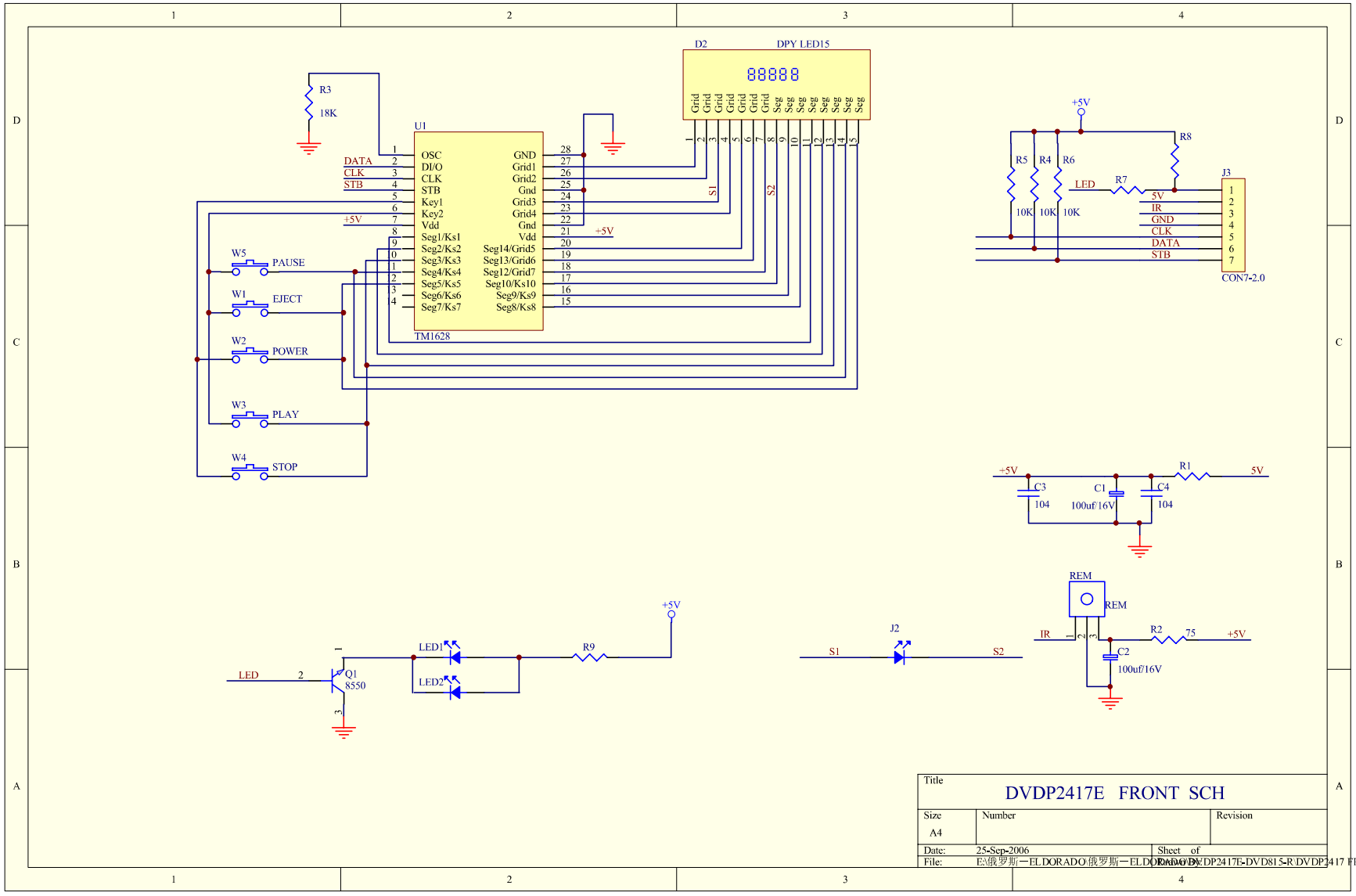
ELECTRICAL CHARACTERISTICS

V_{CC} = ±15V, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{io}	Input Offset Voltage ($R_S \leq 10\ k\Omega$) T_{amb} = 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$		1	 5 6	mV
I_{io}	Input Offset Current T_{amb} = 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$		20	 100 200	nA
I_{ib}	Input Bias Current T_{amb} = 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$		50	 400 500	nA
A_{vd}	Large Signal Voltage Gain (V_O = ±10V, R_L = 2kΩ) T_{amb} = 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$	 50 25	200		V/mV
SVR	Supply Voltage Rejection Ratio ($R_S \leq 10k\Omega$) T_{amb} = 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$	 77 77	90		dB
I_{CC}	Supply Current, all Amp, no Load T_{amb} = 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$		2.3	 4.5 6	mA
V_{icm}	Input Common Mode Voltage Range T_{amb} = 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$	 ±12 ±12			V
CMR	Common-mode Rejection Ratio ($R_S \leq 10k\Omega$) T_{amb} = 25°C $T_{min.} \leq T_{amb} \leq T_{max.}$	 70 70	90		dB
I_{os}	Output Short-circuit Current	10	20	40	mA
V_o	Output Voltage Swing T_{amb} = 25°C R_L = 10kΩ R_L = 2kΩ $T_{min.} \leq T_{amb} \leq T_{max.}$ R_L = 10kΩ R_L = 2kΩ	 ±12 ±10 ±12 ±10	 ±14 ±13		V
SR	Slew Rate (V_I = ±10V, R_L = 2kΩ, C_L = 100pF, T_{amb} = 25°C, unity gain)	1.5	2.2		V/µs
t_r	Rise Time (V_I = ±20mV, R_L = 2kΩ, C_L = 100pF, T_{amb} = 25°C, unity gain)		0.3		µs
K_{OV}	Overshoot (V_I = ±20 mV, R_L = 2kΩ, C_L = 100pF, T_{amb} = 25°C, unity gain)		15		%
R_i	Input Resistance	0.3	2		MΩ
C_i	Input Capacitance		1.4		pF
R_O	Output Resistance		75		Ω
B	Unity Gain Bandwidth		2.8		MHz
GBP	Gain Bandwidth Product (V_I = 10mV, R_L = 2kΩ, C_L = 100pF, f = 100kHz, T_{amb} = 25°C)		5.5		MHz
THD	Total Harmonic Distortion (f = 1kHz, A_v = 20dB, R_L = 2kΩ, V_o = $2V_{pp}$, C_L = 100pF, T_{amb} = 25°C)		0.008		%
e_n	Equivalent Input Noise Voltage (f = 1kHz, R_s = 100Ω)		12		$\frac{nV}{\sqrt{Hz}}$
V_{O1}/V_{O2}	Channel Separation		120		dB

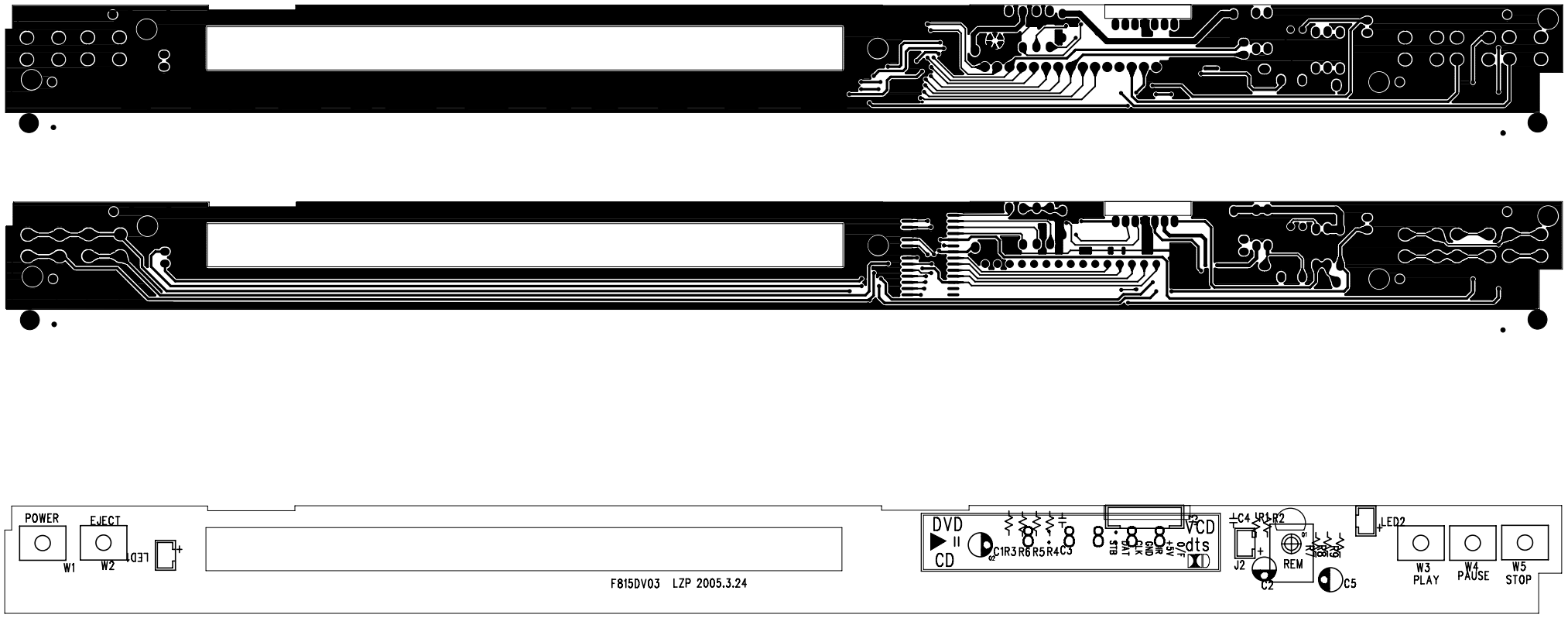
Part 3. Detailed Circuit

Panel Board DVD-2417E



Part 3. Detailed Circuit

Panel Board DVDP2417



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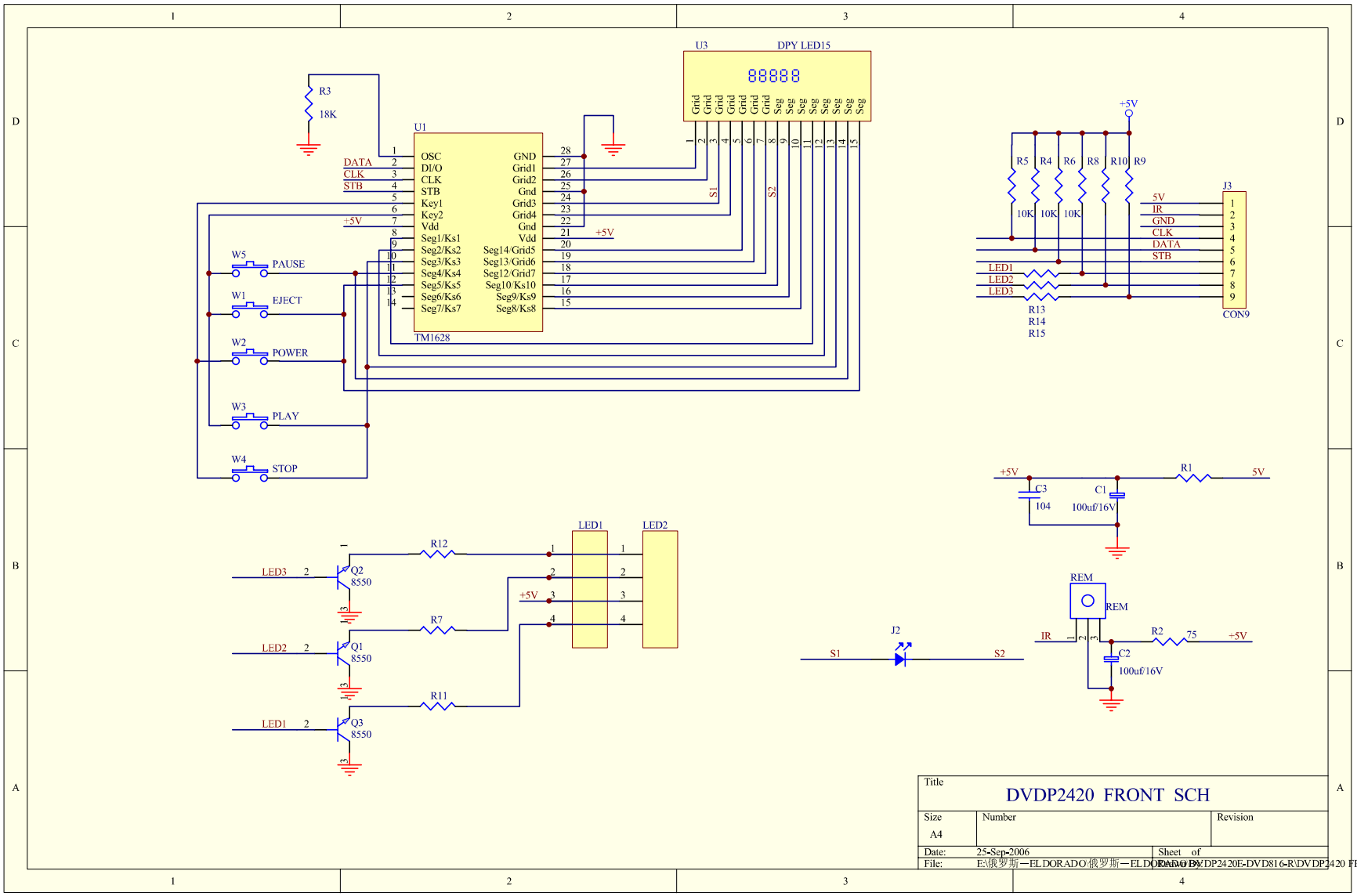
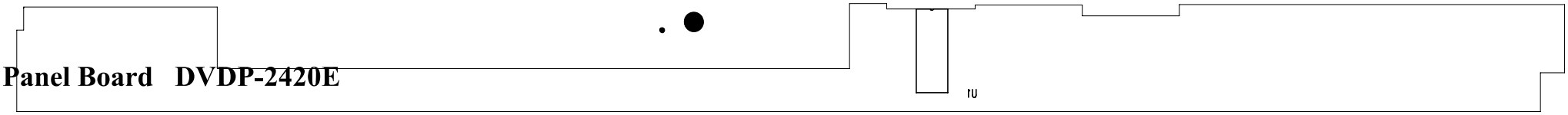
Part 3. Detailed Circuit

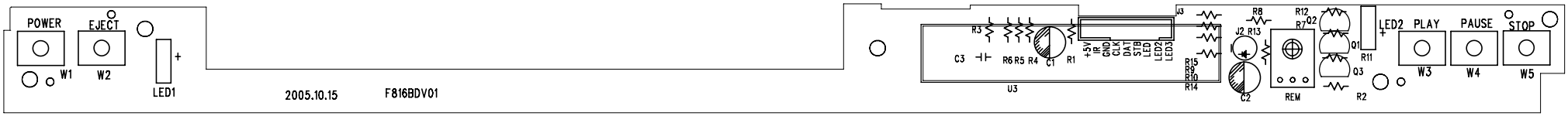
Panel Board DVDP-2420E

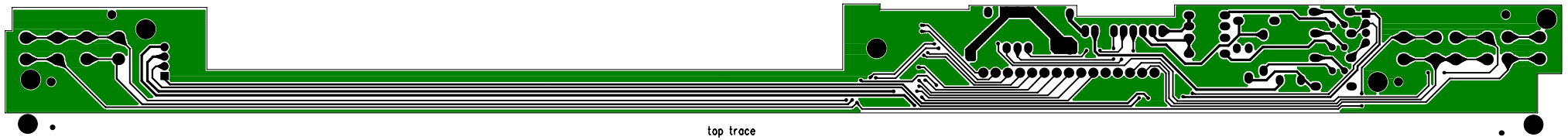


Part 3. Detailed Circuit

Panel Board DVDP-2420E







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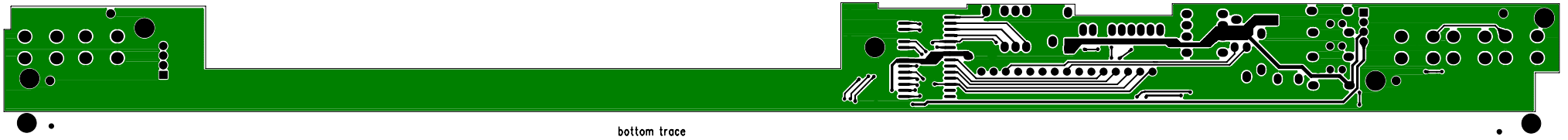
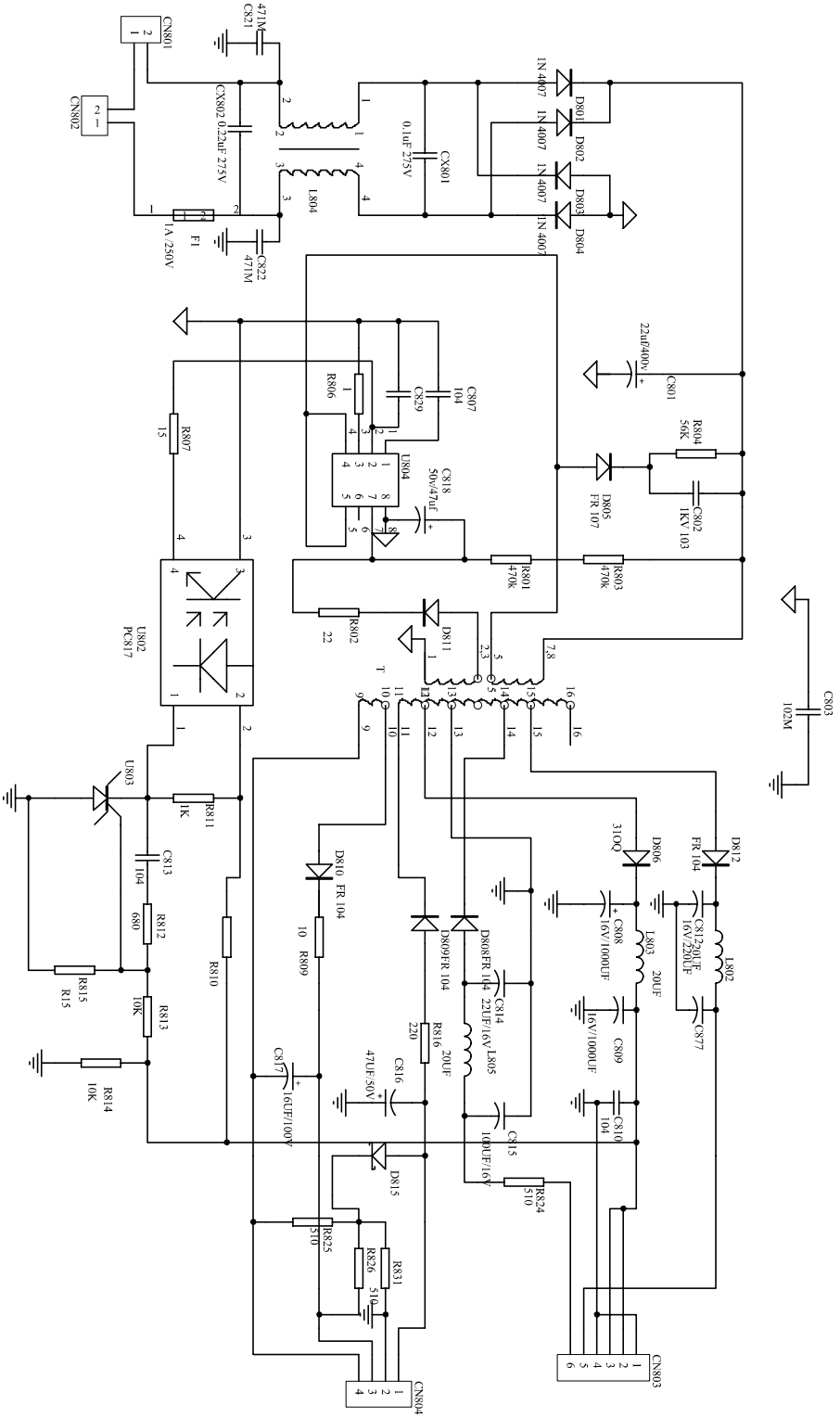


Power Board 10004C VER24



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Power Board 10004C VER24