Features

- **Pulse-width Modulation up to 2 kHz Clock Frequency**
- **Protection Against Short-circuit, Load Dump Overvoltage and Reverse V_S**
- **Duty Cycle 18 to 100% Continuously**
- **Internally Reduced Pulse Slope of Lamp's Voltage**
- **Interference and Damage Protection According to VDE 0839 and ISO/TR 7637/1**
- **Charge-pump Noise Suppression**
- **Ground-wire Breakage Protection**

Description

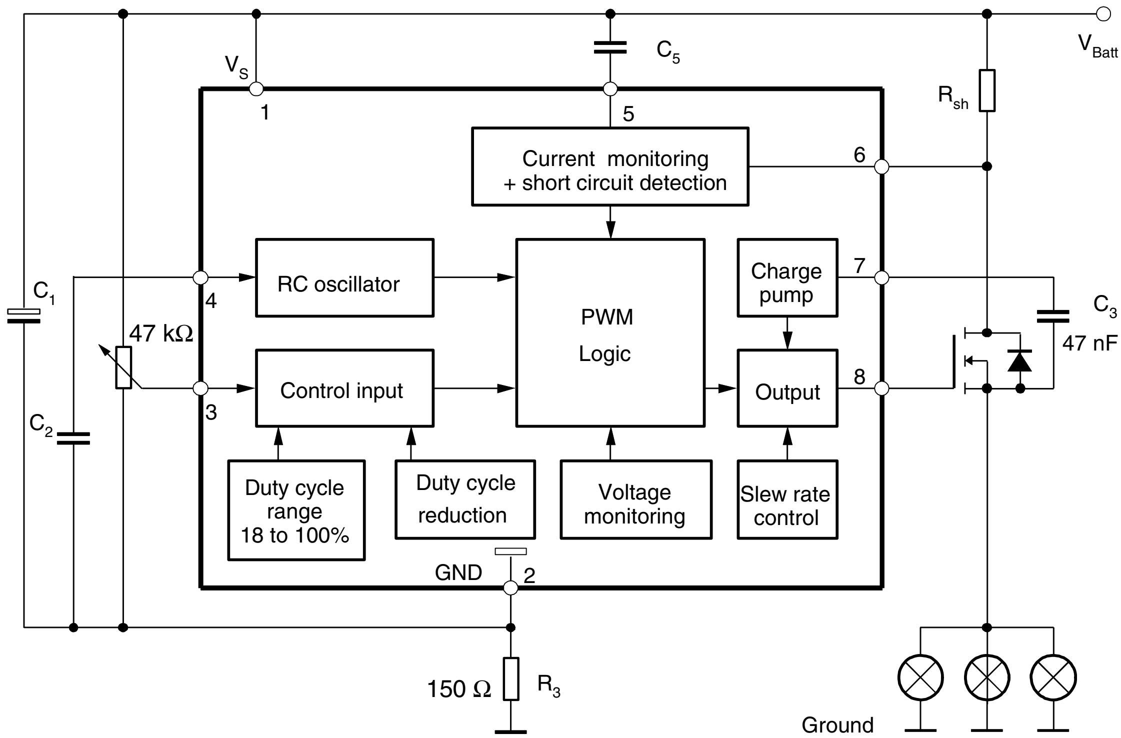
The U6083B is a PWM IC in bipolar technology for the control of an N-channel power MOSFET used as a high-side switch. The IC is ideal for use in brightness control systems (dimming) of lamps, for example, in dashboard applications.

PWM Power Control IC with Interference Suppression

U6083B

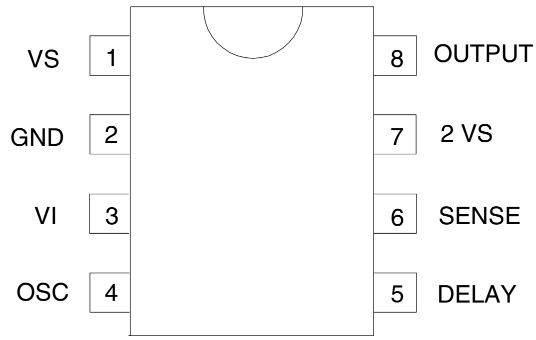
Rev. 4770A–AUTO–11/03

Figure 1. Block Diagram with External Circuit



Pin Configuration

Figure 2. Pinning DIP8



Pin Description

Pin	Symbol	Function
1	VS	Supply voltage V_S
2	GND	IC ground
3	VI	Control input (duty cycle)
4	OSC	Oscillator
5	DELAY	Short-circuit protection delay
6	SENSE	Current sensing
7	2 VS	Voltage doubler
8	OUTPUT	Output

Functional Description

Pin 1, Supply Voltage, V_S or V_{Batt}

Overvoltage Detection

Stage 1

If overvoltages of V_{Batt} > 20 V (typically) occur, the external transistor is switched off, and switched on again at V_{Batt} < 18.5 V (hysteresis).

Stage 2

If V_{Batt} > 28.5 V (typically), the voltage limitation of the IC is reduced from V_S = 26 V to 20 V. The gate of the external transistor remains at the potential of the IC ground, thus producing voltage sharing between FET and lamps in the event of overvoltage pulses (e.g., load dump). The short-circuit protection is not in operation. At V_{Batt} approximately < 23 V, the overvoltage detection stage 2 is switched off. Thus, during overvoltage detection stage 2, the lamp voltage V_{lamp} is calculated as follows:

$V_{Lamp} = V_{Batt} - V_S - V_{GS}$

V_S = supply voltage of the IC at overvoltage detection stage 2

V_{GS} = gate - source voltage of the FET

Undervoltage Detection

In the event of voltages of approximately V_{Batt} < 5.0 V, the external FET is switched off and the latch for short-circuit detection is reset.

A hysteresis ensures that the FET is switched on again at approximately $V_{Batt} \geq 5.4$ V.

Pin 2, GND

Ground-wire Breakage

To protect the FET in the case of ground-wire breakage, a 1 MΩ resistor between gate and source is recommended to provide proper switch-off conditions.

Pin 3, Control Input

The pulse width is controlled by means of an external potentiometer (47 kΩ). The characteristic (angle of rotation/duty cycle) is linear. The duty cycle can be varied from 18 to 100%. It is possible to further restrict the duty cycle with the resistors R_1 and R_2 (see Figure 4 on page 10).

In order to reduce the power dissipation of the FET and to increase the lifetime of the lamps, the IC automatically reduces the maximum duty cycle at pin 8 if the supply voltage exceeds V_2 = 13 V. Pin 3 is protected against short-circuit to V_{Batt} and ground ($V_{Batt} \leq 16.5$ V).

Pin 4, Oscillator

The oscillator determines the frequency of the output voltage. This is defined by an external capacitor, C_2. It is charged with a constant current, I, until the upper switching threshold is reached. A second current source is then activated which taps a double current, 2 × I, from the charging current. The capacitor, C_2, is thus discharged at the current, I, until the lower switching threshold is reached. The second source is then switched off again and the procedure starts once more.

Example for Oscillator Frequency Calculation

Switching thresholds

V_{T100} = High switching threshold (100% duty cycle)

$V_{T100} = V_S \times \alpha_1 = (V_{Batt} - I_S \times R_3) \times \alpha_1$

$V_{T<100}$ = High switching threshold (< 100% duty cycle)

$V_{T<100} = V_S \times \alpha_2 = (V_{Batt} - I_S \times R_3) \times \alpha_2$

V_{TL} = Low switching threshold

$V_{TL} = V_S \times \alpha_3 = (V_{Batt} - I_S \times R_3) \times \alpha_3$

where

α_1, α_2 and α_3 are fixed values

Calculation Example

The above mentioned threshold voltages are calculated for the following values given in the data sheet.

V_{Batt} = 12 V, I_S = 4 mA, R_3 = 150 Ω, α_1 = 0.7, α_2 = 0.67 and α_3 = 0.28

$V_{T100} = (12\text{ V} - 4\text{ mA} \times 150\ \Omega) \times 0.7 \approx 8\text{ V}$

$V_{T<100} = 11.4\text{ V} \times 0.67 = 7.6\text{ V}$

$V_{TL} = 11.4\text{ V} \times 0.28 = 3.2\text{ V}$

Oscillator Frequency

3 cases have to be distinguished

1. f_1 for duty cycle = 100%, no slope reduction with capacitor C_4 (see Figure 4 on page 10)

$$f_1 = \frac{I_{OSC}}{2 \times (V_{T100} - V_{TL}) \times C_2}$$, where C_2 = 68 nF, I_{OSC} = 45 µA

f_1 = ... = 75 Hz

2. f_2 for duty cycle < 100%, no slope reduction with capacitor C_4

For a duty cycle of less than 100%, the oscillator frequency, f, is as follows:

$$f_2 = \frac{I_{OSC}}{2 \times (V_{T<100} - V_{TL}) \times C_2}$$, where C_2 = 68 nF, I_{OSC} = 45 µA

f_2 = ... = 69 Hz

3. f_3 with duty cycle < 100% with slope reduction capacitor C_4 (see "Output Slope Control" on page 6)

$$f_3 = \frac{I_{osc}}{2 \times (V_{T<100} - V_{TL}) \times C_2 + 2V_{Batt} \times C_4}$$

where C_2 = 68 nF, I_{OSC} = 45 µA, C_4 = 1.8 nF

f_3 = ... = 70 Hz

By selecting different values of C_2 and C_4, it is possible to have a range of oscillator frequencies from 10 to 2000 Hz as shown in the data sheet.

Output Slope Control

The slope of the lamp voltage is internally limited to reduce radio interference by limitation of the voltage gain of the PWM comparator.

Thus, the voltage rise on the lamp is proportional to the oscillator voltage increase at the switchover time according to the equation.

$dV_8/d_t = \alpha_4 \times dV_4/d_t = 2 \times \alpha_4 \times f \times (\alpha_2 - \alpha_3) \times (V_{Batt} - I_S \times R_3)$

when

$f = 75$ Hz, $V_{TX} = V_T < 100$ and $\alpha_4 = 63$

then

$dV_8/d_t = 2 \times 63 \times 75\ \text{Hz} \times (0.67 - 0.28) \times (12\ \text{V} - 4\ \text{mA} \times 15\ \Omega) = 42\ \text{V/ms}$

Via an external capacitor, C_4, the slope can be further reduced as follows:

$dV_8/d_t = I_{OSC}/(C_4 + C_2/\alpha_4)$

when

$I_{OSC} = 45\ \mu\text{A}$, $C_4 = 1.8$ nF, $C_2 = 68$ nF and $\alpha_4 = 63$

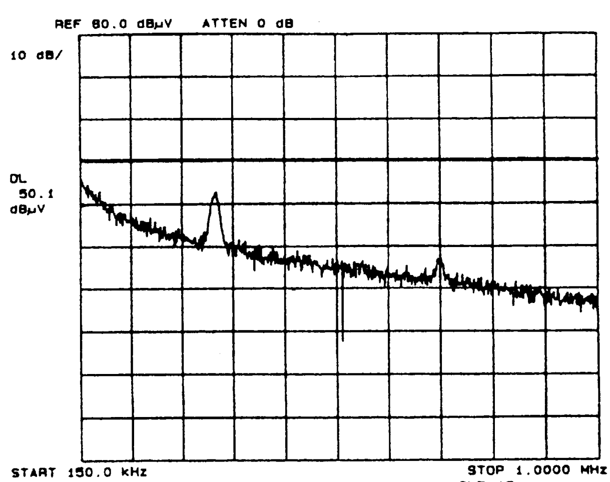
then $dV_8/d_t = 45\ \mu\text{A}/(1.8\ \text{nF} + 68\ \text{nF}/63) = 15.6\ \text{V/ms}$

To damp oscillation tendencies, a resistance of 100 Ω in series with capacitance C_4 is recommended.

Interference Suppression

- "On-board" radio reception according to VDE 0879 part 3/4.81
- Test conditions refering to Figure 3
- Application circuit according to Figure 1 on page 2 or Figure 4 on page 10
- Load: nine 4 W lamps in parallel
- Duty cycle = 18%
- $V_{Batt} = 12$ V
- $f_{Osc} = 100$ Hz

Figure 3. Voltage Spectrum of On-board Radio Reception



Pins 5 and Pin 6, Short-circuit Protection and Current Sensing

Short-circuit Detection and Time Delay, t_d

The lamp current is monitored by means of an external shunt resistor. If the lamp current exceeds the threshold for the short-circuit detection circuit ($V_{T2} \approx 90$ mV), the duty cycle is switched over to 100% and the capacitor C_5 is charged by a current source of I_{ch} - I_{dis}. The external FET again is switched off after the cut-off threshold (V_{T5}) is reached. Switching on the FET again is possible after a power-on reset only. The current source, I_{dis}, ensures that the capacitor C_5 is not charged by parasitic currents.

The time delay, t_d, is calculated as follows:

$t_d = C_5 \times V_{T5}/(I_{ch} - I_{dis})$

With C_5 = 100 nF and V_{T5} = 10.4 V, I_{ch} =13 µA, I_{dis} = 3 µA, the time delay is as follows:

t_d = 100 nF × 10.4 V/(13 µA - 3 µA)

t_d = 104 ms

Current Limitation

The lamp current is limited by a control amplifier to protect the external power transistor. The voltage drop across the external shunt resistor acts as the measured variable. Current limitation takes place for a voltage drop of $V_{T1} \approx 100$ mV. Owing to the difference $V_{T1} - V_{T2} \approx 10$ mV, it ensures that current limitation occurs only when the short-circuit detection circuit has responded.

After a power-on reset, the output is inactive for half an oscillator cycle. During this time, the supply voltage capacitor can be charged so that current limitation is guaranteed in the event of a short-circuit when the IC is switched on for the first time.

Pins 7 and 8, Charge Pump and Output

Pin 8 (output) is suitable for controlling a power MOSFET. During the active integration phase, the supply current of the operational amplifier is mainly supplied by the capacitor C_3 (bootstrapping). In addition, a trickle charge is generated by an integrated oscillator ($f_7 \approx 400$ kHz) and a voltage doubler circuit. This permits a gate voltage supply at a duty cycle of 100%.

Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameters	Symbol	Value	Unit
Junction temperature	T_j	150	°C
Ambient temperature range	T_{amb}	-40 to +110	°C
Storage temperature range	T_{stg}	-55 to +125	°C

Thermal Resistance

Parameters	Symbol	Value	Unit
Junction ambient	R_{thJA}	120	K/W

Electrical Characteristics

T_{amb} = -40°C to +110°C, V_{Batt} = 9 to 16.5 V, (basic function is guaranteed between 6.0 V to 9.0 V) reference point ground, unless otherwise specified (see Figure 1 on page 2). All other values refer to pin GND (pin 2).

Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit
Current consumption		1	I_S			7.9	mA
Supply voltage	Overvoltage detection, stage 1		V_{Batt}			25	V
Stabilized voltage	I_S = 10 mA	1	V_s	24.5		27.0	V
Battery undervoltage detection	on off		V_{Batt}	4.4 4.8	5.0 5.4	5.6 6.0	V
Battery Overvoltage Detection							
Stage 1:	on off		V_{Batt}	18.3 16.7	20.0 18.5	21.7 20.3	V V
Stage 2: Detection stage 2	on off		V_{Batt}	25.5 19.5	28.5 23.0	32.5 26.5	V V
Stabilized voltage	I_S = 30 mA	1	V_s	18.5	20.0	21.5	V
Short-circuit Protection		6					
Short-circuit current limitation	$V_{T1} = V_S - V_6$		V_{T1}	85	100	120	mV
Short-circuit detection	$V_{T2} = V_S - V_6$		V_{T2}	75	90	105	mV
	$V_{T2} = V_S - V_6$		$V_{T1} - V_{T2}$	3	10	30	mV
Delay Timer Short-ciruit Detection, V_{Batt} = 12 V		5					
Switched off threshold	$V_{T5} = V_S - V_5$		V_{T5}	10.2	10.4	10.6	V
Charge current			I_{ch}		13		µA
Discharge current			I_{dis}		3		µA
Capacitance current	$I_5 = I_{ch} - I_{dis}$		I_5	5	10	15	mA
Voltage Doubler		7					
Voltage	Duty cycle 100%		V_7	2 V_S			
Oscillator frequency			f_7	280	400	520	kHz
Internal voltage limitation	I_7 = 5 mA (whichever is lower)		V_7	26	27.5	30.0	V
			V_7	V_{S+14}	V_{S+15}	V_{S+16}	V
Edge steepness	$dv_8/dt = \alpha_4\ dV_4/dt$ dV_8/dt_{max}		α_4	53	63	72 130	V/ms
Gate Output		8					
Voltage	Low level		V_8	0.35	0.70	0.95	V
	V_{Batt} = 16.5 V T_{amb} = 110°C, R_3 = 150 Ω		V_8			1.5[(1)]	V
	High level, duty cycle 100%		V_8		V_7		V
Current	V_8 = Low level		I_8	1.0			mA
	V_8 = High level, $I_7 > \lvert I_8 \rvert$		I_8	-1.0			mA
Duty cycle	Min: C_2 = 68 nF Max: $V_{Batt} \leq 12.4$ V V_{Batt} = 16.5 V, C_2 = 68 nF		t_p/T	15 100 65	18 73	21 81	%

Note: 1. Reference point is battery ground

Electrical Characteristics (Continued)

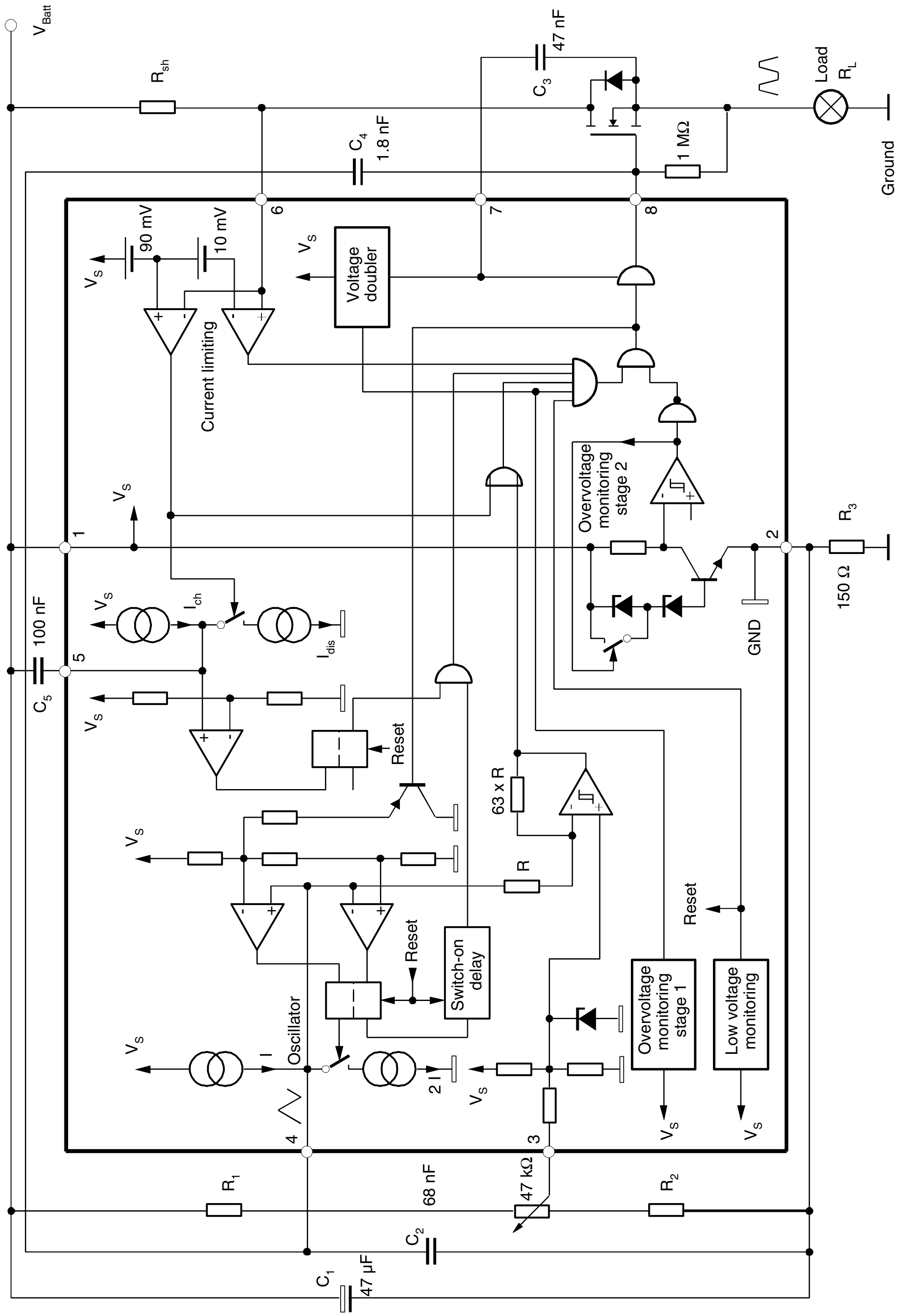
T_{amb} = -40°C to +110°C, V_{Batt} = 9 to 16.5 V, (basic function is guaranteed between 6.0 V to 9.0 V) reference point ground, unless otherwise specified (see Figure 1 on page 2). All other values refer to pin GND (pin 2).

Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit
Oscillator							
Frequency		4	f	10		2000	Hz
Threshold cycle	$V_8 = \text{High}, \alpha_1 = \frac{V_{T100}}{V_S}$		α_1	0.68	0.7	0.72	
Upper	$V_8 = \text{Low}, \alpha_2 = \frac{V_{T<100}}{V_S}$		α_2	0.65	0.67	0.69	
Lower	$\alpha_3 = \frac{V_{TL}}{V_S}$		α_3	0.26	0.28	0.3	
Oscillator current	V_{Batt} = 12 V		$\pm I_{OSC}$	34	45	54	µA
Frequency	C_4 open, C_2 = 68 nF duty cycle = 50%		f	56	75	90	Hz

Note: 1. Reference point is battery ground

Application

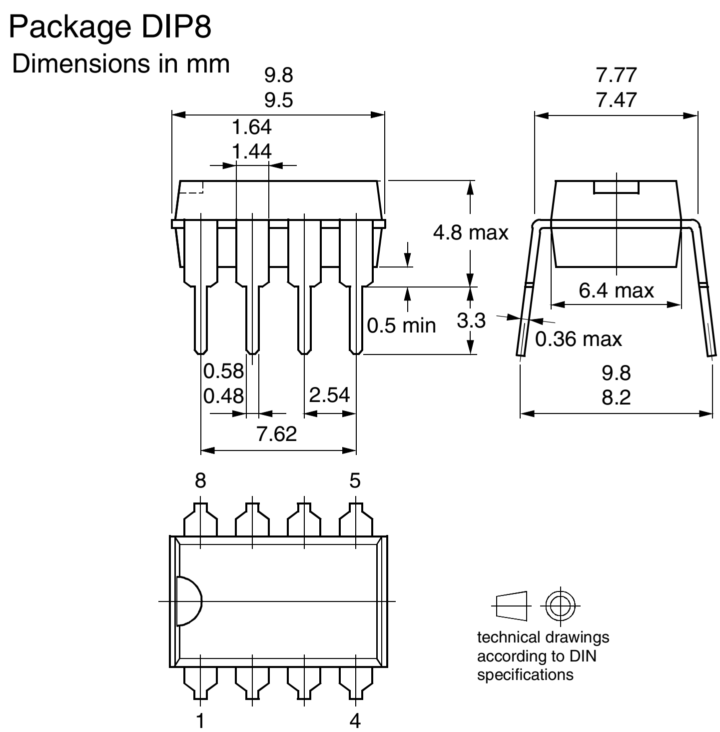
Figure 4. Application Circuit



Ordering Information

Extended Type Number	Package	Remarks
U6083B	DIP8	–

Package Information



Atmel Corporation

2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

Regional Headquarters

Europe
Atmel Sarl
Route des Arsenaux 41
Case Postale 80
CH-1705 Fribourg
Switzerland
Tel: (41) 26-426-5555
Fax: (41) 26-426-5500

Asia
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimshatsui
East Kowloon
Hong Kong
Tel: (852) 2721-9778
Fax: (852) 2722-1369

Japan
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Atmel Operations

Memory
2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

Microcontrollers
2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

La Chantrerie
BP 70602
44306 Nantes Cedex 3, France
Tel: (33) 2-40-18-18-18
Fax: (33) 2-40-18-19-60

ASIC/ASSP/Smart Cards
Zone Industrielle
13106 Rousset Cedex, France
Tel: (33) 4-42-53-60-00
Fax: (33) 4-42-53-60-01

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906, USA
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Scottish Enterprise Technology Park
Maxwell Building
East Kilbride G75 0QR, Scotland
Tel: (44) 1355-803-000
Fax: (44) 1355-242-743

RF/Automotive
Theresienstrasse 2
Postfach 3535
74025 Heilbronn, Germany
Tel: (49) 71-31-67-0
Fax: (49) 71-31-67-2340

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906, USA
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Biometrics/Imaging/Hi-Rel MPU/
High Speed Converters/RF Datacom
Avenue de Rochepleine
BP 123
38521 Saint-Egreve Cedex, France
Tel: (33) 4-76-58-30-00
Fax: (33) 4-76-58-34-80

Literature Requests
www.atmel.com/literature

Printed on recycled paper.

4770A–AUTO–11/03