USB 2.0 Connector

NOTE: USB High Speed not available for the STMP3501, STMP3505, or the STMP3506.

Route USB D+ and D- according to the High Speed USB2.0 Design Guidelines.

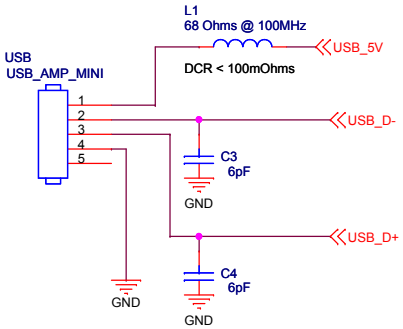
D+ and D- should have a 90 ohm differential trace impedance.

Use 20 mil minimum spacing between D+ and D- and other signal lines.

In order to maximize ESD immunity, the industrial design plastics should expose the USB Connector as little as possible.

L22 is a placeholder for optional ferrite that can be populated for ESD immunity if necessary. If it is not required, populate a 0 ohm resistor. If populated, a ferrite with a low DCR (<100mOhms) should be used.

CN1 Pins 6-9 are pins connecting to the USB connector outer shield

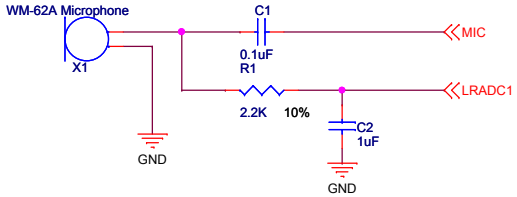


Microphone Bias Options

OPTION 1: Microphone using LRADC1 MIC_BIAS

Using the LRADC MIC_Bias improves power consumption, since the MIC_Bias can be disabled when not being used.

Note: If the LRADC1 line is unavailable, LRADC2 may be used for the Microphone Bias. If both LRADC1 and LRADC2 are unavailable, use OPTION 2.



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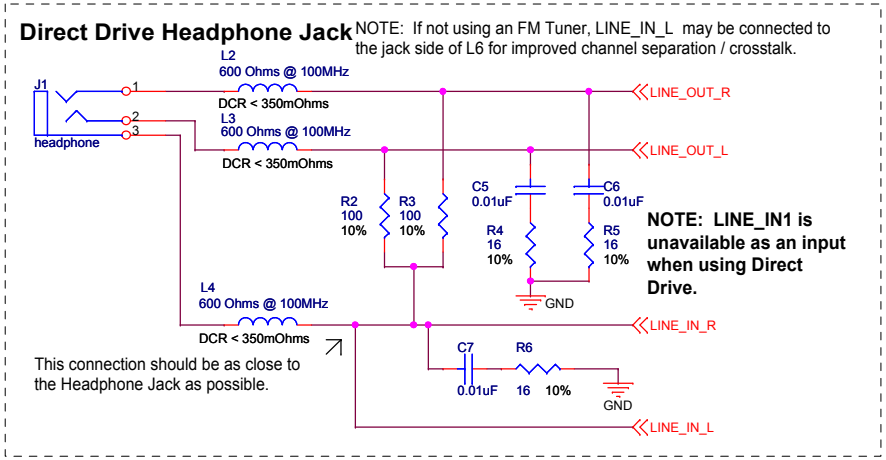
Rev: H

Date: Thursday, August 12, 2004

144BGA STMP35XX AUDIO OPTIONS

NOTE: BGA package not available for the STMP3501.

For a design using a 144BGA with FM Tuner or Line-In Jack:



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Sheet 2 of 8

STMP35XX 144-Pin BGA 2 Channel BUCK MODE

This circuit shows STMP35XX in a Li-Ion buck-mode configuration. This schematic assumes a Li-Ion battery voltage of 3.0V to 4.2V. The Li-Ion battery will be recharged using USB_5V as a source, with the charge current being delivered through the BATT pin.

NOTE: BGA package and Buck Mode are not available for the STMP3501.

NOTE: Battery charge is only available on the STMP3550 and STMP3560.

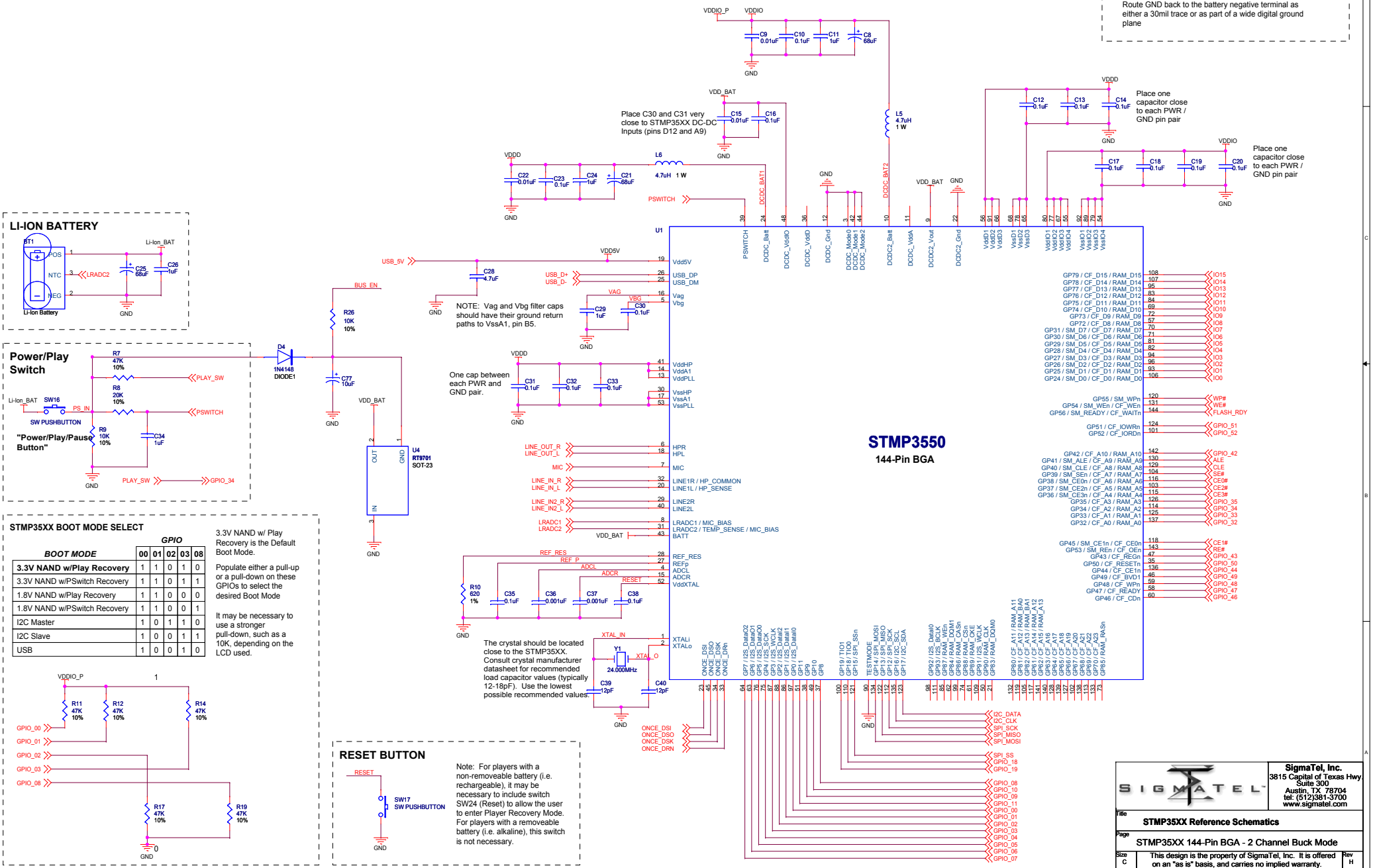
IMPORTANT DESIGN NOTES

The L2 and L18 inductors are critical components - for best battery life, these inductors should be a quality, low-ESR inductor. The Panasonic ELL6H inductor or equivalent is recommended.

The industrial design plastics should mechanically prevent a battery accidentally inserted backwards from making contact with the battery terminals.

Route VDD_BAT as a 30mil trace from the positive battery terminal to the STMP35XX input.

Route GND back to the battery negative terminal as either a 30mil trace or as part of a wide digital ground plane



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Page: STMP35XX 144-Pin BGA - 2 Channel Buck Mode

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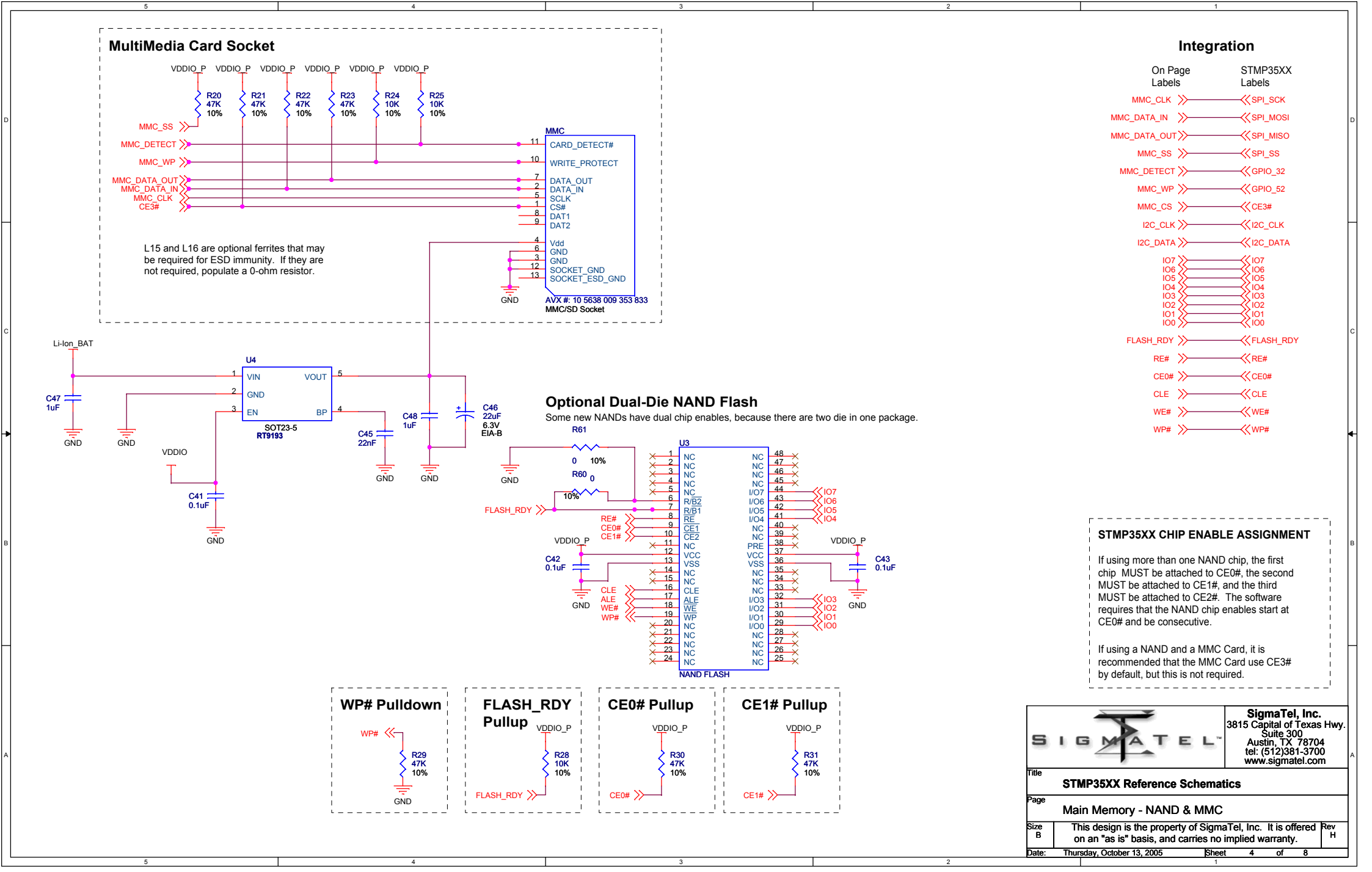
Date: Wednesday, March 23, 2005 | Sheet 3 of 8


MultiMedia Card Socket
VDDIO_P
R20 47K 10%
R21 47K 10%
R22 47K 10%
R23 47K 10%
R24 10K 10%
R25 10K 10%
MMC_SS
MMC_DETECT
MMC_WP
MMC_DATA_OUT
MMC_DATA_IN
MMC_CLK
CE3#
MMC
CARD_DETECT#
WRITE_PROTECT
DATA_OUT
DATA_IN
SCLK
CS#
DAT1
DAT2
Vdd
GND
SOCKET_GND
SOCKET_ESD_GND
AVX #: 10 5638 009 353 833
MMC/SD Socket
L15 and L16 are optional ferrites that may be required for ESD immunity. If they are not required, populate a 0-ohm resistor.
Li-Ion_BAT
U4
VIN
VOUT
GND
EN
BP
SOT23-5
RT9193
C47 1uF
C48 1uF
C46 22uF 6.3V EIA-B
C45 22nF
C41 0.1uF
VDDIO
Optional Dual-Die NAND Flash
Some new NANDs have dual chip enables, because there are two die in one package.
R61 0 10%
R60 0 10%
U3
NAND FLASH
FLASH_RDY
RE#
CE0#
CE1#
CLE
ALE
WE#
WP#
IO7
IO6
IO5
IO4
IO3
IO2
IO1
IO0
C42 0.1uF
C43 0.1uF
Integration
On Page Labels
STMP35XX Labels
MMC_CLK SPI_SCK
MMC_DATA_IN SPI_MOSI
MMC_DATA_OUT SPI_MISO
MMC_SS SPI_SS
MMC_DETECT GPIO_32
MMC_WP GPIO_52
MMC_CS CE3#
I2C_CLK I2C_CLK
I2C_DATA I2C_DATA
FLASH_RDY FLASH_RDY
RE# RE#
CE0# CE0#
CLE CLE
WE# WE#
WP# WP#
STMP35XX CHIP ENABLE ASSIGNMENT
If using more than one NAND chip, the first chip MUST be attached to CE0#, the second MUST be attached to CE1#, and the third MUST be attached to CE2#. The software requires that the NAND chip enables start at CE0# and be consecutive.
If using a NAND and a MMC Card, it is recommended that the MMC Card use CE3# by default, but this is not required.
WP# Pulldown
R29 47K 10%
FLASH_RDY Pullup
R28 10K 10%
CE0# Pullup
R30 47K 10%
CE1# Pullup
R31 47K 10%
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Main Memory - NAND & MMC
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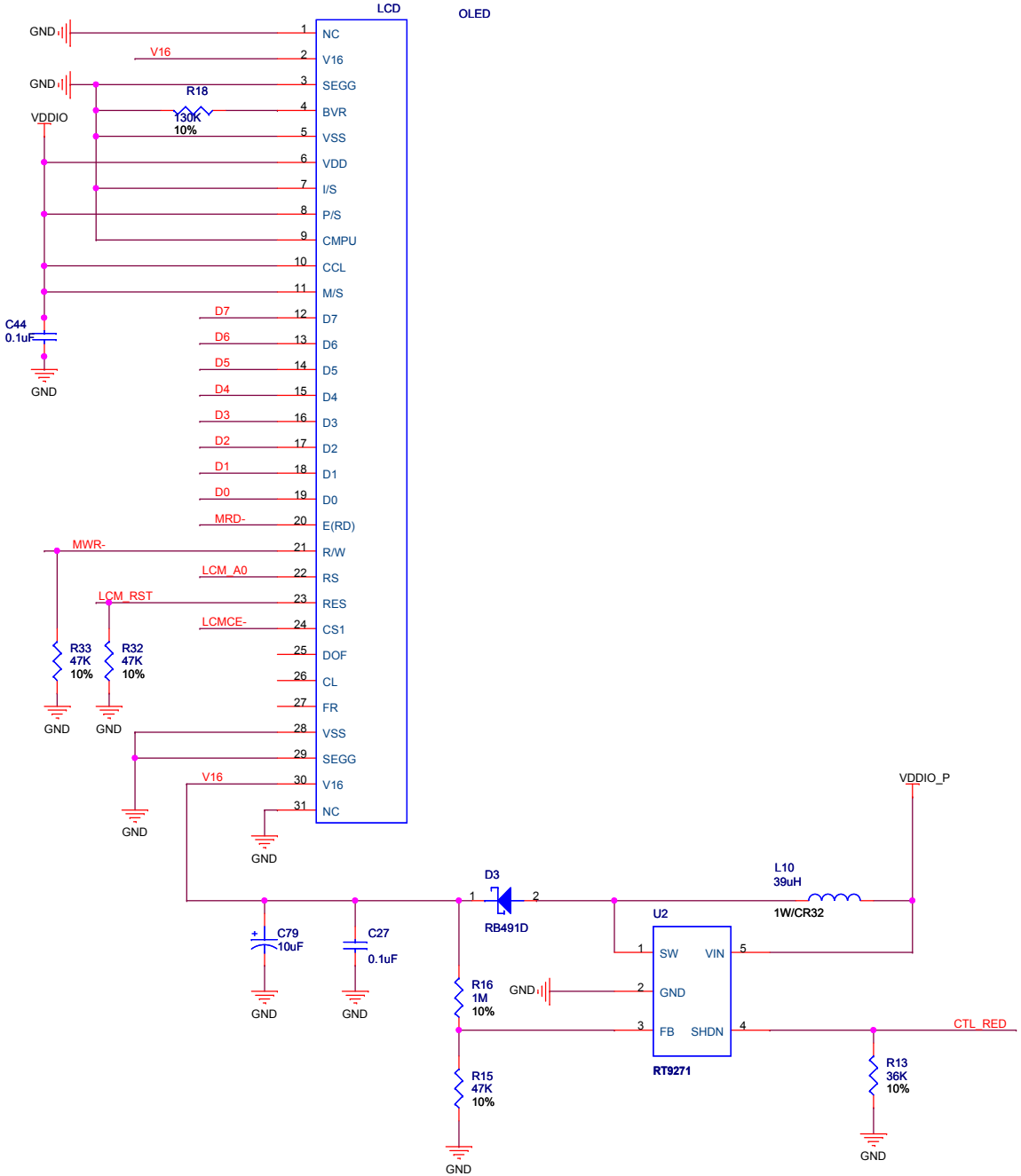
Sheet 4 of 8



Integration

On Page Labels	STMP35XX Labels
LCD_CS#	GPIO_08
LCD_DS	GPIO_10
LCD_RS	GPIO_11
LCD_D0	GPIO_00
LCD_D1	GPIO_01
LCD_D2	GPIO_02
LCD_D3	GPIO_03
LCD_D4	GPIO_04
LCD_D5	GPIO_05
LCD_D6	GPIO_06
LCD_D7	GPIO_07
LCD_RESET	GPIO_44
BL_ON	GPIO_09
GPIO_19	GPIO_19
GPIO_18	GPIO_18

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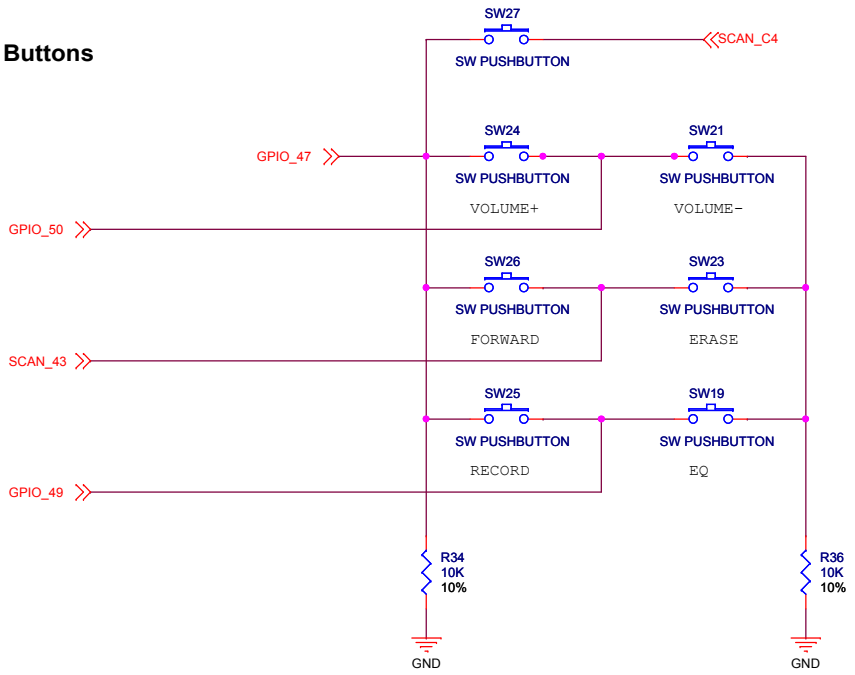
Integration

On Page Labels	STMP35XX Labels
SCAN_C4	GPIO_42
SCAN_C3	GPIO_46
SCAN_C2	GPIO_47
SCAN_C1	GPIO_48
SCAN_R3	GPIO_50
SCAN_R2	GPIO_43
SCAN_R1	GPIO_49
HOLD_SW	GPIO_35

Buttons



NOTE: If the HOLD switch or certain button SCAN lines are not required for your design, you MUST either include pull-down resistors on the HOLD, SCAN_R1, SCAN_R2, and SCAN_R3 lines OR disable the unused lines in the firmware.

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Page: Buttons

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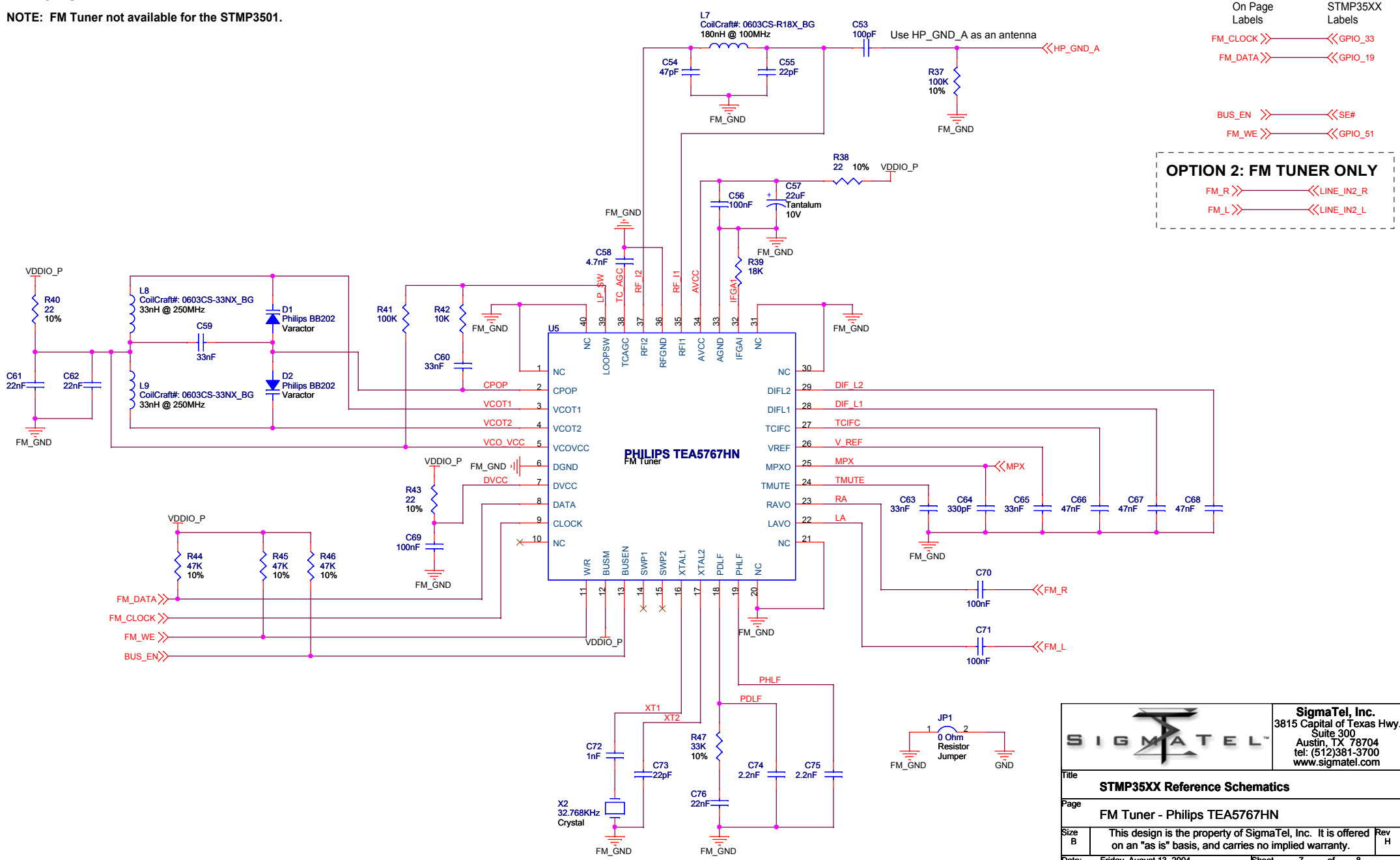
FM Tuner

NOTE: FM Tuner not available for the STMP3501.



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Page: FM Tuner - Philips TEA5767HN

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Sheet 7 of 8

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Page
Optional Circuits

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C

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