Class AB Stereo Headphone Driver with Mute

Features

- **High Signal-to-Noise Ratio**
- **High Slew Rate**
- **Low Distortion**
- **Large Output Voltage Swing**
- **Flexible Mute Function**
- **Excellent Power Supply Ripple Rejection**
- **Low Power Consumption**
- **Short-Circuit Elimination**
- **Wide Temperature Range**
- **No Switch ON/OFF Clicks**
- **Integrated Voltage Divider (V_{DD}/2) to Eliminate External Resistors**
- **Lead Free and Green Devices Available (RoHS Compliant)**

General Description

The APA3541/4 is an integrated class AB stereo headphone driver contained in a SOP-8 or a DIP-8 plastic package with Mute feature. Besides the common Mute feature, the APA3541/4 further integrates a voltage divider inside the chip. Thus, the external resistors can be eliminated. The APA3541 has a fixed gain of 0dB and the APA3544 has a fixed gain of 6dB so that external gain setting is unnecessary. The device is fabricated in a CMOS process and has been primarily developed for portable digital audio applications.

Applications

- **Portable Digital Audio**

Ordering and Marking Information

APA3541/4 □□-□□□ Assembly Material Handling Code Temperature Range Package Code		Package Code J : DIP - 8 K : SOP - 8 Temperature Range I : - 40 to 85 °C Handling Code TU : Tube TR : Tape & Reel Assembly Material G : Halogen and Lead Free Device
APA3541/4 J :	APA3541/4 XXXXX	XXXXX - Date Code
APA3541/4 K :	APA3541/4 XXXXX	XXXXX - Date Code

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020C for MSL classification at lead-free peak reflow temperature. ANPEC defines “Green” to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
V_{DD}	Supply Voltage	7	V
$t_{SC(O)}$	Output Short-circuit Duration, at T_A=25°C, P_{tot}=1W	20	S
T_A	Operating Ambient Temperature range	-40 to 85	°C
T_J	Maximum Junction Temperature	150	°C
T_{STG}	Storage Temperature Range	-65 to +150	°C
T_S	Maximum Lead Soldering Temperature, 10 Seconds	260	°C

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

Symbol	Parameter		Typical Value	Unit
θ_{JA}	Thermal Resistance from Junction to Ambient in Free Air (Note 2)	DIP-8	108	°C/W
		SOP-8	210	
θ_{JC}	Thermal Resistance from Junction to Case	DIP-8	45	°C/W
		SOP-8	40	

Note 2: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air.

Electrical Characteristics

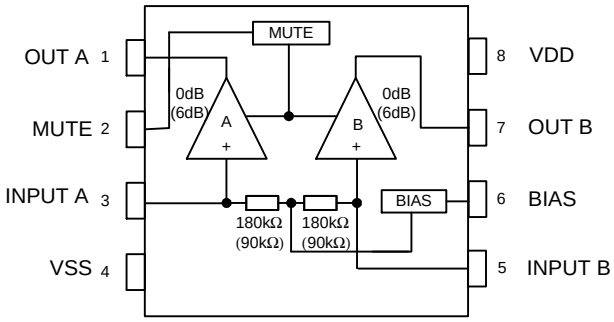
V_{IN}=0dBV, V_{DD}=5V, T_A=25°C, f_{in}=1kHz, R_L=32Ω (unless otherwise noted)

Symbol	Parameter	Test Conditions		APM3541/4			Unit
				Min.	Typ.	Max.	
V_{DD}	Supply Voltage			3.0	5.0	6.0	V
I_Q	Quiescent Current	V_{IN}= 0 V_{rms}		-	3.5	5	mA
I_{mute}	Mute Current			-	200	-	μA
V_{TM}	Mute Terminal Voltage			0.3	0.7	1.6	V
ΔGVCL	Differential Channel Voltage Gain			-0.5	0	0.5	dB
GVCL	Voltage Gain	V_{IN}=1V_{rms},f_{in}= 1kHz,R_L=32Ω	APA3541	-2	0	2	dB
		V_{IN}=0.5V_{rms}, f_{in}=1kHz,R_L=32Ω	APA3544	4	6	8	
THD+N	Total Harmonic Distortion Factor Plus Noise	BW<80kHz		-	0.03	0.1	%
P_{U1}	Rated Output Power1	R_L=32Ω,THD+N=0.1%,BW<80kHz	APA3541	50	55	-	mW
			APA3544	75	80	-	
P_{U2}	Rated Output Power2	R_L=16Ω,THD+N=0.1%,BW<80kHz	APA3541	105	110	-	mW
			APA3544	140	145	-	
V_n	Output Noise Voltage	BW=20~20kHz, V_{IN}=0V_{rms}		-	-93	-85	dBV
Crosstalk	Channel Separation	f_{in}=1kHz	APA3541	-90	-95	-	dB
			APA3544	-65	-70	-	
$Mute_{ATT}$	Mute Attenuation	V_{IN}=1V_{rms},f_{in}=1kHz,Mute=0V	65	70	-	dB	
PSRR	Power Supply Reject Ratio	f_{rr}=100Hz,V_{rr}=-20dBV	50	60	-	dB	

Pin Description

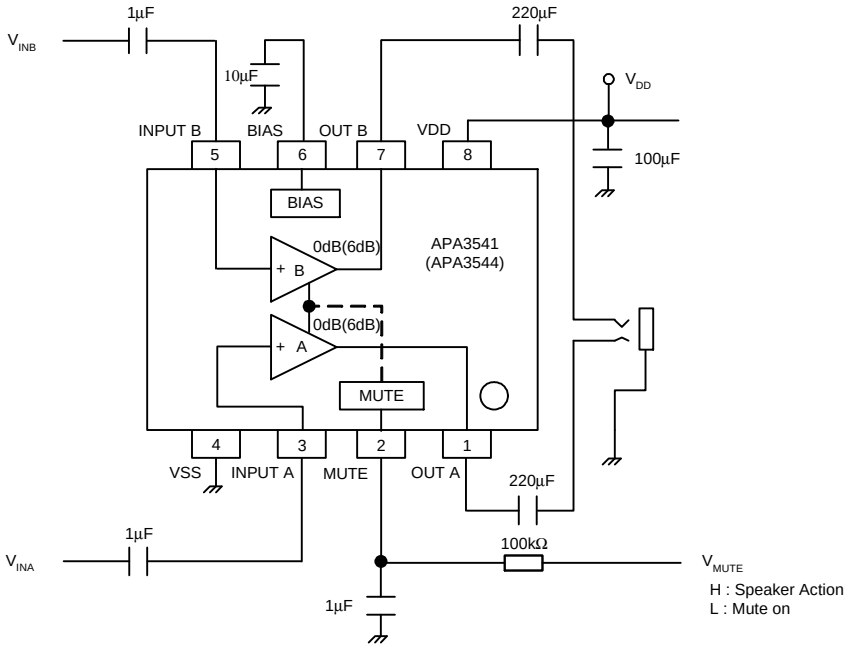
PIN NAME	I/O	FUNCTION
OUT A	O	A channel output pin
MUTE	I	Chip disable control input, low active and high for normal operating
INPUT A	I	A channel input terminal
VSS		Power ground pin
INPUT B	I	B channel input terminal
BIAS	I	Right channel bias input pin
OUT B	O	B channel output pin
V_{DD}		Power input pin

Block Diagram



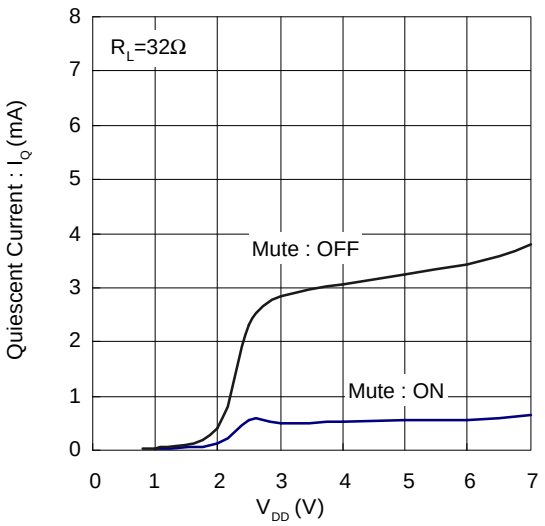
* The values in parenthesis are for the APA3544.

Test and Application Circuit

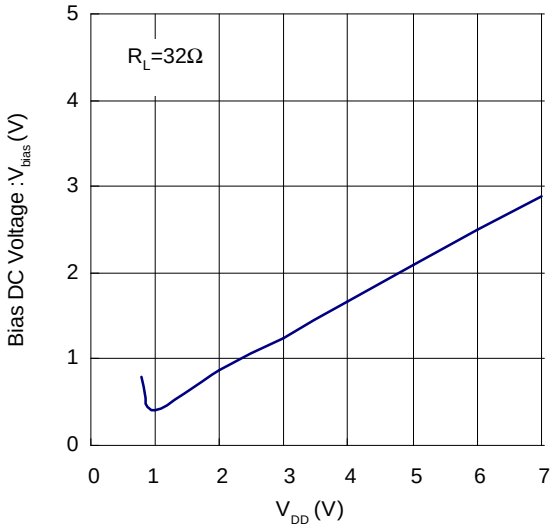


Typical Operating Characteristics

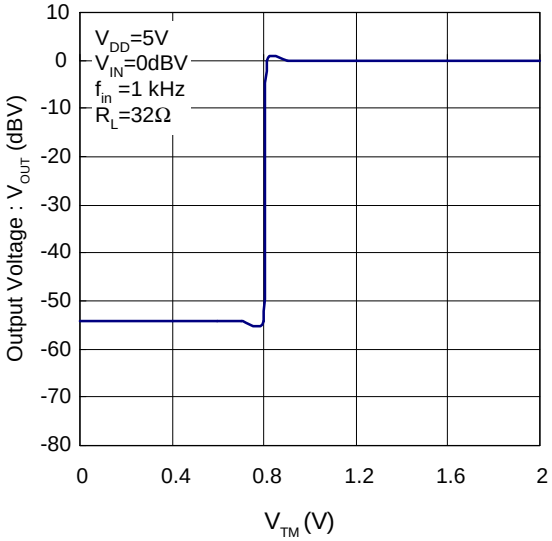
Supply Voltage



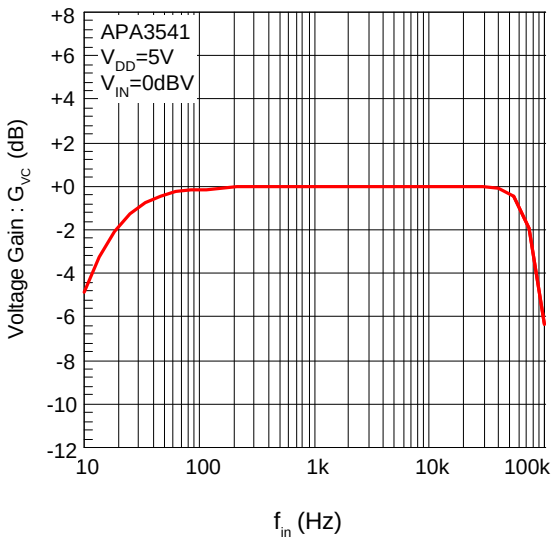
Supply Voltage



Mute Control Voltage

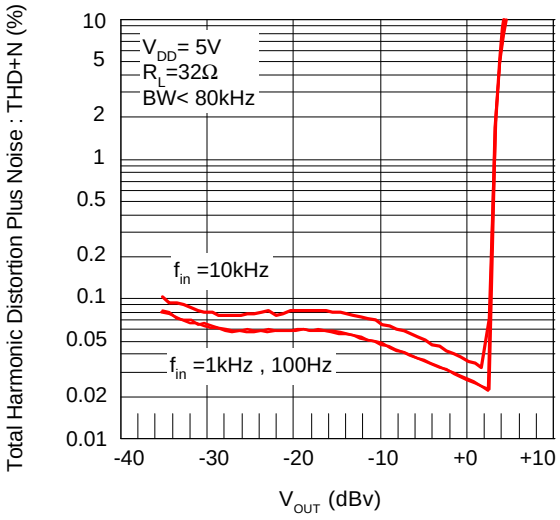


Frequency

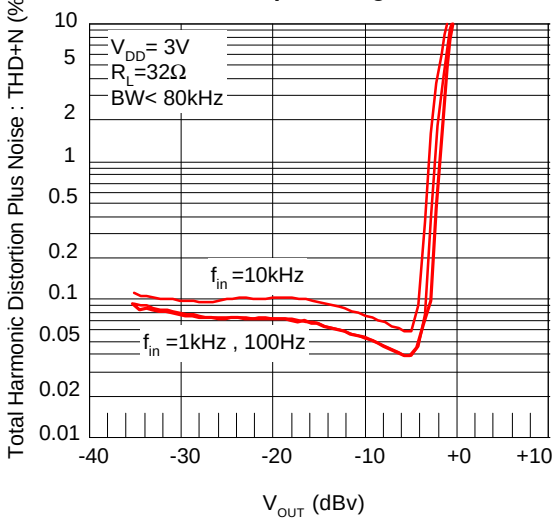


Typical Operating Characteristics (Cont.)

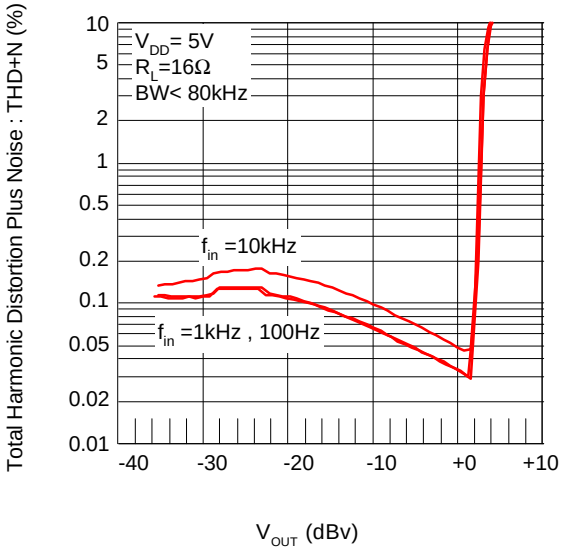
Output Voltage



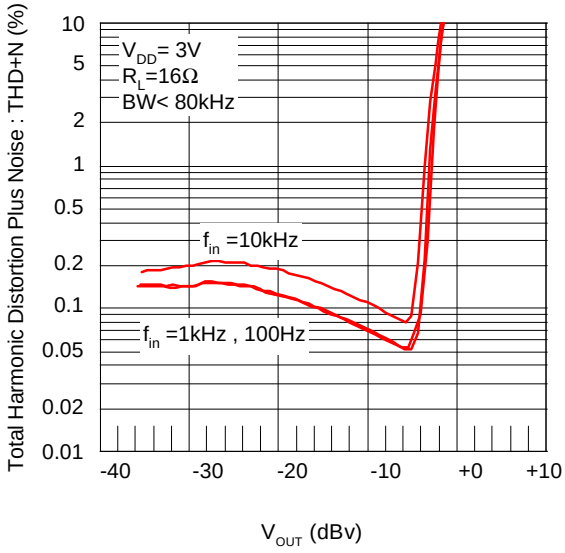
Output Voltage



Output Voltage

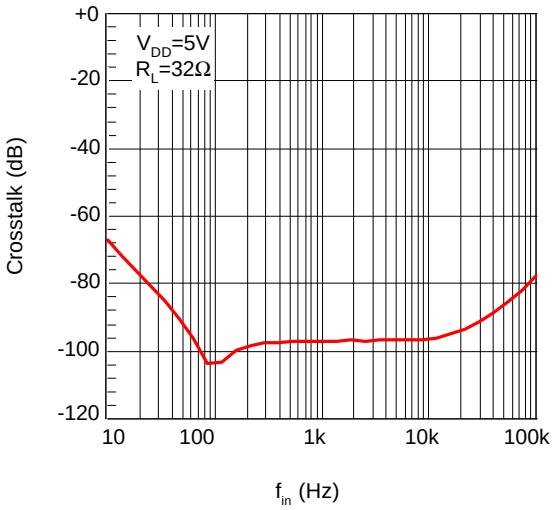


Output Voltage

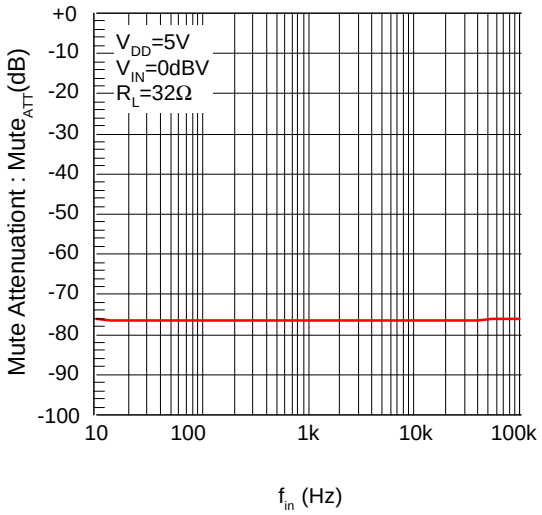


Typical Operating Characteristics (Cont.)

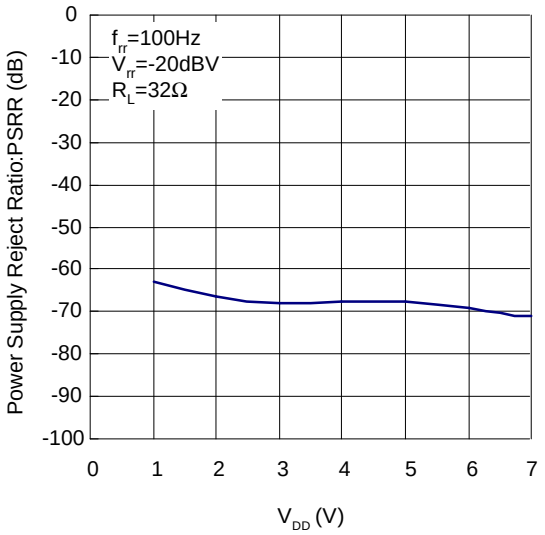
Frequency



Frequency



Supply Voltage



Application Information

Input Capacitor , C_i

In the typical application, an input capacitor, C_i, is required to allow the amplifier to bias the input signal to the proper DC level for optimum operation. In this case, the external capacitor C_i and the internal resistance R_i form a high-pass filter with the corner frequency are determined in the following equation:

$$f_C \text{ (highpass)} = 1/ (2\pi R_i C_i) \quad (1)$$

The value of C_i is important to consider as it directly affects the low frequency performance of the circuit. Consider the APA3541 where R_i is 180kΩ and APA3544 is 90kΩ internal fixed. Equation is reconfigured as below:

$$C_i = 1/(2\pi * 180k\Omega * f_C) \text{ for APA3541}$$
$$C_i = 1/(2\pi * 90k\Omega * f_C) \text{ for APA3544} \quad (2)$$

And the ceramic capacitor is recommended.

Bias Capacitor , C_B

As any power amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection. The capacitor location on both the bypass and power supply pins should be as close to the device as possible. The effect of a larger half supply bias capacitor is improved PSRR due to increased half-supply stability. Typical applications employ a 5V regulator with 10µF and a 0.1µF bias capacitors which aid in supply filtering.

This does not eliminate the need for bypassing the supply nodes of the APA3541/4. The selection of bias capacitors, especially C_B, is dependent upon desired PSRR requirements, click and pop performance. The capacitor is fed from a 95kΩ source inside the amplifier. To keep the start-up pop as low as possible, the relationship shown in equation should be maintained.

$$1/(C_B * 95k\Omega) \leq 1/\{C_i * R_i\} \quad (3)$$

As an example, consider a circuit where C_B is 4.7µF, C_i is 1µF and APA3541 R_i is 180kΩ. Inserting these values into the equation we get 2.24≤ 5.55 which satisfies the rule. Bias capacitor, C_B, values of 2.2µF to 10µF ceramic or tantalum low-ESR capacitors are recommended for the best THD and noise performance.

Output Coupling Capacitor, C_O

In the typical single-supply SE configuration, an output coupling capacitor (C_O) is required to block the DC bias at the output of the amplifier thus preventing DC currents in the load. As the input coupling capacitor, the output coupling capacitor and impedance of the load form a high-pass filter governed by the following equation.

$$f_C(\text{highpass}) = 1/(2\pi R_L C_O) \quad (4)$$

For example, a 220µF capacitor with an 32Ω speaker would attenuate low frequencies below 22Hz. The main disadvantage, from a performance standpoint, is the load impedance is typically small, which drives the low-frequency corner higher degrading the bass response. Large values of C_O are required to pass low frequencies into the load.

Optimizing Depop Circuitry

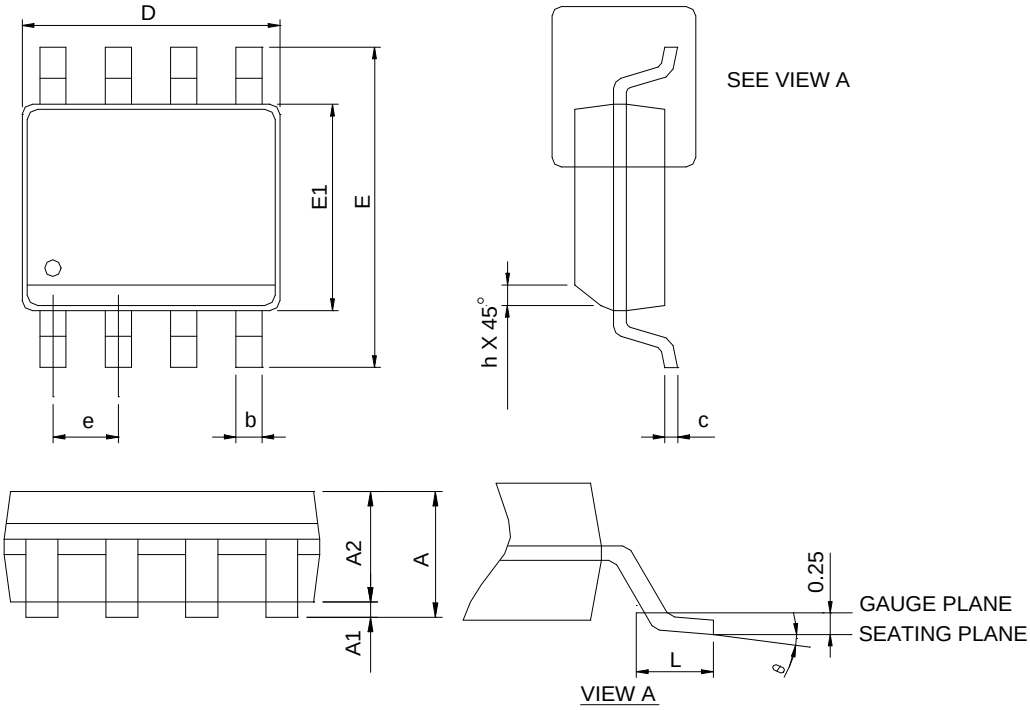
When the amplifier is in mute mode, both of the output stage and input bypass continues to be biased. Besides, no pop noise will be heard during the transition out of the mute mode.

Power Supply Decoupling, C_S

APA3541/4 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents the oscillations being caused by long lead length between the amplifier and the speaker. The optimum decoupling is achieved by using two different types of capacitors which target on different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1µF placed as close as possible to the device V_{DD} lead works best. For filtering lower-frequency noise signals, a large aluminum electrolytic capacitor of 10µF or greater placed near the audio power amplifier is recommended.

Package Information

SOP-8

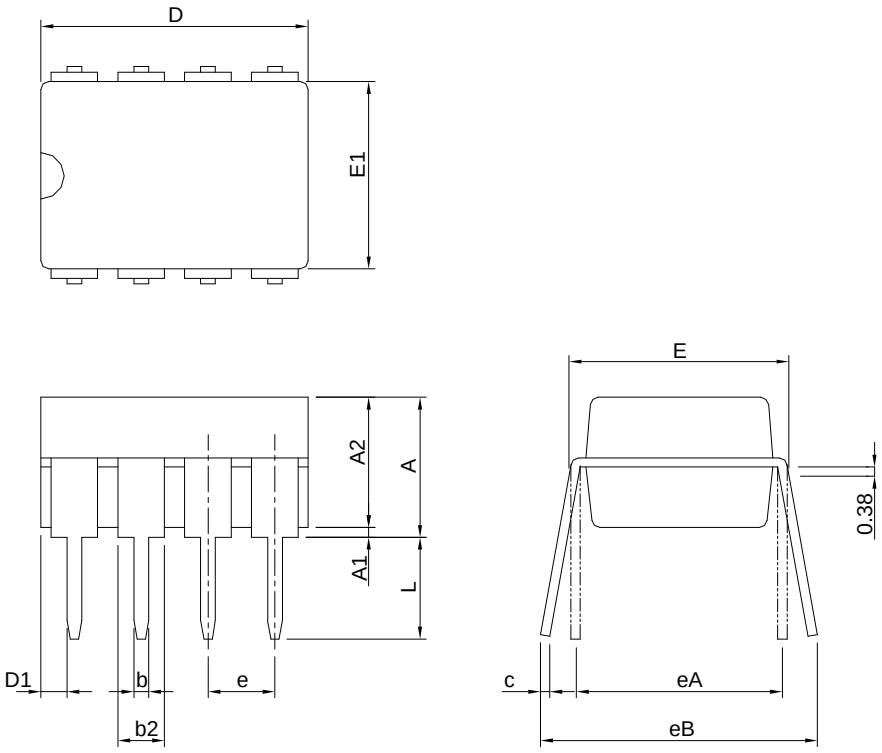


SYMBOL	SOP-8			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.75		0.069
A1	0.10	0.25	0.004	0.010
A2	1.25		0.049	
b	0.31	0.51	0.012	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
h	0.25	0.50	0.010	0.020
L	0.40	1.27	0.016	0.050
θ	0°	8°	0°	8°

Note: 1. Follow JEDEC MS-012 AA.
2. Dimension “D” does not include mold flash, protrusions or gate burrs.
Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.
3. Dimension “E” does not include inter-lead flash or protrusions.
Inter-lead flash and protrusions shall not exceed 10 mil per side.

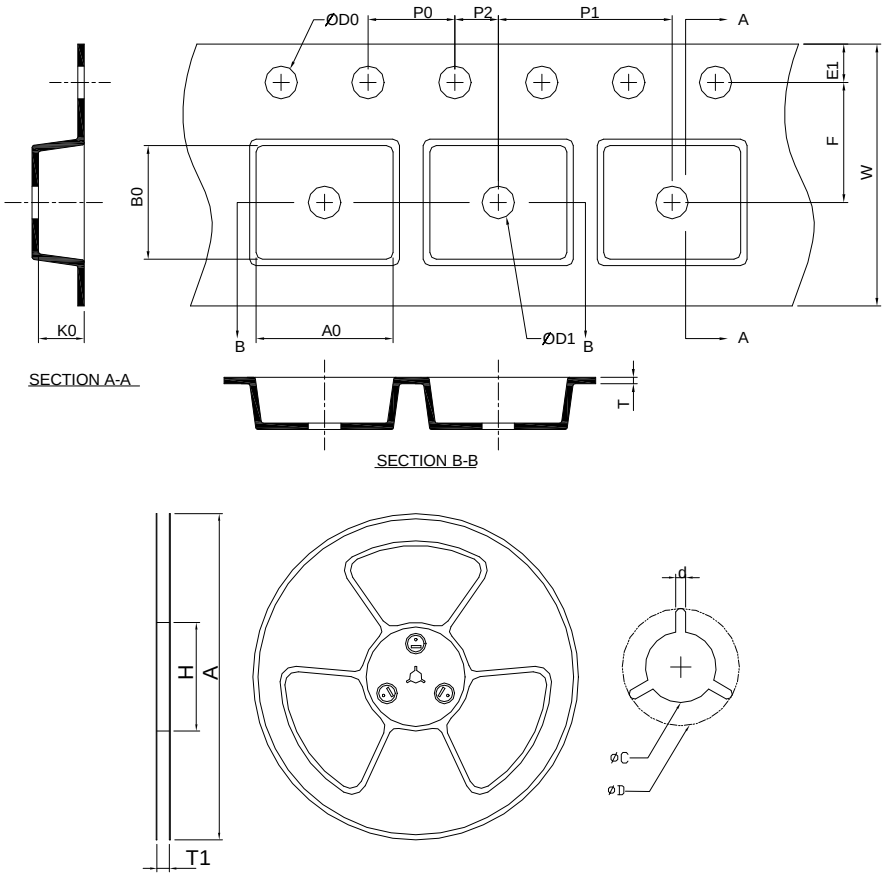
Package Information

DIP-8



SYMBOL	DIP-8			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		5.33		0.210
A1	0.38		0.015	
A2	2.92	4.95	0.115	0.195
b	0.36	0.56	0.014	0.022
b2	1.14	1.78	0.045	0.070
c	0.20	0.35	0.008	0.014
D	9.01	10.16	0.355	0.400
D1	0.13		0.005	
E	7.62	8.26	0.300	0.325
E1	6.10	7.11	0.240	0.280
e	2.54 BSC		0.100 BSC	
eA	7.62 BSC		0.300 BSC	
eB		10.92		0.430
L	2.92	3.81	0.115	0.150

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
SOP-8	330.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	6.40±0.20	5.20±0.20	2.10±0.20

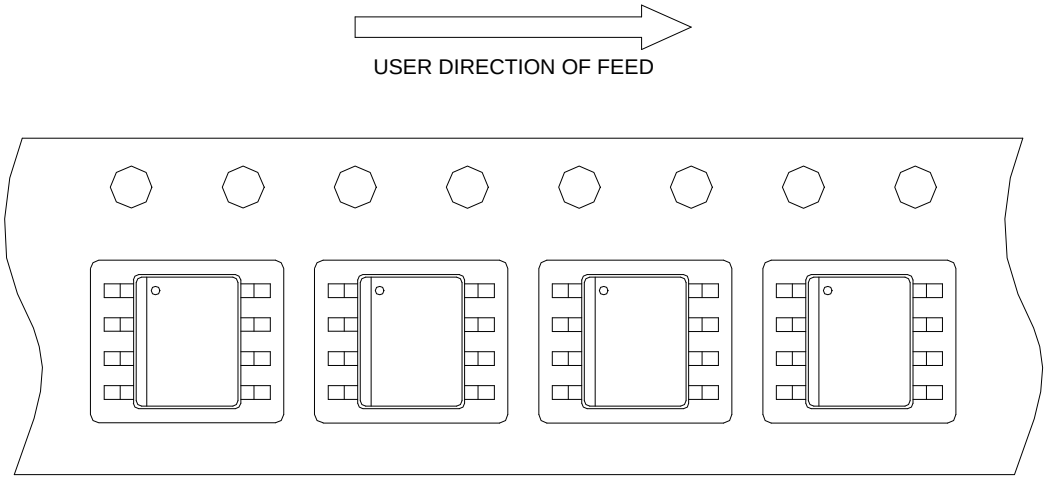
(mm)

Devices Per Unit

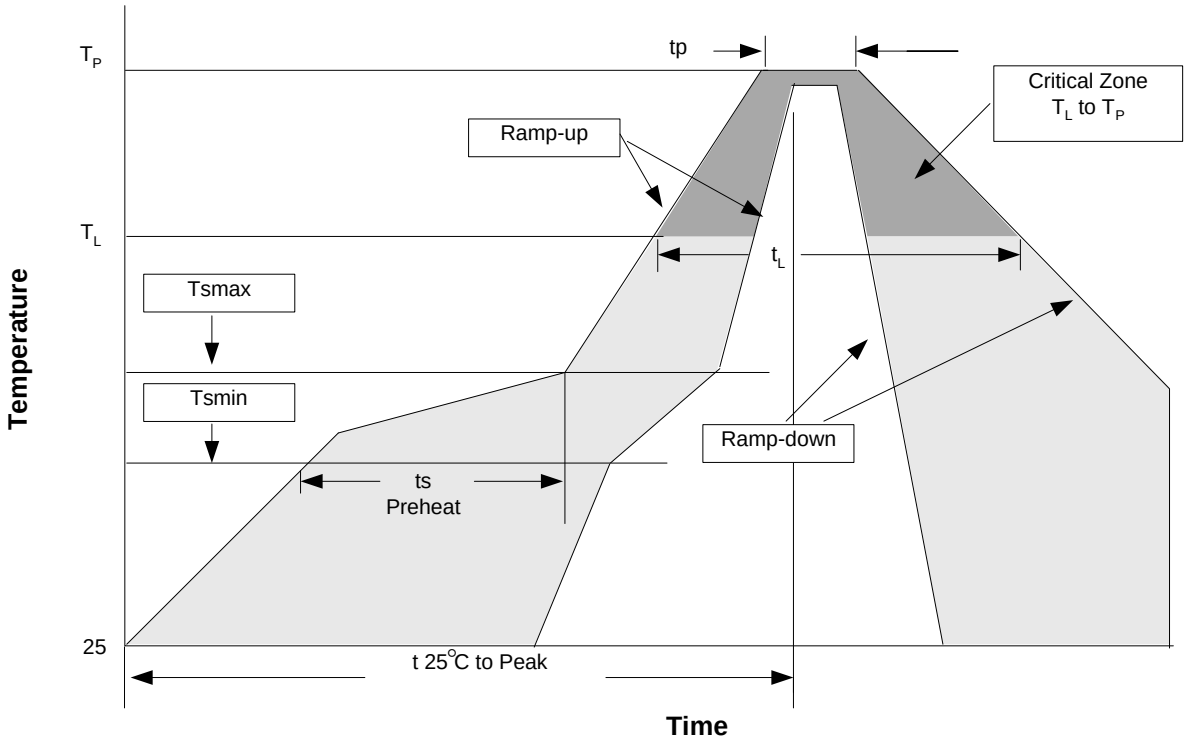
Package Type	Unit	Quantity
SOP-8	Tape & Reel	2500

Taping Direction Information

SOP-8



Reflow Condition (IR/Convection or VPR Reflow)



Reliability Test Program

Test item	Method	Description
SOLDERABILITY	MIL-STD-883D-2003	245°C, 5 sec
HOLT	MIL-STD-883D-1005.7	1000 Hrs Bias @125°C
PCT	JESD-22-B,A102	168 Hrs, 100%RH, 121°C
TST	MIL-STD-883D-1011.9	-65°C~150°C, 200 Cycles
ESD	MIL-STD-883D-3015.7	VHBM > 2KV, VMM > 200V
Latch-Up	JESD 78	10ms, 1_{tr} > 100mA

Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average ramp-up rate (T_L to T_P)	3°C/second max.	3°C/second max.
Preheat - Temperature Min (Tsmin) - Temperature Max (Tsmax) - Time (min to max) (ts)	100°C 150°C 60-120 seconds	150°C 200°C 60-180 seconds
Time maintained above: - Temperature (T_L) - Time (t_L)	183°C 60-150 seconds	217°C 60-150 seconds
Peak/Classification Temperature (Tp)	See table 1	See table 2
Time within 5°C of actual Peak Temperature (tp)	10-30 seconds	20-40 seconds
Ramp-down Rate	6°C/second max.	6°C/second max.
Time 25°C to Peak Temperature	6 minutes max.	8 minutes max.

Note: All temperatures refer to topside of the package. Measured on the body surface.

Table 1. SnPb Eutectic Process – Package Peak Reflow Temperatures

Package Thickness	Volume mm^3 <350	Volume mm^3 ³350
<2.5 mm	240 +0/-5°C	225 +0/-5°C
≥2.5 mm	225 +0/-5°C	225 +0/-5°C

Table 2. Pb-free Process – Package Classification Reflow Temperatures

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 +0°C*	260 +0°C*	260 +0°C*
1.6 mm – 2.5 mm	260 +0°C*	250 +0°C*	245 +0°C*
≥2.5 mm	250 +0°C*	245 +0°C*	245 +0°C*

* Tolerance: The device manufacturer/supplier **shall** assure process compatibility up to and including the stated classification temperature (this means Peak reflow temperature +0°C. For example 260°C+0°C) at the rated MSL level.

Customer Service

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