Audio power amplifier frequency compensation:

Is PLIL an Alternative to the Miller Capacitor?

A lot of audio amplifiers, from around 40 years ago right up to today, use the Miller capacitor. An inherent problem with this is that it delays the output voltage response and thus the negative feedback to the input stage. John N. Ellis, B.Sc., Ph.D. thinks he may have an alternative.

The transistor audio amplifier can be generalised as having an input stage, which may be a single transistor or differential pair, a voltage amplifying stage (VAS), a driver pair and an output pair as shown in Fig. 1. As there are more than two time constants encompassed by the feedback loop, negative feedback can cause instability that requires frequency compensation to put right. A common method to stabilise amplifiers is to use a "Miller" capacitor Ccomp, as this causes a monotonic roll-off at 6dB/octave, which is, as Nyquist, Bode and others have shown, stable.

Many audio amplifiers, ranging from the decidedly mediocre (typically from the 60's and 70's) to good ones from the 90's[1], use the Miller capacitor. An inherent problem with the Miller capacitor is that it delays the output voltage response and thus the negative feedback to the input stage. If the input signal is fast enough, this will cause transient distortion due to overloading in the input stage, until such time as the feedback "catches up" with it. The problem can be eliminated by using resistors in series with the input transistor emitters which are large enough to prevent overloading in the input stage, or using moderate resistors and increasing the current in the input stage to achieve the same voltage margin, such that the input

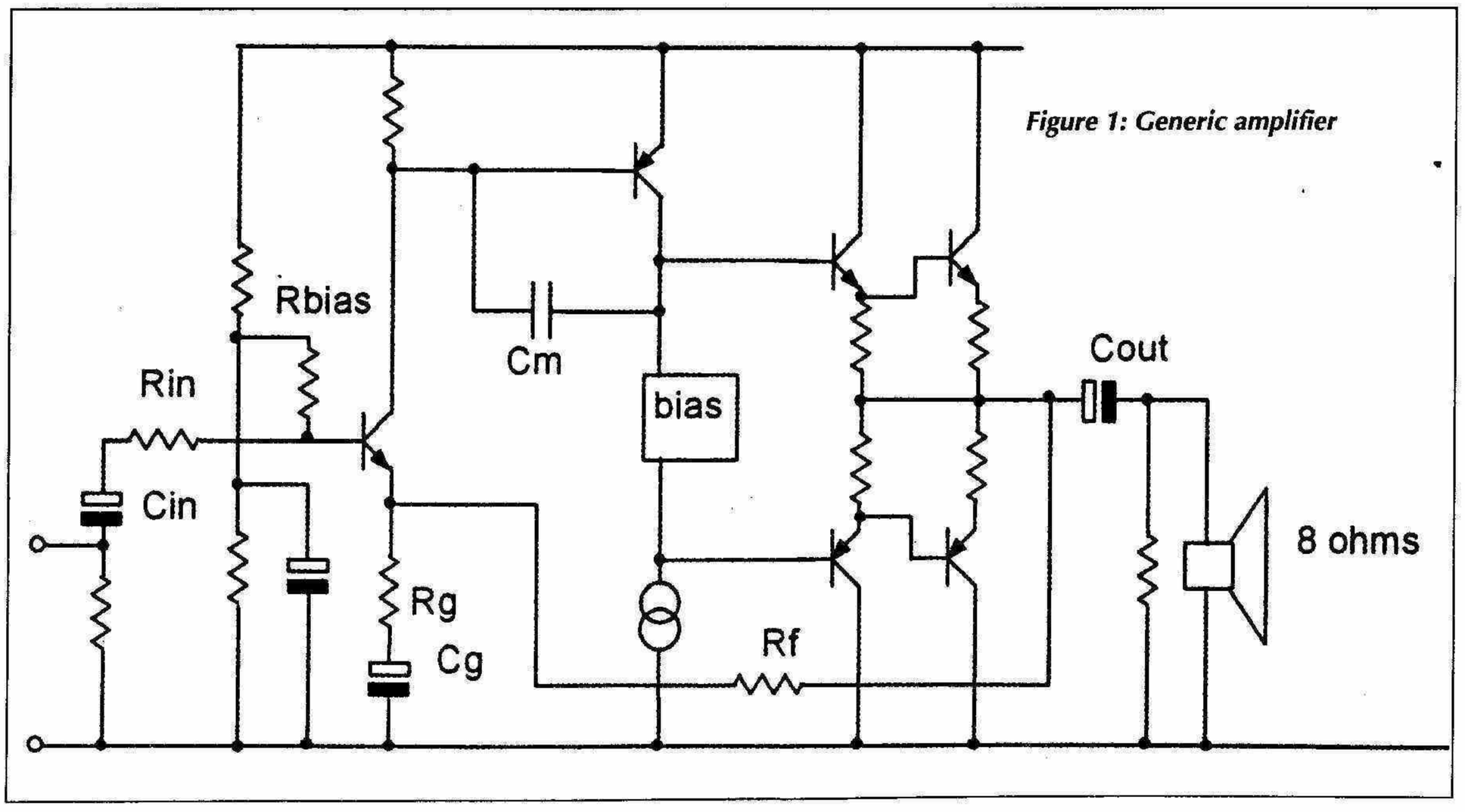


Figure 1: Generic amplifier

transistors do not cut off for any input within normal limits. This approach to "fast slew" was exploited by Stochino[2]. I hasten to add that for ref. 1, transient distortion from slewing does not arise for normal audio-band signals usually taken to be 20kHz maximum, as it has a good margin to at least to 150kHz. Nevertheless, the potential for input stage overload is not desirable, and the Miller capacitor method of compensation is not one which I would use by preference. However, the search for an alternative is not easy but phase lead compensation with input lag (PLIL) seems to be a possibility. This article reports on the investigations I have undertaken in the PLIL approach.

The use of a phase lag capacitor on the input stage of the amplifier was first suggested by Otala[3] to prevent transient intermodulation distortion. Since then, there has been much debate about whether "transient intermodulation distortion" is the right term for such distortion products (intermodulation implies continuous frequency spectra) that are transient in nature. Today it is usually accepted that control of slewing is the important point.

Several authors have compensated their amplifiers by a capacitor Ccomp connected between the collector of the VAS transistor to the feedback point FB, as shown in outline in **Fig. 2,** the so-called phase-lead method. The first author who caught my attention with this approach was Bailey[4]. Linsley-Hood also used this method[5], as did Gibbs and Shaw[6], who also included an input phase lag capacitor, and is perhaps the first example of phase-lead, input lag.

I found that when a phase-lead capacitor was used by itself, it was not reliably stable. I tested a version of Bailey's amplifier which used a small-signal PNP input transistor and NPN VAS. The original circuit used a 40361 medium-power NPN transistor in the input stage and a 40362 PNP VAS. In my circuit, using a medium power PNP input transistor (actually a 2N4036), I found that the amplifier was stable only when I increased the series input resistor to 4.7kΩ. When a small signal transistor was used, the amplifier was once more unstable.

To shed some light on the instability using phase lead compensation alone I simulated a four-stage equivalent circuit to represent the generic amplifier, **Fig. 3a.** The stages represented the input, VAS, driver and output transistors. Each transistor stage (treating the driver and output as singles) was modelled by a simple p-type equivalent circuit comprising an input impedance, base-emitter capacitance, collector-base capacitance and mutual conductance as shown in **Fig. 3b.**

To simulate Bailey's amplifier, I had to devise p-type model parameters for the 40361 and 40362, neither of which I had and are, it seems, obsolete, RCA having been taken over nearly 15 years ago now. The parameters I used were based on measured capacitance data for devices 2N2102 and 2N4036, plus estimated diffusion capacitance and gm parameters. SPICE data from some manufacturers, available on the internet, give rather better values than I suspect the original RCA transistors would have had. I also had to estimate the data for the Motorola MJ481 and MJ491 power transistors which are also past their sell-by date. The collector-base capacitance (Ccb or Cob) is in the data sheet, but other parameters were estimated from larger transistors and adjusted for the lower current handling of the MJ481/MJ491. **Table 1** gives my guesstimated data for interested readers. The rather low gm figures for the power device represents near-cut off values for a class B amplifier. Clearly there is scope for a wide range of parameters in the output stage: it is not possible to model a Class B (a large signal configuration) amplifier using small signals and expect it to be correct for all conditions. This could of course point to where the last vestige of amplifier design remains to be uncovered: the dynamic performance of transistors in a large-signal amplifier. In this case, I was seeking to reveal the basic properties of the compensation method.

In the above table, Cbt refers to the total base capacitance that is a sum of the depletion and diffusion parts.

Fig. 4(a) shows the rather awful-looking frequency response. Immediately one would conclude that this design is not stable. In the critical 1 to 10MHz region, the unity-

Table 1: p-model data for the "Bailey" amplifier

transistor	hie (ohms)	Cbt (F)	Ccb (F)	gm (mA/V)
40361 (input)	880	260p	4p	.064
40362 (VAS)	100	510p	16p	0.4
40361 (driver)	210	340p	10p	0.2
MJ481 (output)	40	25n	250p	1.4
BC307B (alt. i/p)	4000	70p	1.5p	.064

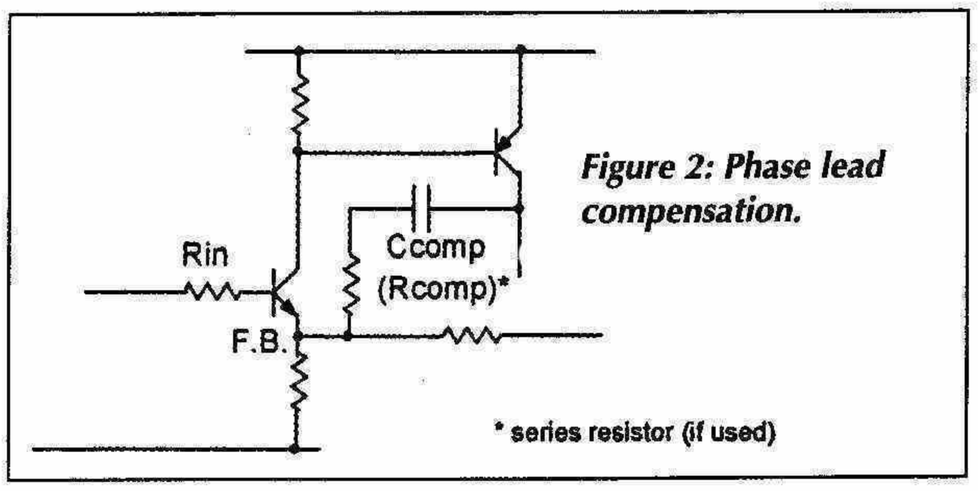


Figure 2: Phase lead compensation.

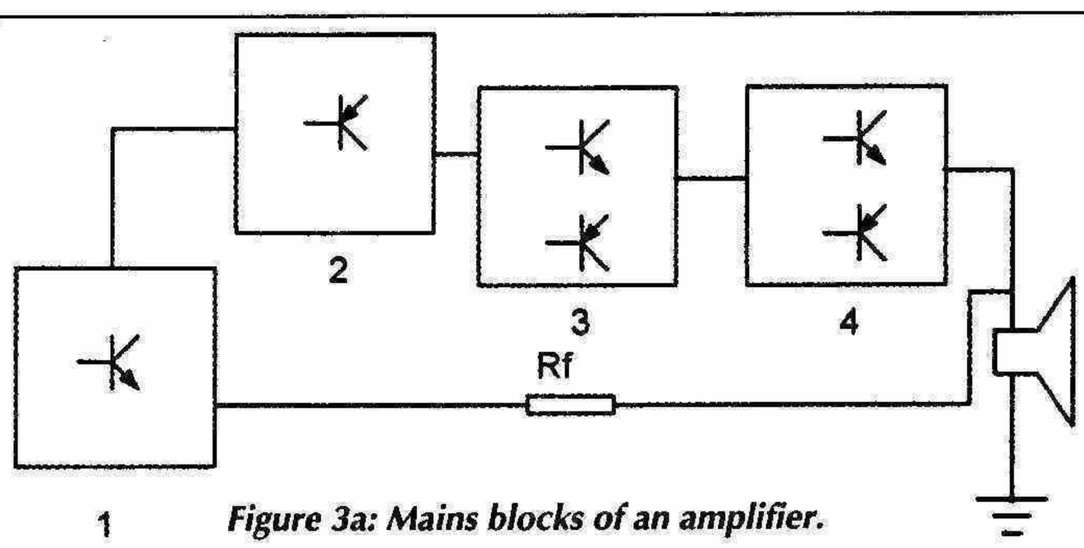


Figure 3a: Mains blocks of an amplifier.

1 - input stage; 2 - voltage amplifier;
3 - driver(s); 4 - output(s)

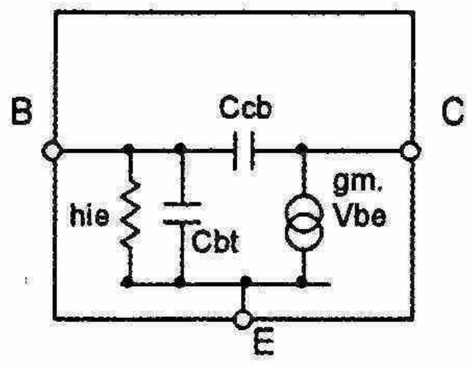


Figure 3b. π-type equivalent circuit

Fig. 3 (b)
π -type Equivalent Circuit

Cbt = total base (diffusion + depletion) capacitance
Ccb= collector-base depletion capacitance
hie = input impedance
gm = mutual conductance

gain frequency point has not been achieved cleanly and the phase shift is undergoing some rather alarming changes. (The straight-line jump is not real: it is an artefact of the simulation returning the phase angle between the limits of +/- p. The top arc continues the lower phase shift in practice – but at least this acts as a 180° marker). I increased the input resistance to 10kΩ, and the response is shown in **Fig. 4(b).** This is stable, just, as the unity gain point is not quite 12dB/octave and the phase at unity gain is below 180. Substituting a small-signal transistor equivalent circuit, also listed in table 1, for Tr1, gave the response shown in **Fig. 4(c)** while retaining the 10kΩ input resistor. This is marginally unstable. While I am happy to accept that my models are somewhat simplistic, and the parameters guesstimates, the results confirm my experimental observations. In practice, Bailey's design may well have been stable with the original components but larger input resistors may have been necessary in some cases. Evidently it required the frequency response of the input transistor to have designed-in limitations. Using a 40361 may have been judicial!

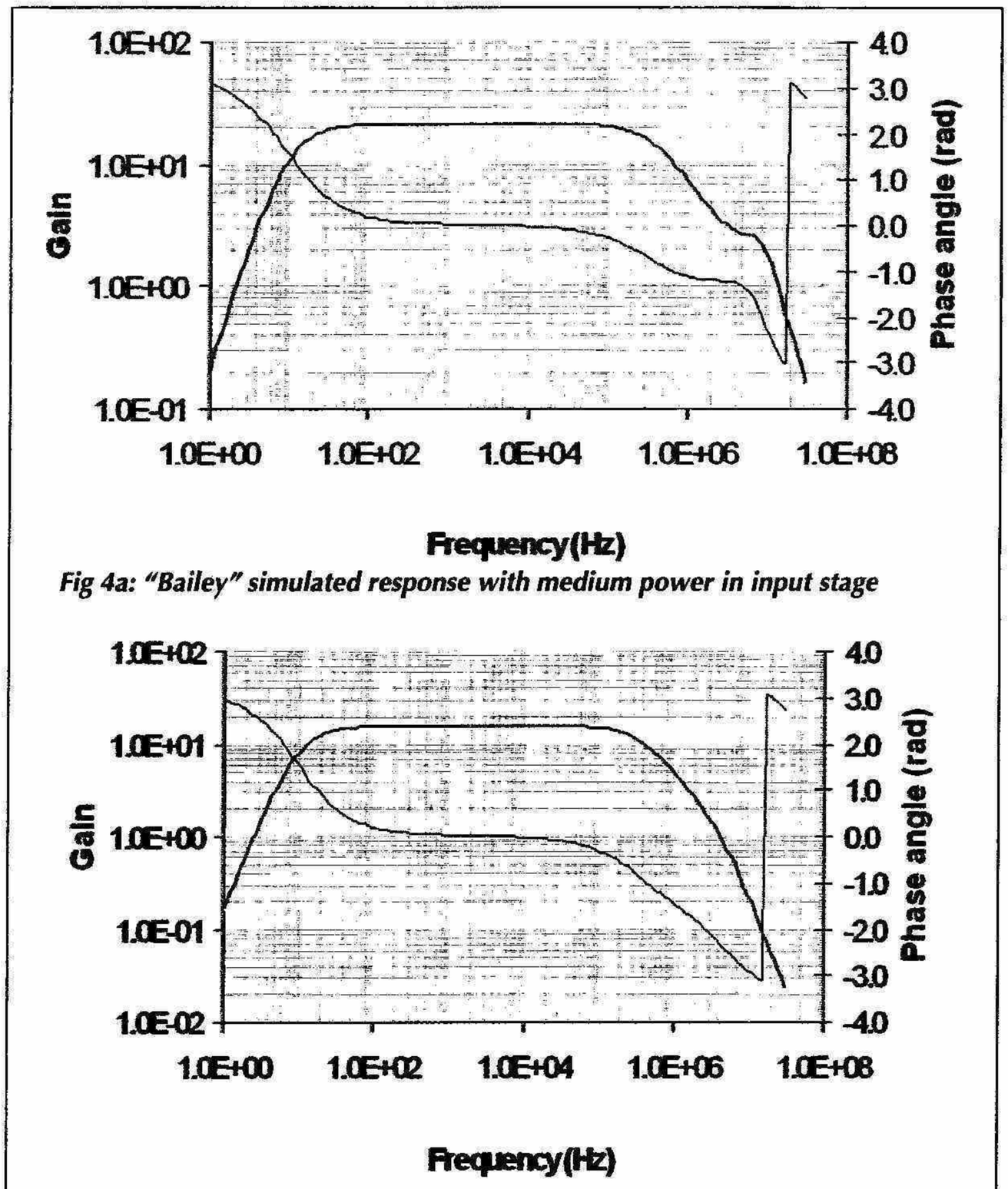


Fig 4a: "Bailey" simulated response with medium power in input stage

Fig 4b: With 10kΩ instead of 1.5kΩ

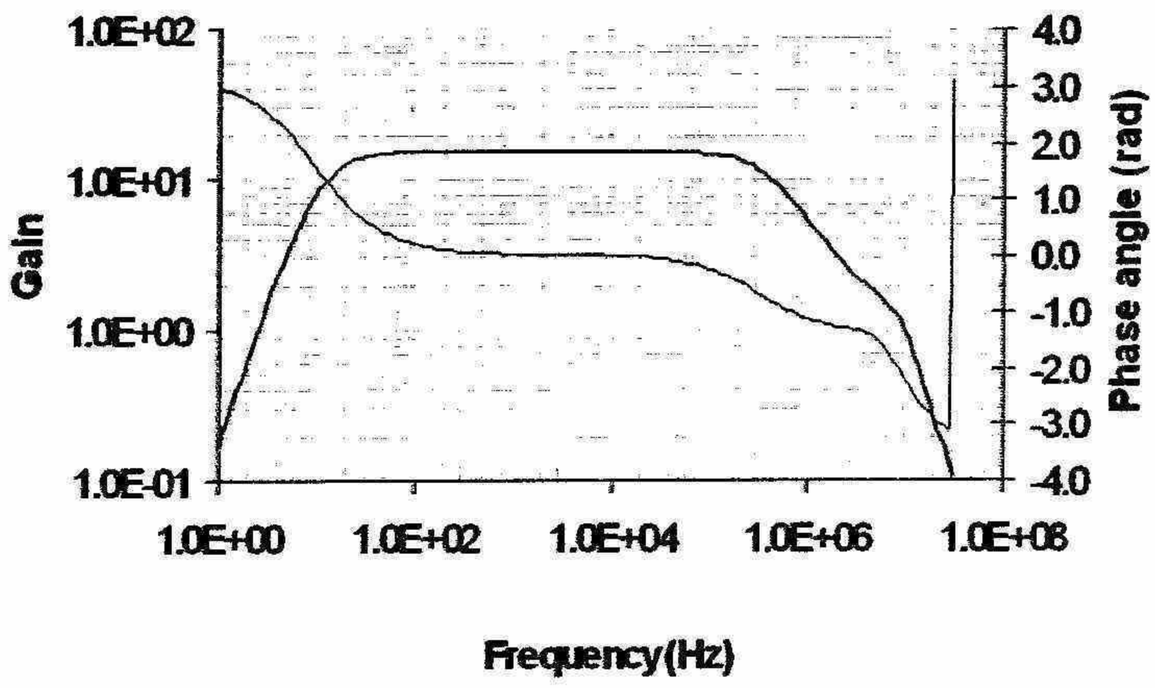
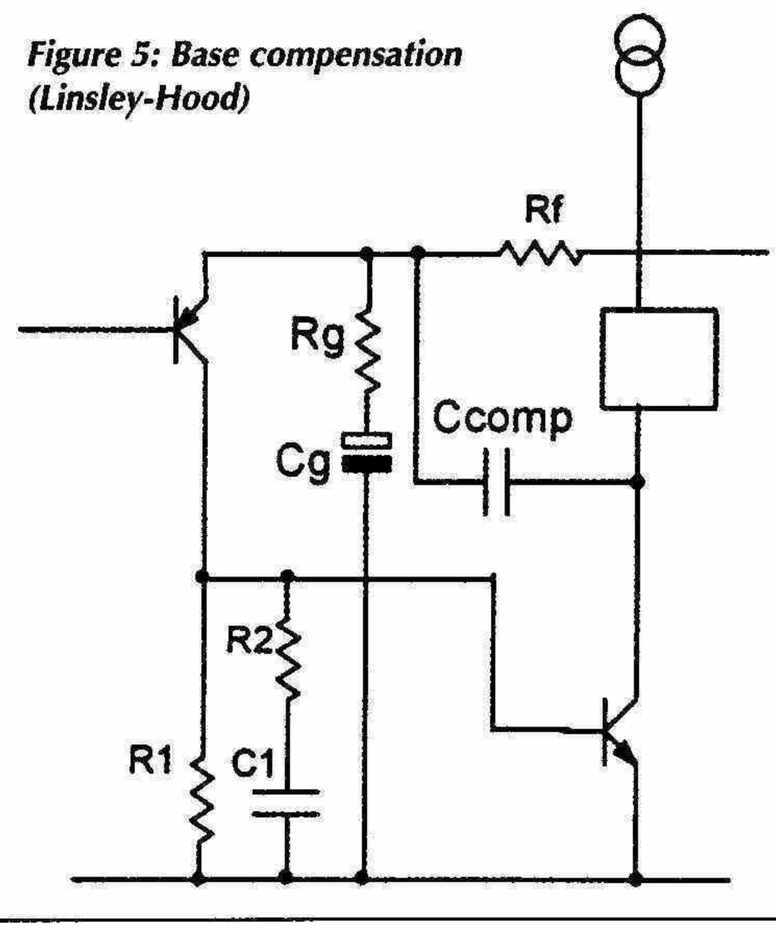


Fig 4c: With 10kΩ and small signal transistor in input stage

Astute readers will immediately point out that the use of a resistor-capacitor network, as Bailey described (op. cit.), should in theory never give a unity-gain response. Indeed, the concept seems flawed because the gain cannot even approach unity, until such time as the amplifier open loop runs out of steam. This is where the phase-lag (Miller) method appears superior in that it has a monotonic characteristic – the gain continues to fall throughout the whole frequency spectrum.

Linsley-Hood also appears to have found that the phase-lead capacitor was insufficient by itself when higher frequency input transistors are used because in his amplifier (op. cit), he used an additional resistor-capacitor pair generating a phase-lag across the base of the VAS transistor (e.g. **Fig. 5**). Evidently, this will give rise to a

Figure 5: Base compensation (Linsley-Hood)



reduction in gain which falls monotonically (until the series resistor limits it at least) and would provide the desired improvement in stability. In my view, this is as bad as using a Miller capacitor as it does nothing for the input transistor, and would also lead to transient distortion at high frequencies. Linsley-Hood, and Gibbs and Shaw (op. cit.) both avoided using the resistor, Rcomp in Fig. 2, which Bailey had specified in series with the compensation capacitor. This at least allows the gain to be able to become closer to unity than with it. **Fig. 6** shows the response for a 470pF compensation capacitor with no series resistor. The unity gain point hovers tantalisingly around the critical frequency point, but refuses to dip below unity until the amplifier open loop limit sets in. This is just not stable enough and in practice it may be very dependent on transistor parameters.

I simulated the PLIL approach and after several variations, I found the optimum network for the single-

ended input stage required: (i) a small resistor in series with the input phase-lag capacitor; (ii) a resistor in series with the input lead; and (iii), a small resistor in series with the emitter of the PNP input transistor as shown in **Fig. 7(a).** The response for a circuit with the components given is shown in **Fig. 7(b).** This time, the response is virtually ideal, with a monotonic decrease until well beyond the critical phase-shift point. This method of input lag with phase lead compensation is along the lines that Otala[3] recommended, but does not require extensive local feedback.

I checked the stability of this method firstly by considering the input phase-lag capacitor only in a simulation **(Fig. 8).** The graph shows a second-order roll-off initially, but there is a relaxation towards a single-pole slope near the unity gain point, conveniently. The circuit seems to share some similarity with a Colpitts type

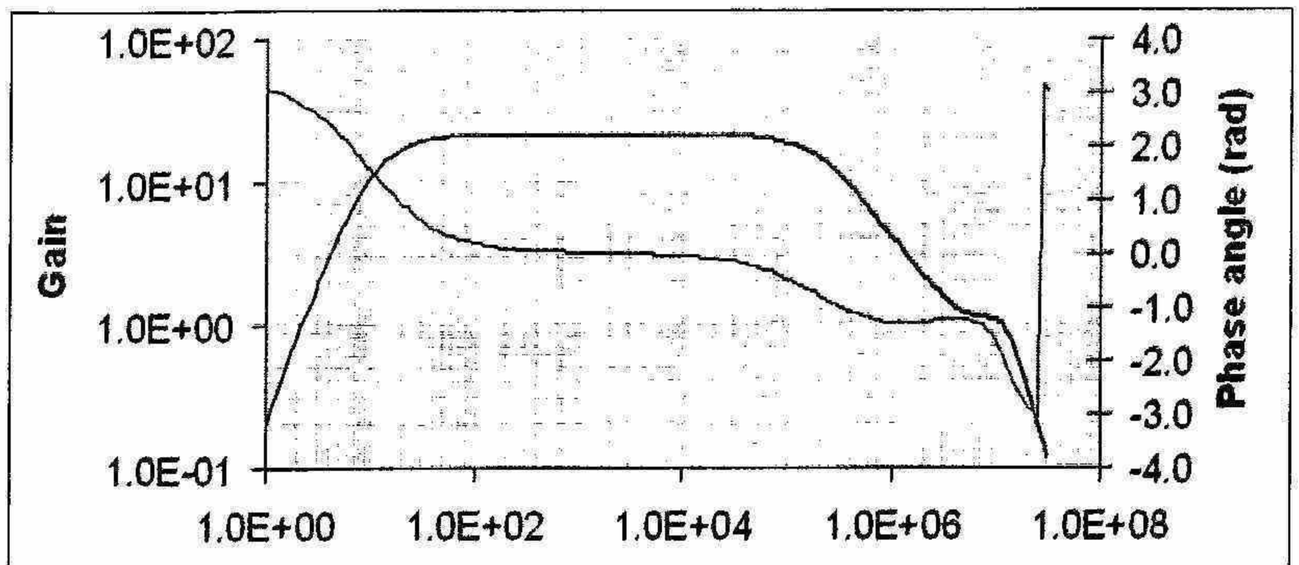
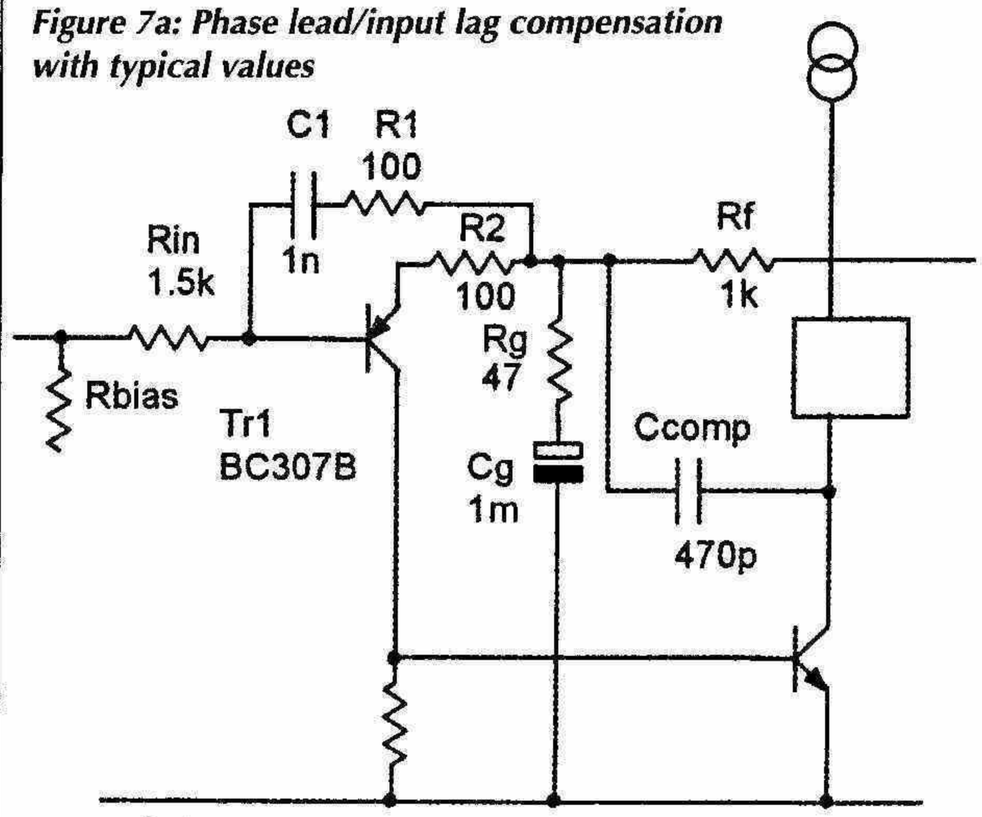


Fig 6: Simulation of "Bailey" amplifier without series compensation resistor

Figure 7a: Phase lead/input lag compensation with typical values



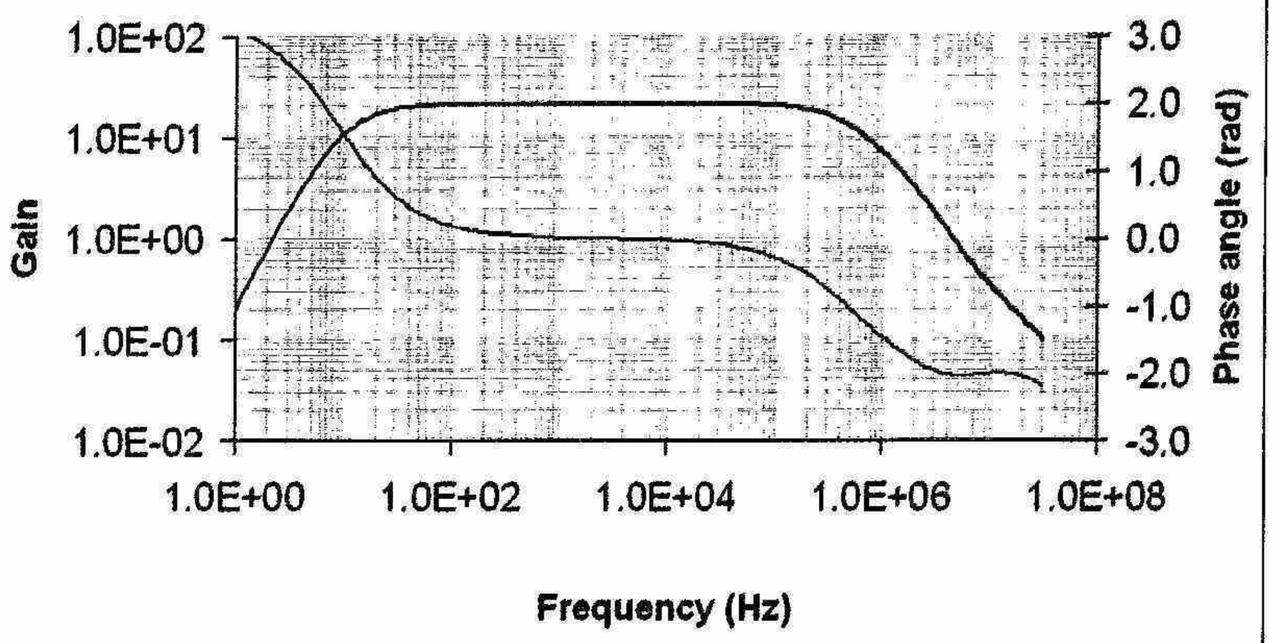


Fig 7(b): Response of "Bailey" amplifier simulation with phase lead/input lag compensation

oscillator, or a second-order filter **(Figs. 9(a) and (b)**. In fact, the second-order roll-off is damped by the series resistors, and is compensated by using the phase-lead network in conjunction with this phase-lag circuit. The input capacitor-resistor network, then, is capable of providing the required monotonic control of gain at high frequencies where the phase-lead capacitor rolls to unity. But the network is definitely NOT a replacement for the phase-lead capacitor, nor for the phase-lag Miller type. The method requires both phase lead and input (phase) lag together to operate correctly.

There are two advantages of the PLIL compensation method. For one, it eliminates the Miller capacitor. Instead of burdening the input stage at higher frequencies, the phase-lead capacitor provides a signal which tries to balance the feedback side of the input stage. Measurements have confirmed the simulations in a differential version of the amplifier where the base to base voltage at 20V and 20kHz output is only about 2mV compared with the 25mV or so for the Miller compensated amplifier. This has to be kinder to the transistors than forcing them into a larger signal mode than necessary. Even a degenerated input pair will experience a reduction in non-linearity from about 0.1% to 0.02%. A fast square-wave applied to the Miller-compensated amplifier shows an alarming peak of 600mV on the base-to-base differential, **Fig. 10** while PLIL compensation eliminates this spike almost completely as in **Fig. 11(b).**

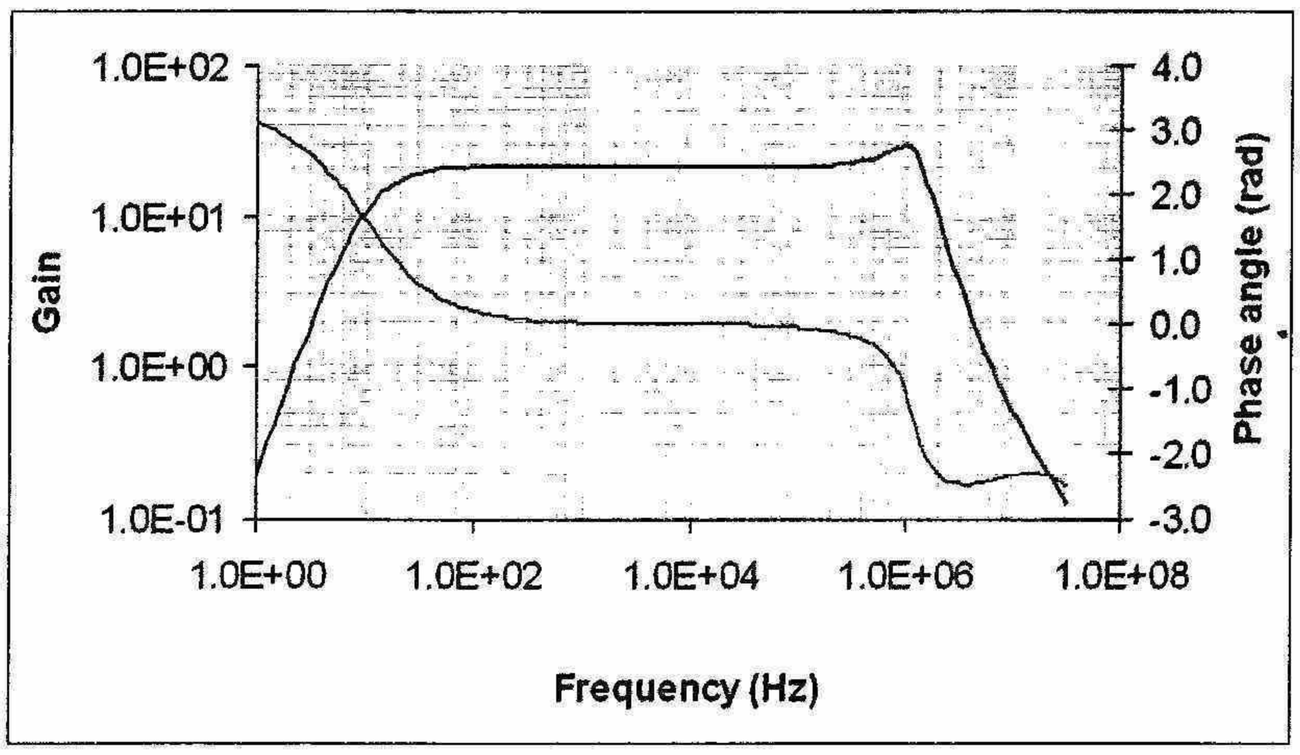


Fig 8: Simulation of input phase-lag compensation alone

The second advantage is that because the input phase-lag network has a second-order rate of climb, the loop gain is not going to be seriously impacted. This means that the distortion should be about the same as in the phase-lag compensation circuit, unlike the use of an input RC filter, **Fig. 11,** about which there has been some criticism[8], and I accept is a heavy-handed approach to avoiding transient distortion.

The time-constant of the input phase-lag network should be chosen to be around the same as or a little higher than

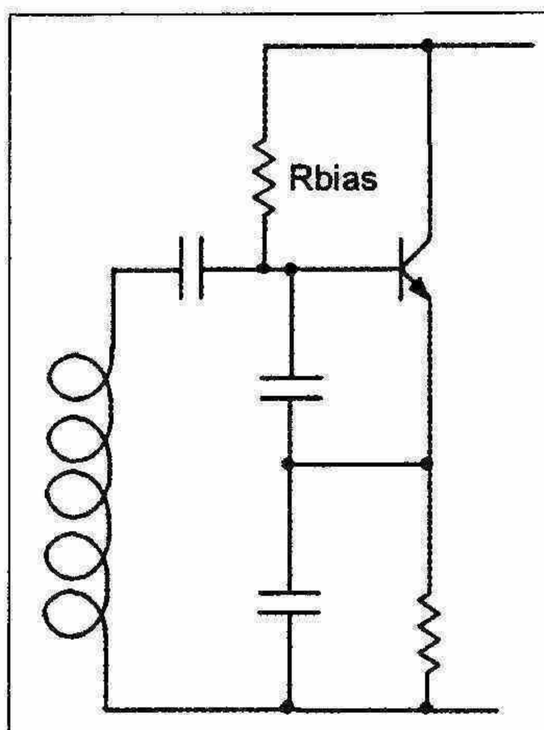


Figure 9a: Colpitts oscillator.

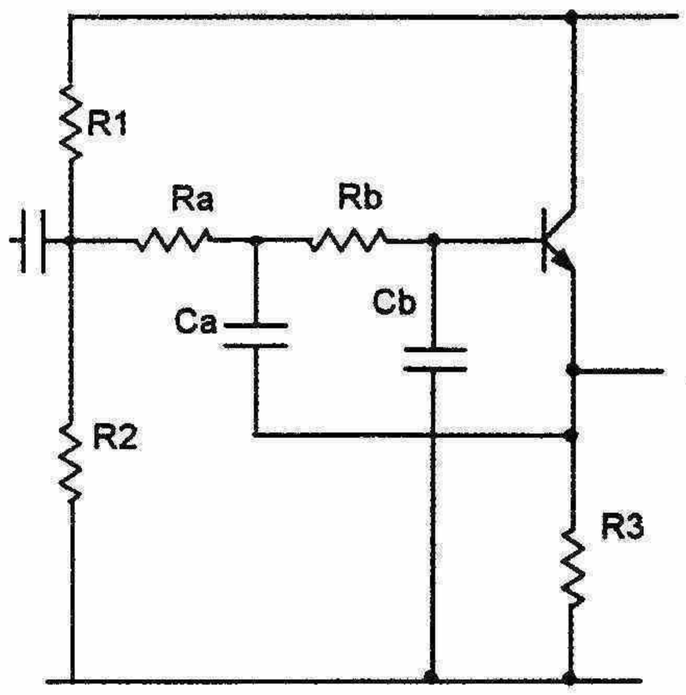


Figure 9b: Two-pole filter.

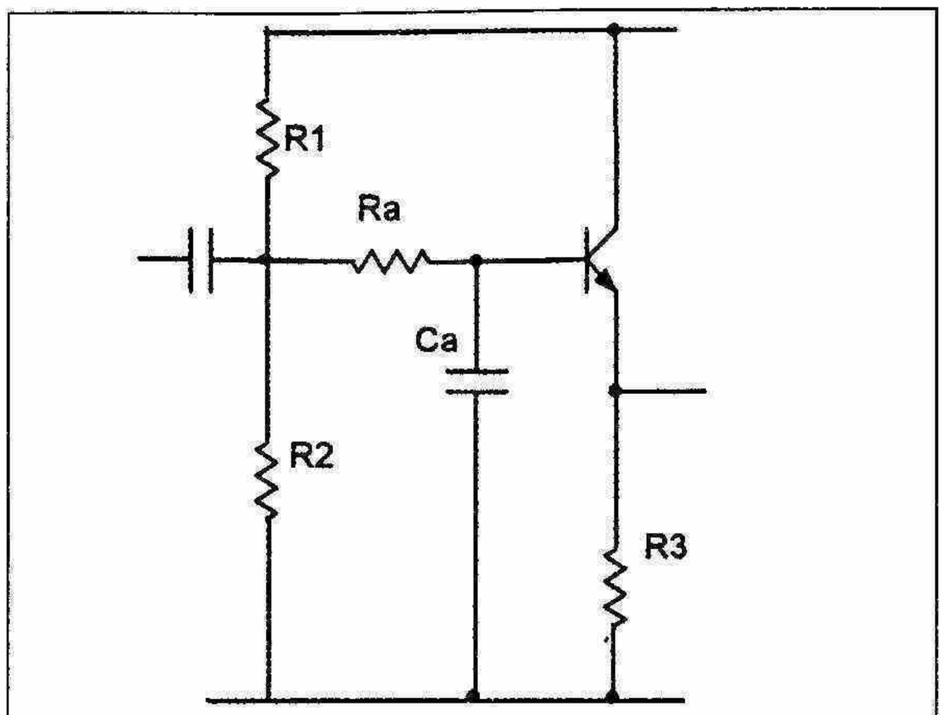
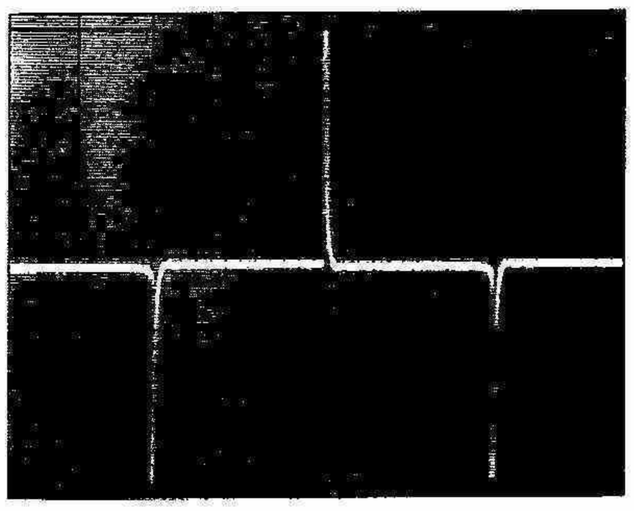


Figure 11: Simple input filter



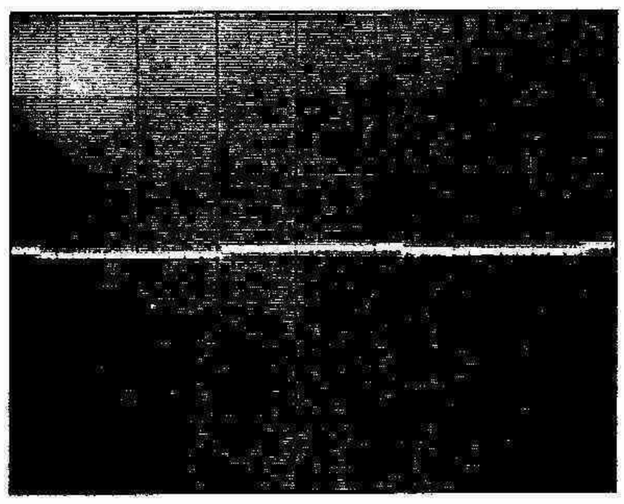


Fig 10(a): Differential signal (base to base) for Miller compensated amplifier in response to a 10kHz square wave signal
Fig 10(b): Differential signal for a PLIL compensated amplifier for same input (vert 200mV/div, hor 20µS/div)

the amplifier closed-loop roll off as set by the phase-lead capacitor and feedback resistor. In a test amplifier shown in **Fig. 12,** which is based on Self's "blameless" design (op.cit), the compensation capacitor operates with the feedback resistor to give about 150kHz closed-loop cut-off. I have chosen a slightly higher overall gain of 30 rather than 20.

As a resistor is required in series with the base lead of the input stage to ensure that the additional phase-lag capacitor does not give rise to oscillation, the noise level will be higher than without. The noise voltage I measured was under 1mV, rms, or about 100dB down from

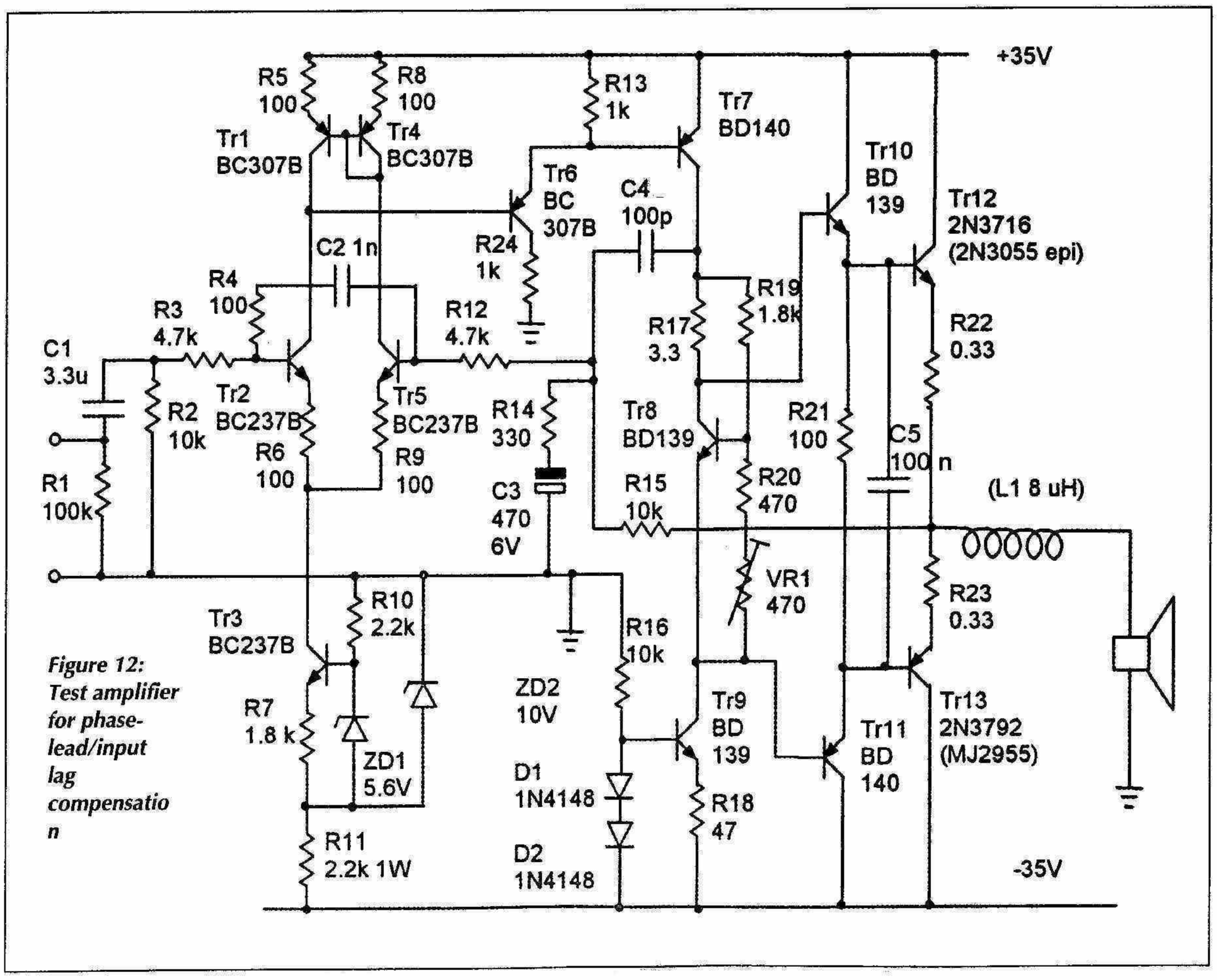


Figure 12: Test amplifier for phase-lead/input lag compensation

maximum output, and still quite acceptable.

On the question of distortion, I attempted to measure the performance but I have to say that the oscillator I used for distortion measurements was not ideal. It had more second and third harmonic distortion than the amplifier and to make any readings at all I had to subtract the reference input from the output at all frequencies, rather error-prone and troublesome.

At 1kHz and 1V RMS output, corresponding to 125mW into an 8Ω load, I could not see any additional harmonic components from the noise, setting the limit at around 0.01%, within my experimental limits. The same was true at 10kHz. At 10V RMS output, 12.5W, the distortion components were found to be largely odd harmonics, and around 1mV. Adding the fourth to ninth at 10kHz, (the odd harmonics being indicative of residual crossover distortion) the total distortion was 5mV rms giving a maximum total harmonic distortion of 0.05%. There may have been some distortion components higher than 100kHz but the analyser I used was unable to record them, and the 9th harmonic was at least smaller than the 7th. At 10V, 1kHz, the high frequency components vanished after the 6th.

Thus, it seems that, for a steady-state signal, the input-lag and phase-lead compensation method gives a distortion below 0.05% at 10kHz and 10V RMS, and considerably lower at lower frequencies, within the limitations of my experimental tests. In a short burst at 30W, before my load resistor overheated, I measured the same ratio of distortion components as at 10V. With the absence of input transient overload distortion, this approach seems to have some advantages over the Miller compensation method.

To provide a sanity check on the distortion levels, I compared the simulated open loop gains of the two methods. **Fig. 13** shows the graphs. It has to be said that the phase-lead-input lag approach does suffer a little. Curve 1 is for the Miller-compensated, modelled amplifier; curve 2 is the modelled stable PLIL amplifier and curve 3 is based on real component values required in a practical amplifier. At 1kHz the gain is down about a factor of two compared with the phase-lag (Miller) circuit, with the parameters I used. If the reference amplifier is under 0.001% at 1kHz, this leaves the phase-lead/lag design at under 0.002%. Thus, it seems that while the approach may increase noise and distortion, it is by a very small margin. There is however, some additional increase at the top end, where the components required in an actual circuit were rather greater than the model prediction. Thus, is appears that the PLIL method may need some optimisation for best performance. It may be concluded that while audible distortions are controlled, high frequency distortions may be less so.

In testing this configuration for stability during clipping, the amplifier showed a very fast recovery when coming out of clipping. Initially, it oscillated alarmingly but this was found to be due to the protection circuitry, which I removed, and the emitter resistors, which I will return to. Although the recovery from clipping was then found not to cause oscillation, I nevertheless considered that the amplifier gain should be reduced, passively, during clipping. It was easy to add the standard anti-saturation diodes, following Stochino, to the upper (VAS) stage because the additional transistor in front of the BD140 lends itself to this. The current source in the lower arm required an extra three diodes **(Fig. 14).** The result was that the amplifier gain is killed in the pre-driver stages rather than in the driver and output stages, and the clipping signal is "soft". Recovery with this approach is well controlled, as shown in **Fig. 15.** This was measured with a reduced power supply voltage and including a pair of filter chokes to prevent mains ripple appearing on the clipped signal.

I further checked the stability by using the proverbial 2.2mF capacitor load on the output. On testing with a 10kHz square wave the amplifier showed classic ringing **(Fig. 16),** after I had added further power supply decoupling on the amplifier rails. For continuous operation on a capacitive load, the usual small inductor or small power resistor of 0.22Ω should be inserted in the output lead.

One final point emerged from these experiments. I found that under some circumstances the amplifiers I tested sometimes oscillated at a low level, inexplicably. There was no indication from the simulations what might have

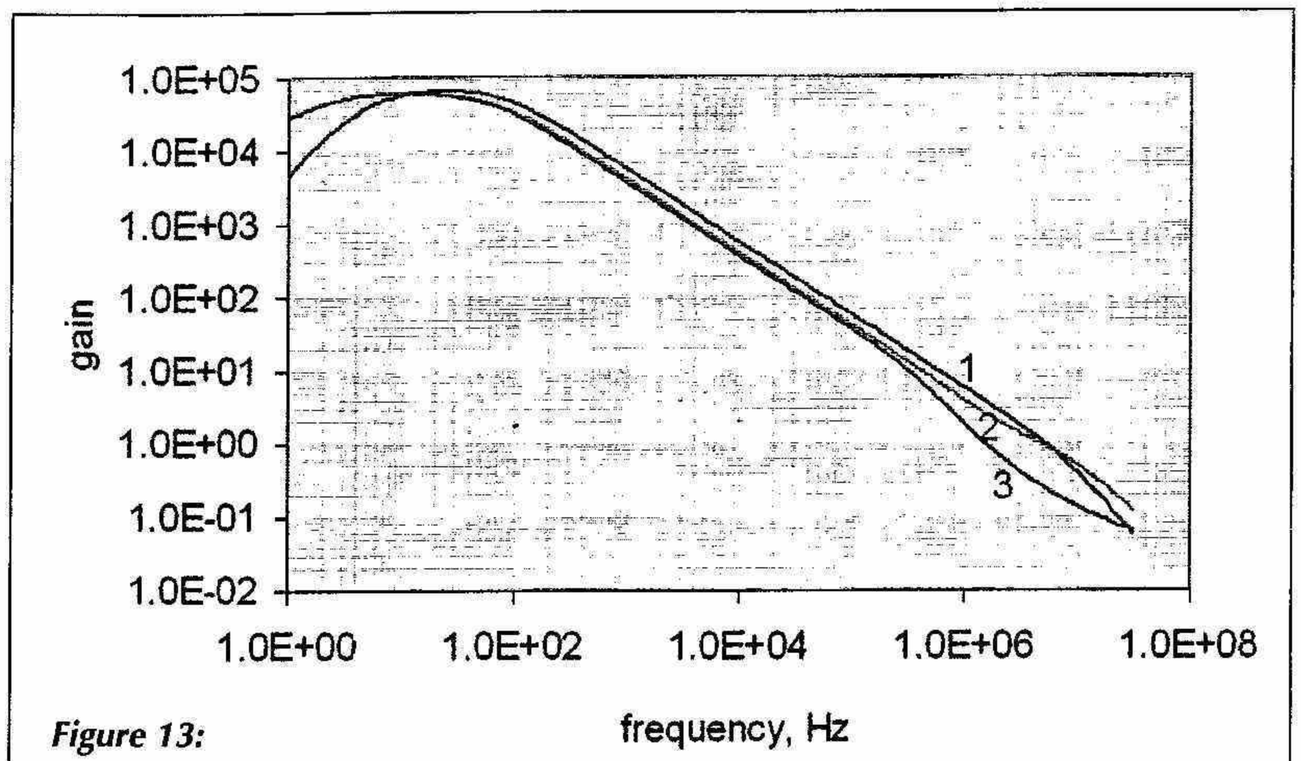


Figure 13:

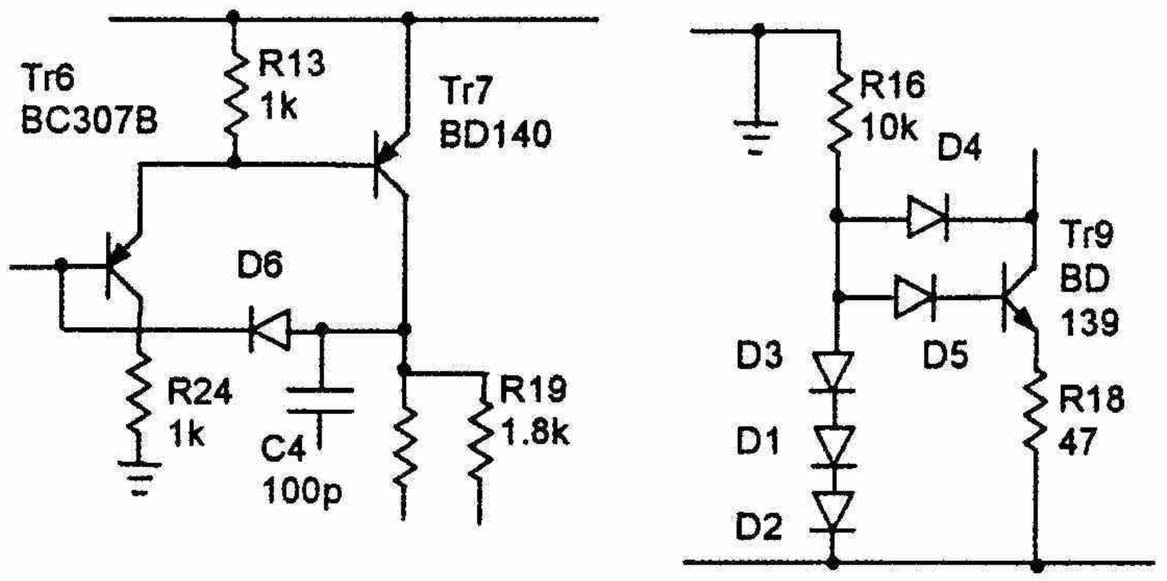


Figure 14: Adding anti-saturation diodes. All diodes are 1N4148 (but supply voltage must not exceed 75V total)

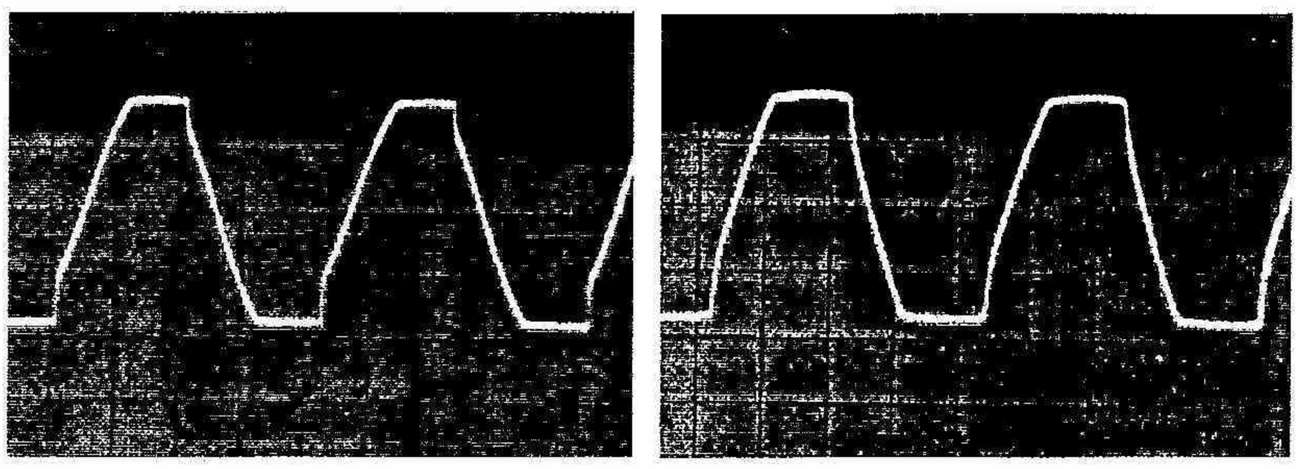


Fig 15(a): Clipping on conventional PLIL amplifier

Fig 15(b): Clipping with anti-saturation diodes added

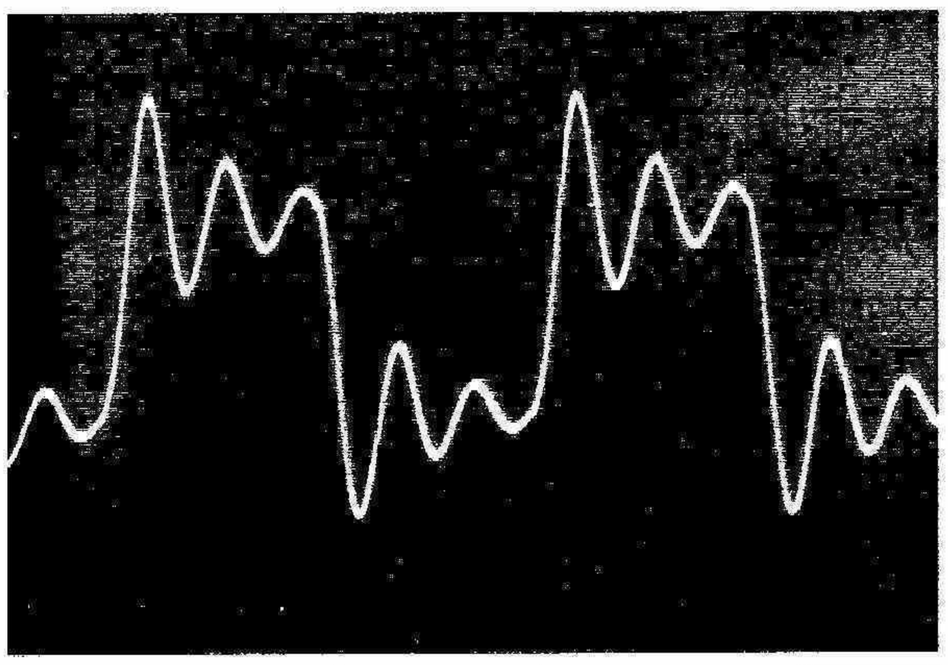


Fig 16: P.L.I.L amplifier response with 8Ω plus 2.2μF load at 10kHz. (vert 5V/div hor 20μS/div)

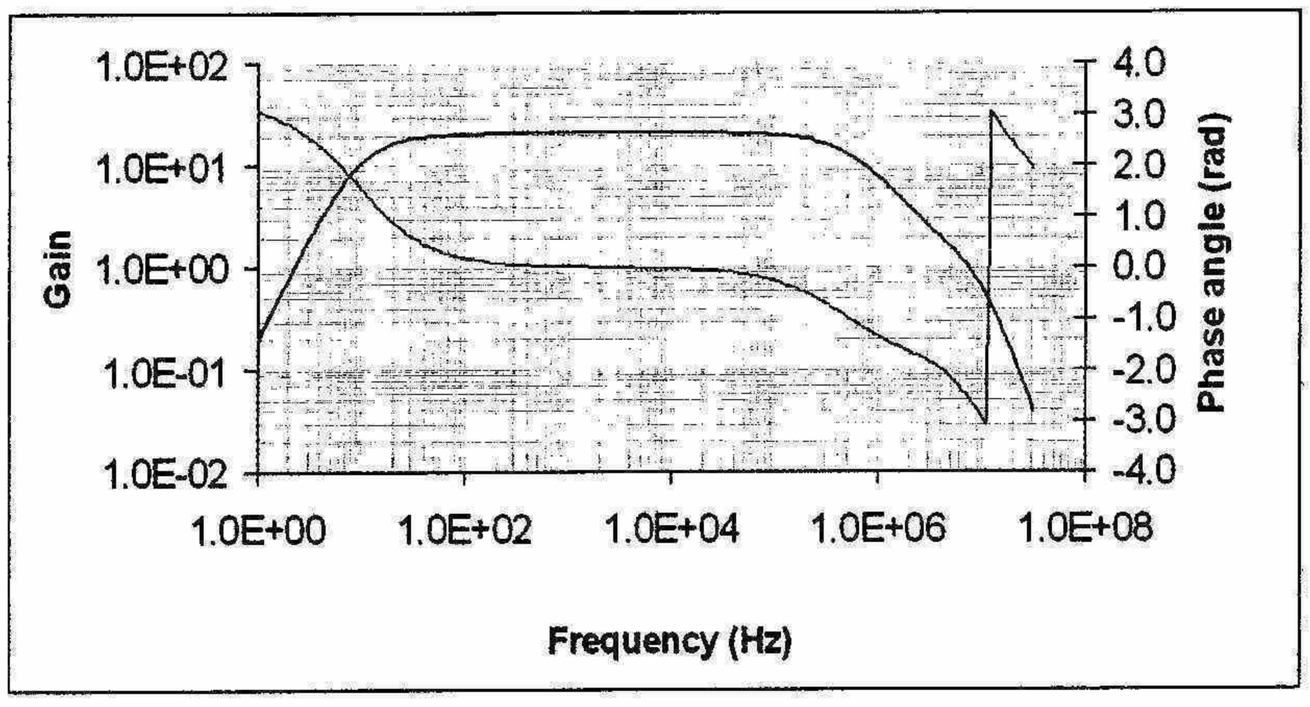


Fig. 17: Effect of 100 nH in a 0.33 ohm emitter resistor. The roll-off at the H.F. unity gain point is on an increasing slope and the phase shift is moving rapidly towards the unstable 180 degree point. The amplifier is bordering on instability. (compare with fig. 7(b)).

caused this but I suspected, from the problems with the protection circuitry, the emitter resistors. Measuring two wire-wound, 0.33Ω resistor samples I found that their impedances at 1MHz were no less than 0.6Ω for the 2.5Ω sample (corresponding to 60nH) and 0.8Ω (116nH) for the 5Ω sample. Bailey quite categorically stated that the emitter resistors should be non-inductive[9], and replacing the commercial resistors by a non-inductive helix (doubled-back) of 24 s.w.g. resistance wire eliminated the problem. I evaluated the effect of some inductance in the emitter resistor in my simulator. With just 100nH, the phase shift induced at around 5MHz, the unity gain point, is very nearly 180 degrees as indicated by the position of the step in the phase plot **(Fig. 17).** This confirms from simulation that inductive resistors can be a cause of spurious oscillations sometimes observed. I have yet to dare to test whether non-inductive resistors would allow the phase lead compensation capacitor to be connected to the output point rather than the collector of the VAS, though I suspect not, as three time-constants (two being significantly variable) are enclosed in such a feedback loop. Nevertheless, I would strongly reinforce Bailey's concern and state that the emitter resistors MUST be non-inductive. The simulations show that even small diameter helical windings, where the inductance is in the order of tens of nH, have too much inductance. Not only does this play havoc with the protection circuitry but also generates phase shifts right where they are least welcome. It may be possible to use a number of 1Ω metal film resistors in parallel, or series-parallel: measurements on the small, 1Ω type showed no significant change at 1MHz.

Figure 18: Class A amplifier for phase-lead/input lag compensation (adapted from Linsley-Hood's Simple Class A Amplifier. Output transistors require heatsink of 1° C/W or less).

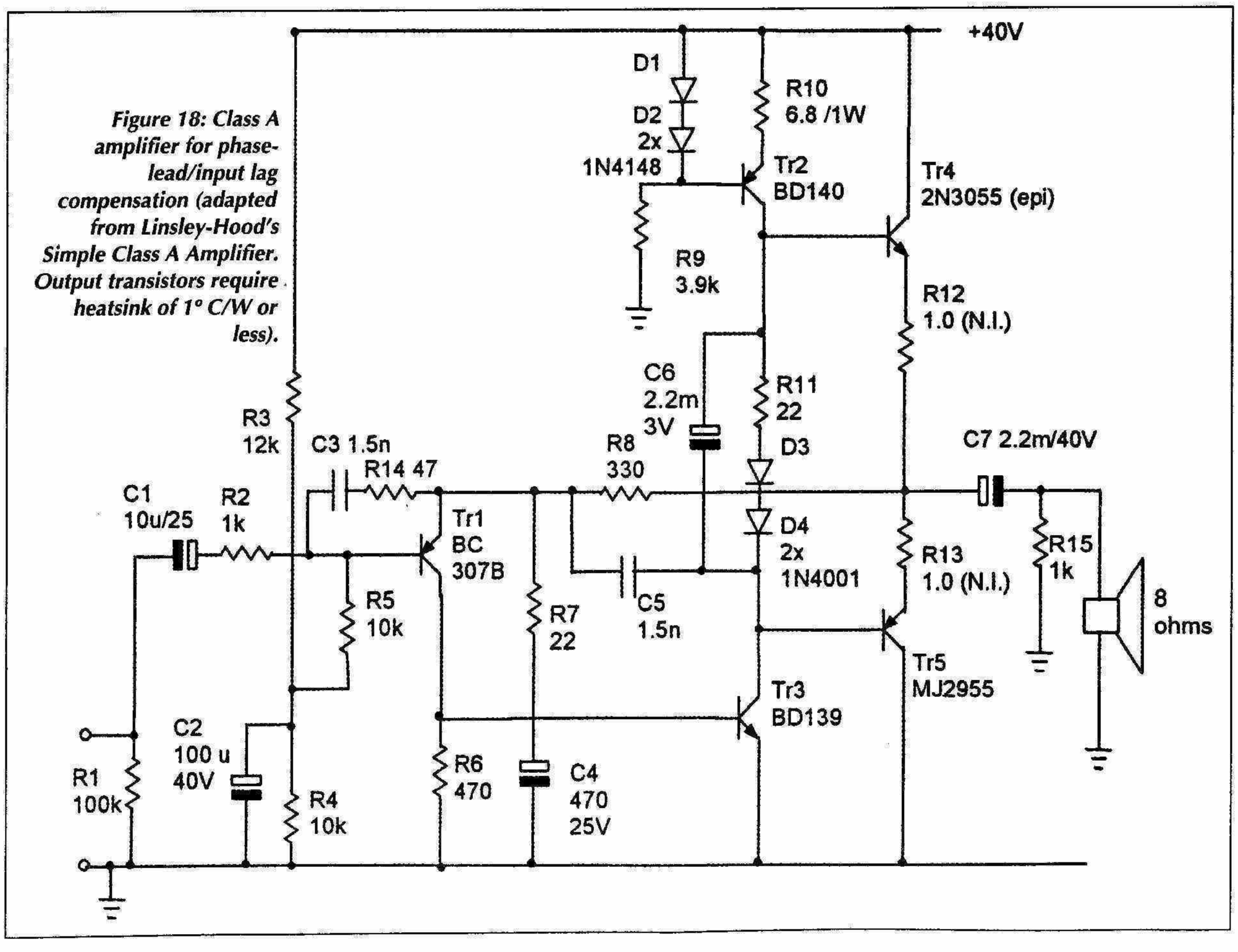
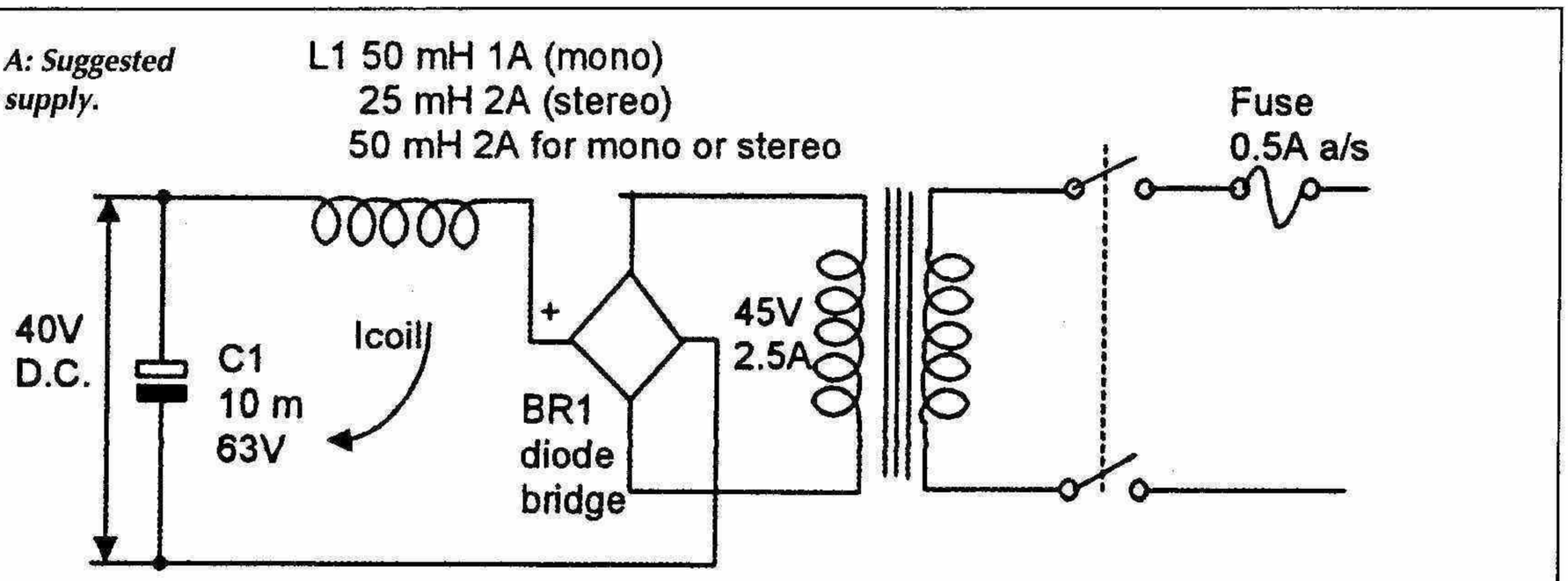


Figure A: Suggested power supply.



Choke filtered power supply - ideal for Class A as choke can be a simple air-gapped core for single current (not "saturating").
Note: earthing on the amplifier may be more critical to avoid circulating choke current flow, not easier!

In summary, a stable amplifier performance is possible with the phase-lead/input lag method when the input phase-lag is matched to the phase lead components. This has been supported through simulation. Distortion and noise may both be very slightly degraded compared with a phase-lag (Miller) amplifier, but this seems a small price to pay for a design which minimises the differential signal, and hence improves linearity, in the input transistors, particularly at high frequencies. High frequency distortion may increase slightly, so the time constants should be as high as possible. Whether the very sharp, odd harmonic distortions present at higher power levels, which are only around 1mV, cause listener fatigue is not something I can comment on.

The capacitor between the bases of the output transistors also acts to improve high frequency switching. Though I have some reservations about such a capacitor because, at high frequencies, it will pull charge from the output transistors in the same direction, despite the A.C. output signal, potentially charging unidirectionally, and reducing the driver transistor bias dynamically. However, it too helps to minimise parasitic oscillations, and on balance improves the switching speed, so is recommended.

Distortion arising from the compensation capacitor loading the VAS stage will arise to the same degree as in a Miller compensated amplifier as it increases loading at high frequencies. But the input transistors are spared the extra drive that this would have required from them since the differential signals remain low. As with all high performance amplifiers, the decoupling on the amplifier PCB needs to be good – as Self mentioned, power supply ripple should be prevented from entering the amplifier or it may appear as distortion.

I have shown through simulation, though fairly basic, how the method of using a combined phase lead and input phase lag compensation network can offer a possible alternative to the Miller capacitor. While I cannot say that all the issues with this approach have been unravelled, the phase-lag network operates as a two-pole, low-pass filter in the audio band. This achieves the objectives of an input filter and "slow" input stage at the same time, but without significantly impacting audio frequency bandwidth. Therefore, it is capable of providing similar performance to a Miller capacitor, but without requiring extensive local feedback (unless one counts the phase-lead network as local feedback). The method works with single and differential input stages. If a single-ended input stage requires an emitter resistor, there will be some increase in distortion due to the open loop gain reduction although this is partly offset by the extra local feedback the resistor introduces. The method can be used effectively in a 15W, modified version of Linsley-Hood's class A amplifier as shown in **Fig. 18.** ■

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