ABSOLUTE MAXIMUM RATINGS

(VSS=0V; Note 1)

Parameter		Symbol	min	max	Units
Power Supply	Analog Power Supply	VA	-0.3	4.6	V
	Digital Power Supply	VD	-0.3	4.6	V
Input Current (Any Pin Except Supplies)		IIN	-	±10	mA
Analog Input Voltage (LIN, RIN pin)		VINA	-0.3	VA+0.3	V
Digital Input Voltage		VIND	-0.3	VD+0.3	V
Ambient Temperature (power applied)		Ta	-40	85	◦C
Storage Temperature		Tstg	-65	150	◦C

Note: 1. All voltages with respect to ground.

WARNING: Operation at or beyond these limits may results in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(VSS=0V; Note 1)

Parameter		Symbol	min	typ	max	Units
Power Supply	Analog Power Supply	VA	2.4	3.0	4.0	V
	Digital Power Supply (Note 2)	VD	2.4 or VA-0.3	3.0	4.0	V

Note: 1. All voltages with respect to ground.
Note: 2. Min Value is high value either 2.4V or VA-0.3V.

*AKM assumes no responsibility for the usage beyond the conditions in this data sheet.

ANALOG CHARACTERISTICS

(Ta=25◦C; VA, VD=3.0V; VSS=0V; fs=44.1kHz; Signal Frequency=1kHz; BCLK=64fs;
Measurement frequency=10Hz ~20kHz at fs=44.1kHz, 20Hz ~40kHz at fs=96kHz; unless otherwise specified)

Parameter			min	typ	max	Units
ADC Analog Input Characteristics: (Note 3)						
Resolution					24	Bits
S/(N+D)	(-0.5dB Input)	fs=44.1kHz	80	89		dB
		fs=96kHz	80	89		dB
D-Range	(-60dB Input)	fs=44.1kHz, A-weighted	90	97		dB
		fs=96kHz	87	94		dB
		fs=96kHz, A-weighted	-	100		dB
S/N		fs=44.1kHz, A-weighted	90	97		dB
		fs=96kHz	87	94		dB
		fs=96kHz, A-weighted	-	100		dB
Interchannel Isolation			90	110		dB
Interchannel Gain Mismatch				0.2	0.5	dB
Input Voltage		(Note 4)	1.65	1.85	2.05	Vpp
Input Resistance		fs=44.1kHz	20	34	-	kΩ
		fs=96kHz	14	24	-	kΩ
DAC Analog Output Characteristics:						
Resolution					24	Bits
S/(N+D)	(0dB Output)	fs=44.1kHz	78	88		dB
		fs=96kHz	75	85		dB
D-Range	(-60dB Output)	fs=44.1kHz, A-weighted	93	100		dB
		fs=96kHz	88	96		dB
		fs=96kHz, A-weighted	-	100		dB
S/N		fs=44.1kHz, A-weighted	93	100		dB
		fs=96kHz	88	96		dB
		fs=96kHz, A-weighted	-	100		dB
Interchannel Isolation			90	110		dB
Interchannel Gain Mismatch				0.2	0.5	dB
Output Voltage		(Note 4)	1.56	1.75	1.94	Vpp
Load Resistance			10			kΩ
Load Capacitance					30	pF
Power Supplies						
Power Supply Current (VA+VD)						
Power up		PDN = “H”	fs=44.1kHz		14	21	mA
			fs=96kHz		18	27	mA
Power down	(Note 5)	PDN = “L”			10	100	μA

Note: 3. The offset of ADC is removed by internal HPF.
Note: 4. Input/Output of ADC and DAC scales with VA voltage. (ADC = 0.617 x VA, DAC = 0.583 x VA)
Note: 5. In case of power-down mode, all digital input including clocks pins (MCLK, BCLK, LRCK) are held VD or VSS. But PDN pin is held VSS.

FILTER CHARACTERISTICS

(Ta=25◦C; VA, VD=2.4 ~4.0V; fs=44.1kHz; DEM0="1", DEM1="0")

Parameter		Symbol	min	typ	max	Units
ADC Digital Filter (Decimation LPF):						
Passband (Note 6)	±0.1dB	PB	0		17.4	kHz
	-1.0dB			20.0		kHz
	-3.0dB			21.1		kHz
Stopband (Note 6)		SB	27.0			kHz
Passband Ripple		PR			±0.1	dB
Stopband Attenuation		SA	65			dB
Group Delay (Note 7)		GD		17.0		1/fs
Group Delay Distortion		GD		0		μs
ADC Digital Filter (HPF):						
Frequency Response (Note 6)	-3dB	FR		3.4		Hz
	-0.5dB			10		Hz
	-0.1dB			22		Hz
DAC Digital Filter:						
Passband (Note 6)	±0.1dB	PB	0		20.0	kHz
	-6.0dB			22.05		kHz
Stopband (Note 6)		SB	24.1			kHz
Passband Ripple		PR			±0.06	dB
Stopband Attenuation		SA	43			dB
Group Delay (Note 7)		GD		15.4		1/fs
Group Delay Distortion		GD		0		μs
DAC Digital Filter + Analog Filter						
Frequency Response 0 ~20.0kHz		FR		±0.5		dB
~40.0kHz (Note 8)				±1.0		dB

Note: 6. The passband and stopband frequencies scale with fs (sampling frequency).
For examples, PB=20.0kHz(@ADC: -1.0dB, DAC: -0.1dB) are 0.454 x fs.

Note: 7. The calculating delay time which occurred by digital filtering. This time is from the input of analog signal to setting the 24bit data of both channels to the output register for ADC. For DAC, this time is from setting the 24bit data of both channels on input register to the output of analog signal.

Note: 8. fs=96kHz.

DC CHARACTERISTICS

(Ta=25◦C; VA, VD=2.4 ~4.0V)

Parameter	Symbol	min	typ	max	Units
High-Level Input Voltage	VIH	70%VD	-	-	V
Low-Level Input Voltage	VIL	-	-	30%VD	V
High-Level Output Voltage (Iout=-20μA)	VOH	VD-0.1	-	-	V
Low-Level Output Voltage (Iout=20μA)	VOL	-	-	0.1	V
Input Leakage Current	Iin	-	-	±10	μA

SWITCHING CHARACTERISTICS

(Ta=25◦C; VA, VD=2.4 ~4.0V; C_L=20pF)

Parameter	Symbol	min	typ	max	Units
Master Clock Timing					
Frequency	fCLK	2.048		38.4	MHz
Pulse Width Low	tCLKL	10			ns
Pulse Width High	tCLKH	10			ns
LRCK Frequency					
Normal Speed	fsn	8		50	kHz
Double Speed	fsd	50		100	kHz
Quad Speed	fsq	100		200	kHz
Duty Cycle	Duty	45		55	%
Serial Interface Timing					
BCLK Period					
Normal Speed	tBCK	1/96fsn			ns
Double Speed	tBCK	1/64fsd			ns
Quad Speed	tBCK	1/64fsq			ns
BCLK Pulse Width Low	tBCKL	33			ns
Pulse Width High	tBCKH	33			ns
LRCK Edge to BCLK "↑" (Note 9)	tLRB	20			ns
BCLK "↑" to LRCK Edge (Note 9)	tBLR	20			ns
LRCK Edge to SDTO (MSB)	tDLR			40	ns
BCLK "↓" to SDTO	tDBS			40	ns
SDTI Hold Time	tSDH	20			ns
SDTI Setup Time	tSDS	20			ns
Reset Timing					
PDN Pulse Width	tPW	150			ns
PDN "↑" to SDTO Valid (Note 10)	tPWV		2081		1/fs

Note: 9. BCLK rising edge must not occur at the same time as LRCK edge.

Note: 10. These cycles are the number of LRCK rising from PDN rising.