SECTION 2. AUDIO PART

ADJUSTMENTS

This set has been aligned at the factory and normally will not require further adjustment. As a result, it is not recommended that any attempt is made to modificate any circuit. If any parts are replaced or if anyone tampers with the adjustment, realignment may be necessary.

IMPORTANT

1. Check Power-source voltage.
2. Set the function switch to band being aligned.
3. Turn volume control to minimum unless otherwise noted.
4. Connect low side of signal source and output indicator to chassis ground unless otherwise specified.
5. Keep the signal input as low as possible to avoid AGC and AC action.

TAPE DECK ADJUSTMENT

1. AZIMUTH ADJUSTMENT

Deck Mode	Test Tape	Test Point	Adjustment	Adjust for
Palyback	MTT-114	Speaker Out	DECK Screw Azimuth Screw	Maximum

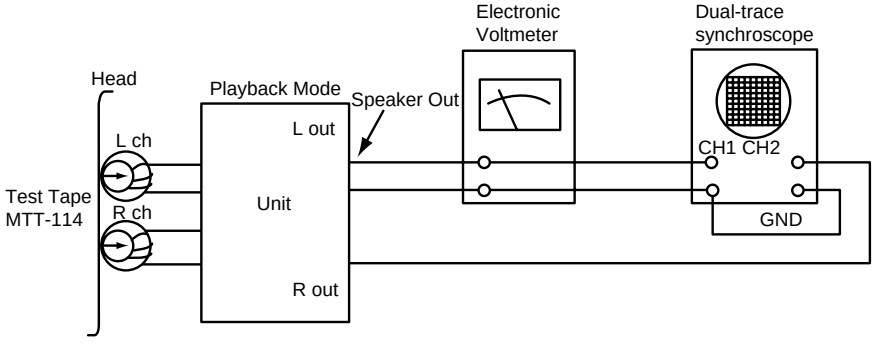


Figure 1. Azimuth Adjustment Connection Diagram

2. RECORD BIAS ADJUSTMENT

Deck Mode	Test Tape	Test Point	Adjustment	Adjust for
Rec/Pause	MTT-5511	ERASE HEAD WIRE(PN201)	L201	60kHz±5kHz (Auto stop) 85kHz±5kHz(Auto Reverse)

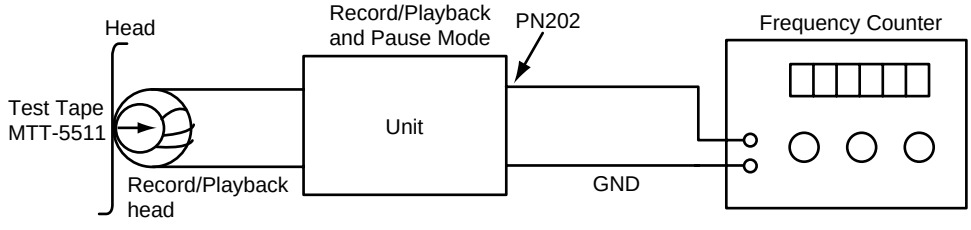
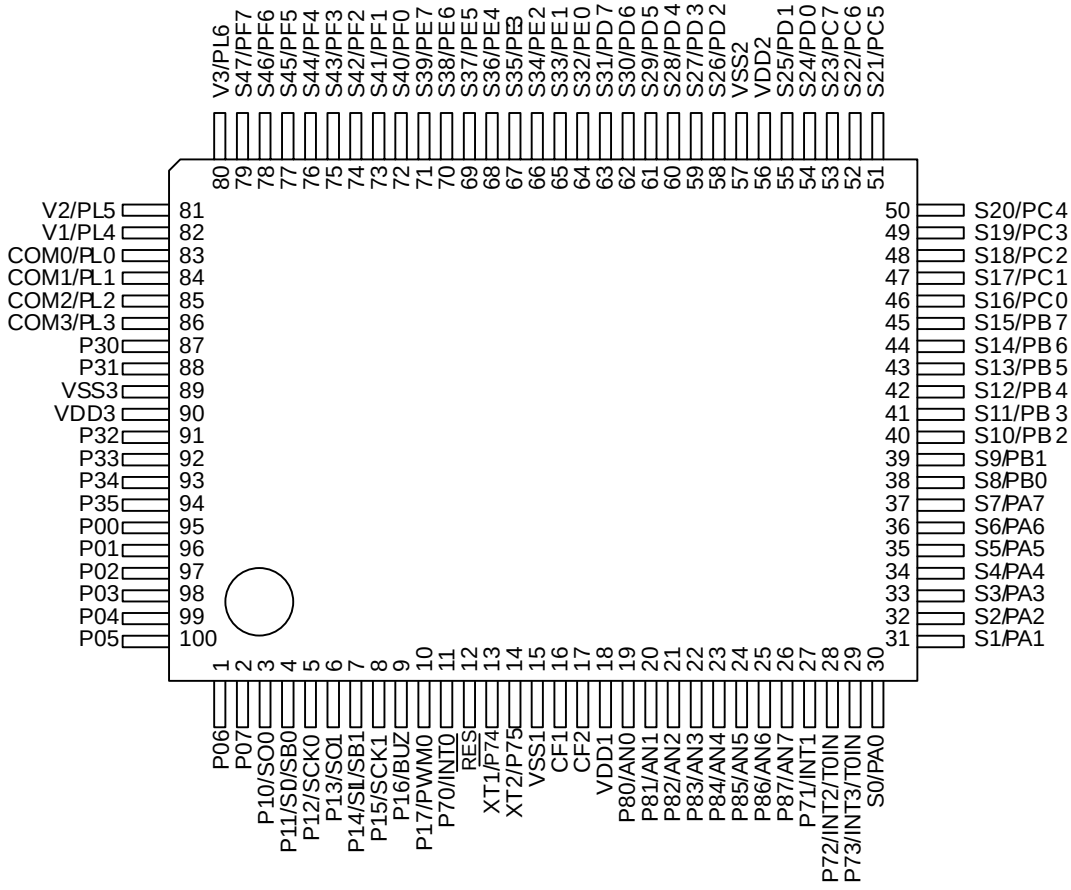


Figure 2. Record Bias Adjustment Connection Diagram

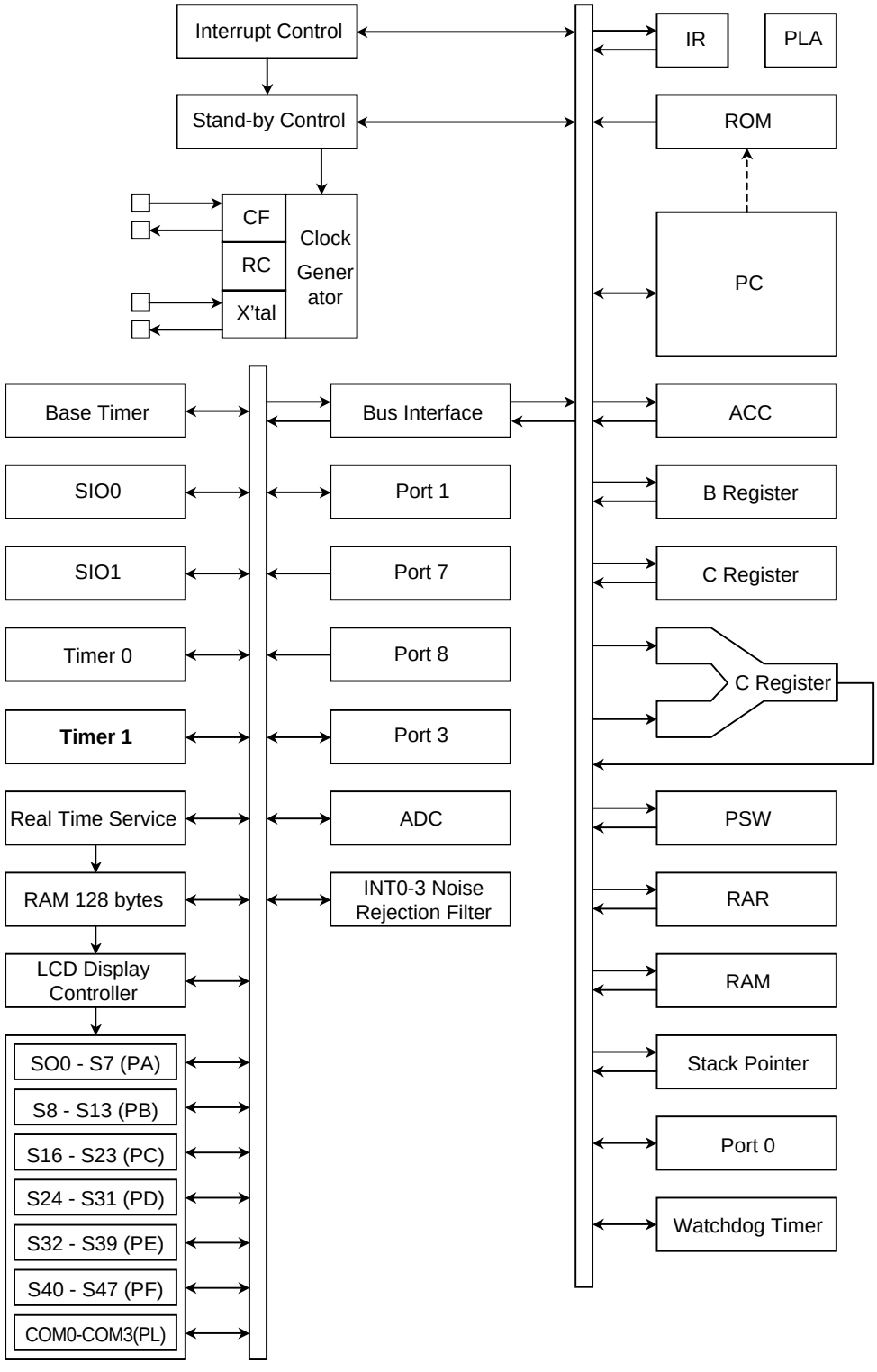
3. TUNER ADJUSTMENT

Non-adjusting

Pin Assignment



System Block Diagram



Pin Description

<table>
<tr><th>Pin name</th><th>I/O</th><th>Function description</th><th>Option</th></tr>
<tr><td>VSS1, 2, 3</td><td>-</td><td>Power pin (–)</td><td>-</td></tr>
<tr><td>VDD1, 2, 3</td><td>-</td><td>Power pin (+)</td><td>-</td></tr>
<tr><td>PORT0

P00 - P07</td><td>I/O</td><td>• 8-bit input/output port
Input/output in nibble units
• Input for port 0 interrupt
• Input for HOLD release</td><td>• Pull-up resistor :
Provided/Not provided
(specified in nibble units)
• Output form (P00 – P07) :
CMOS/N-channel open drain(specified in a bit)</td></tr>
<tr><td>PORT1
P10 - P17</td><td>I/O</td><td>• 8-bit input/output port
Input/output can be specified in bit unit
• Other pin functions
P10 SIO0 data output
P11 SIO0 data input/bus input/output
P12 SIO0 clock input/output
P13 SIO1 data output
P14 SIO1 data input/bus input/output
P15 SIO1 clock input/output
P16 Buzzer output
P17 Timer1 output (PWM output)</td><td>• Output form :
CMOS/N-channel open drain
(specified in a bit)</td></tr>
<tr><td>PORT3
P30 - P35</td><td>I/O</td><td>• 6-bit input/output port
• Input/output in nibble units</td><td>• Output form :
CMOS/N-channel open drain
(specified in a bit)</td></tr>
<tr><td>PORT7

P70

P71 - P73

$\overline{P74}$ - P75</td><td>

I/O

1

I</td><td>• 6-bit input port
• Other pin functions
P70 : INT0 input/HOLD release input/
N-channel Tr. output for watchdog timer
P71 : INT1 input/HOLD release input
P72 : INT2 input/timer 0 event input
event input
• Interrupt received form, vector address

$\overline{P74}$: XT1 terminal for crystal oscillation
P75 : XT2 terminal for crystal oscillation</td><td>Pull-up resistor :
Provided/Not provided
(specified in a bit)
(P70, P71, P72, P73)
* $\overline{P74}$, P75 don't have the pull-up resistor option.</td></tr>
<tr><td>Port8
P80 – P87</td><td>I</td><td>• 8-bit input port
• Other function
AD input port (8 port pins)</td><td>-</td></tr>
</table>

	rising	falling	rising & falling	high level	low level	vector
INT0	enable	enable	disable	enable	enable	03H
INT1	enable	enable	disable	enable	enable	0BH
INT2	enable	enable	enable	disable	disable	13H
INT3	enable	enable	enable	disable	disable	1BH

Pin name	I/O	Function description	Option
PORT A (S0/PA0 – S7/PA7)	I/O	• Segment output terminal for LCD display • Can be used as a general input/output port	-
PORT B (S8/PB0 – S15/PB7)	I/O	• Segment output terminal for LCD display • Can be used as a general input/output port	-
PORT C (S16/PC0 – S23/PC7)	I/O	• Segment output terminal for LCD display • Can be used as a general input/output port	-
PORT D (S24/PD0 – S31/PD7)	I/O	• Segment output terminal for LCD display • Can be used as a general input/output port	-
PORT E (S32/PE0 – S39/PE7)	I/O	• Segment output terminal for LCD display • Can be used as a general input/output port	-
PORT F (S40/PF0 – S47/PF7)	I/O	• Segment output terminal for LCD display • Can be used as a general input/output port	-
PORT L (COM0/PL0 – COM3/PL7)	I/O	• Common output terminal for LCD display • Can be used as a general input port	-
V1/PL4 – V3/PL6	I	• Bias power terminal for LCD drive • Can be used as a general input port	-
$\overline{RES}$	I	Reset pin	-
XT1/ $\overline{P74}$	I	• Input pin for 32.768kHz crystal oscillation In case of non use, connect to VDD. • Other function A general input port $\overline{P74}$	-
XT2/P75	O	• Output pin for 32.768kHz crystal oscillation In case of non use, should be left unconnected • Other function A general input port P75	-
CF1	I	Input pin for ceramic resonator oscillation	-
CF2	O	Output pin for ceramic resonator oscillation	-

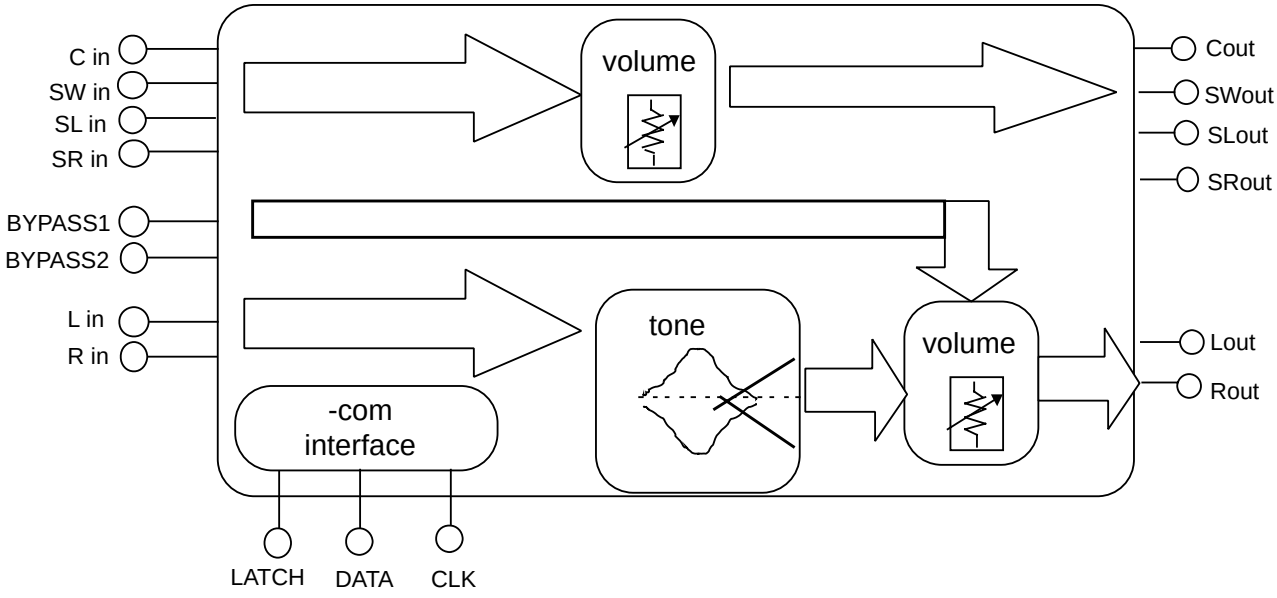
* All of port options can be specified in bit unit except the pull-up resistor of port 0.

* A state of pins at reset

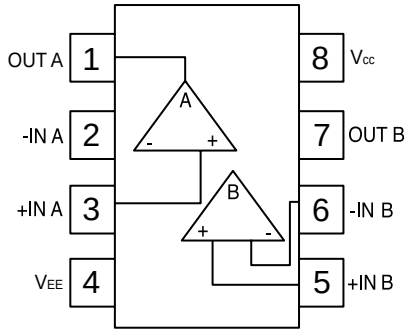
Pin name	I/O mode	A state of pull-up resistor specified at pull-up option
Port 0	Input	Fixed pull-up resistor OFF
Port 1	Input	Programmable pull-up resistor OFF
Port 3	Input	Programmable pull-up resistor OFF
Ports 70, 71, 72, 73	Input	Fixed pull-up resistor OFF
XT1/ P74 , XT2/P75	Input	General input port as P74 , P75 (If using as the crystal oscillation, the specified register must be set.)

Pin name	I/O mode
Ports A, B, C, D, E, F	Output OFF

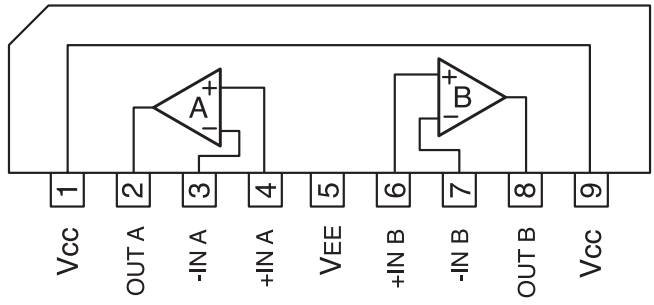
■ M62446FP



■ KIA4558P, KIA4558F



■ KIA4558S



PIN CONFIGURATION AND IC INTERNAL BLOCK DIAGRAM